

# Crosstalk-noise-aware bus coding with low-power ground-gated repeaters

**Citation for published version (APA):**

Jiao, H., Wang, R., & He, Y. (2018). Crosstalk-noise-aware bus coding with low-power ground-gated repeaters. *International Journal of Circuit Theory and Applications*, 46(2), 280-289. <https://doi.org/10.1002/cta.2378>

**DOI:**

[10.1002/cta.2378](https://doi.org/10.1002/cta.2378)

**Document status and date:**

Published: 01/02/2018

**Document Version:**

Accepted manuscript including changes made at the peer-review stage

**Please check the document version of this publication:**

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

**General rights**

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

[www.tue.nl/taverne](http://www.tue.nl/taverne)

**Take down policy**

If you believe that this document breaches copyright please contact us at:

[openaccess@tue.nl](mailto:openaccess@tue.nl)

providing details and we will investigate your claim.

# Crosstalk-Noise-Aware Bus Coding with Low-Power Ground-Gated Repeaters

<sup>1,2</sup>Hailong Jiao, <sup>2</sup>Rui Wang, <sup>3,2</sup>Yifan He

<sup>1</sup>School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School  
Li-Shui Road 2199, Shenzhen, P. R. China

<sup>2</sup>Electronic Systems group, Department of Electrical Engineering, Eindhoven University of Technology  
Den Dolech 2, 5612 AZ, Eindhoven, The Netherlands

<sup>3</sup>Xiamen University of Technology, Xiamen, Fujian, P. R. China  
Email: jiaohl@pkusz.edu.cn; r.wang@student.tue.nl; y.he@xmut.edu.cn

April 17, 2017

## SUMMARY

Crosstalk noise is one of the serious reliability concerns in nanoscale integrated circuits. Repeater insertion together with shielding wires is a typical method to suppress crosstalk noise associated with global data bus. A new crosstalk-noise-aware bus coding scheme with ground-gated repeaters is proposed in this paper to minimize the routing overhead as well as power consumption of data bus systems. A subset of 4-to-6 crosstalk-noise-aware codes is selected to minimize the number of simultaneous data transitions. The routing overhead is reduced by 12.31% with the new bus coding scheme compared to the conventional data bus with shielding wires. Furthermore, the leakage power and worst-case active power consumptions are reduced by 12.5% and 18.26%, respectively, with the new crosstalk-noise-aware data bus system as compared to the previously published bus coding system in an industrial 40nm CMOS technology.

**KEY WORDS:** Global interconnect, sleep transistor, leakage power, active power, routing overhead.

## 1. INTRODUCTION

Higher quality-of-experience requirements of integrated circuits lead to increased number of on-chip transistors that boosts both performance and functionality. The chip areas therefore tend to increase in each new CMOS technology generation despite the miniaturized transistors [1] – [3]. The global interconnects, which are elongated with larger chips, suffer from serious signal integrity issues such as crosstalk noise, which is primarily caused by capacitive coupling between interconnects [4], [5]. Crosstalk noise causes longer propagation delay, higher power consumption, and degraded noise margin in nanoscale CMOS integrated circuits.

Repeater (inverter/buffer) insertion is the most commonly used technique to deal with signal integrity issues in global interconnects [6] – [9]. By inserting repeaters along a long wire, each segment of the divided interconnect is strongly driven by the inserted buffers. The immunity of interconnects to crosstalk noise is thereby enhanced. Hundreds of thousands of repeaters are inserted along global interconnects, a significant amount of which are used for data buses, in state-of-the-art microprocessors [2], [3]. These repeaters consume huge amount of dynamic power in active mode and leakage power in idle status. Development of novel low-power and robust data bus system where a large number of repeaters drive long wires is therefore highly desirable.

A new crosstalk-noise-aware bus coding scheme with low-power ground-gated repeaters is proposed in this paper. The new bus coding scheme is employed to minimize the crosstalk noise between neighboring

global interconnects with minimal aid of power or ground shielding. The routing overhead is thereby reduced with the new bus coding scheme compared to the conventional power and ground wire shielding techniques. The sizes of the sleep transistors are miniaturized with the new bus coding scheme, thereby reducing the leakage power consumption compared to a previously published data bus system with ground-gated repeaters. Furthermore, the switching probability of the data along the global buses is reduced with the proposed bus coding scheme, thereby reducing the active power consumption compared to the previously published ground-gated repeater technique for driving long global interconnects in complex nanoscale CMOS integrated circuits.

The paper is organized as follows. The existing crosstalk noise reduction techniques are reviewed in Section 2. The new crosstalk-noise-aware bus coding scheme with low-power ground-gated repeaters is presented in Section 3. Different crosstalk-noise-aware data bus systems are optimized and evaluated in Section 4. The paper is summarized in Section 5.

## 2. EXISTING CROSSTALK NOISE REDUCTION TECHNIQUES

Since crosstalk noise is a critical reliability issue in integrated circuits, various bus coding techniques have been proposed to mitigate the impact of crosstalk noise. The analysis of crosstalk noise is presented in Section 2.1. The existing crosstalk-noise-aware bus coding schemes are introduced as well. In Section 2.2, the previously published crosstalk-noise-aware bus coding scheme with ground-gated buffers is reviewed.

### 2.1. Crosstalk Noise on Data Bus and Noise Reduction

The amplitude of crosstalk noise is affected by the switching signal patterns on adjacent wires. There are three possible signal switching scenarios on a single wire: switching from 0 to 1 ( $\uparrow$ ), switching from 1 to 0 ( $\downarrow$ ), or no switching activity (-). Combining all the possible signal switching patterns on two adjacent wires, there are four types of switching scenarios as listed in Table I. For Type 1, there is no switching activity on both wires, thereby resulting in no crosstalk noise. For Type 2, the voltage level on one wire switches either from 0 to 1 or from 1 to 0, while the other wire has no switching activity. Crosstalk noise is induced on the quiet wire due to the coupling capacitance between the two wires. For Type 3, both wires switch to the same direction, so that the coupling capacitance is weakly charged or discharged. There is therefore marginal crosstalk between the two adjacent wires for Type 3 switching scenario. For Type 4, two wires switch in the opposite directions. In this case, the effective coupling capacitance between these two wires is significantly higher than the other three scenarios. The maximum (worst-case) crosstalk noise therefore occurs under the Type 4 switching scenario.

Existing crosstalk noise reduction techniques typically aim to eliminate the worst-case crosstalk noise by avoiding the Type 4 signal switching scenario. The conventional method to suppress crosstalk noise between interconnects is to put a power/ground wire (shielding wire) between every two adjacent signal wires on a data bus [2], [3], as shown in Fig. 1. Since the shielding wires are permanently connected to either  $V_{DD}$  or ground, only Type 1 or Type 2 switching scenarios in Table I occur between the shielding wire and the signal wire. The conventional shielding method is therefore effective in eliminating crosstalk noise. However, large routing overhead is caused due to the additional wide shielding wires since the current electronic design automation (EDA) tools have difficulty in reusing those shielding power/ground wires.

In order to reduce the large routing overhead that is caused by the additional shielding wires, a bus coding methodology is proposed in [10]. Instead of transmitting the data on the original data bus directly, an encoder is inserted at the source of the data bus to encode the input data before data transmission, as shown in Fig. 2. The encoded data is transmitted on the data bus to the sink where a decoder is used to translate the encoded data into the original value. These codes are commonly referred to as Crosstalk Avoidance Codes (CACs) [14]. A unique feature of the encoded data is that no Type 4 switching scenario exists between any two

adjacent wires on the bus since crosstalk-noise-aware bus coding is employed in this scheme. No shielding wire is needed to be inserted between two adjacent signal wires on the bus, thereby significantly reducing the number of global wires in the bus system. A similar technique, which is commonly referred to as forbidden pattern coding, is proposed in [11] to prohibit 010 and 101 patterns from codewords, thereby eliminating the Type 4 switching scenario. While reducing the number of global wires along the bus compared to the conventional shielding method, the forbidden pattern coding technique requires similar amount of global wires compared to the crosstalk avoidance coding technique in [10]. A variety of follow-up works propose different techniques to generate either the Crosstalk Avoidance Codes or the Forbidden Pattern Codes (FPCs) in an efficient way [12] – [15]. However, these works only focus on the coding scheme, yet overlook the power consumption issue of the bus system. Alternatively, in this paper, a power-friendly crosstalk-noise-aware bus coding scheme is proposed to not only suppress the crosstalk noise (by eliminating the Type 4 switching scenario), but also minimize the power consumption of the data bus system.

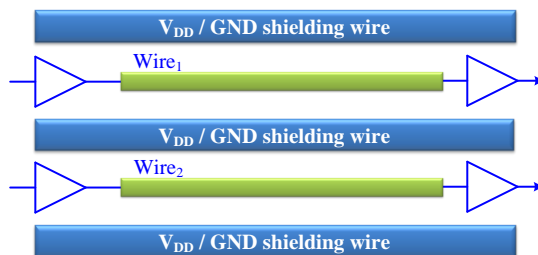


Fig. 1. Conventional crosstalk noise reduction with shielding wires [2], [3].

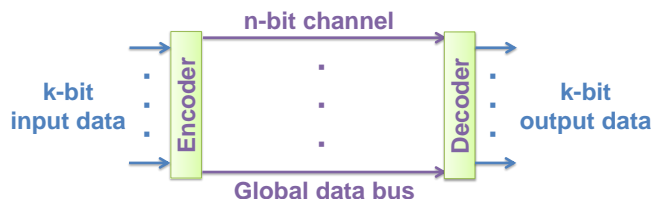


Fig. 2. Crosstalk noise reduction with noise-aware bus coding [10].

## 2.2. Crosstalk-Noise-Aware Bus Coding with Ground-Gated Buffers

Power/ground gating is the most commonly used circuit technique for leakage power reduction [18] – [20]. In a power/ground gated circuit, high threshold voltage (HVT) sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle circuit block. Ground gating is used in [9] to suppress the leakage currents that are produced by the repeaters inserted along the data bus. A 3-to-4 crosstalk-noise-aware coding scheme that is proposed in [10] is adopted in [9]. A wide data bus is divided into multiple groups. Each group contains three bits which are encoded into four crosstalk-noise-aware bits (the last two bits are not encoded in a 32-bit data bus case, see Fig. 3). A power/ground shielding wire is required to be inserted between the adjacent groups of the 4-bit encoded data. Footer sleep transistors are used for repeater leakage reduction, as shown in Fig. 3. Since two adjacent buffers along the same wire are separated from each other for long distance, sharing the same footer sleep transistor with all repeaters is difficult. Therefore, a column of repeaters along the bus, which are physically close to each other, shares a footer sleep transistor as shown in Fig. 3. The ground gating bus coding scheme in [9] is effective in both suppressing crosstalk noise and reducing leakage power consumption of the interconnect buffers. However, the coding scheme that is used in [9] is far from optimized for both leakage power and dynamic power reductions while employing ground gating technique. In this paper, while employing group gating technique

for the buffers along the bus, alternative power-efficient crosstalk-noise-aware bus coding schemes are explored to achieve lower power consumption compared to the 3-to-4 crosstalk-noise-aware coding scheme that is proposed in [10] at the same crosstalk noise level.

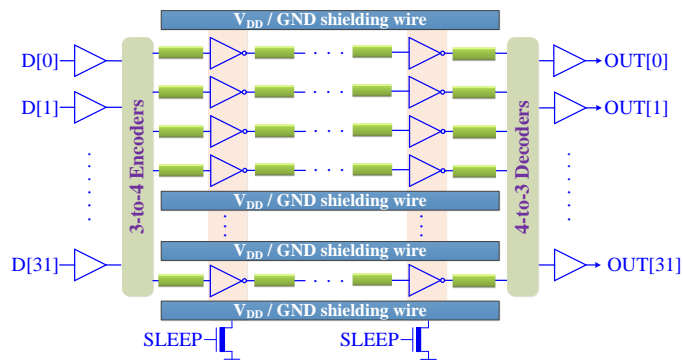


Fig. 3. Crosstalk noise reduction with 3-to-4 noise-aware bus coding [9]. Ground-gating is applied to repeaters. HVT sleep transistors are represented with thick line in the channel region.

### 3. NEW CROSSTALK-NOISE-AWARE BUS CODING SCHEME WITH GROUND-GATED REPEATERS

New crosstalk-noise-aware bus coding scheme with low-power ground-gated repeaters is proposed in this section to reduce both the leakage power consumed by the inserted repeaters in idle status and the dynamic power consumed by the repeaters in active mode.

For the crosstalk-noise-aware bus coding system that is shown in Fig. 2, the encoded data are defined as codeword [10]. A codeword is connected to another codeword if a transition between these two codewords does not incur Type 4 switching scenario. The neighbor set of one codeword is the set of codewords to which the codeword is connected. The degree ( $d_n$ ) of this neighbor set is the number of codewords inside this set [10]. The relationship between the data width  $n$  and  $d_n$  for noise-aware bus coding is listed in Table II. For example, when  $n = 4$  and  $d_n = 8$ , eight 4-bit codewords exist. Each of these eight codewords can make a transition to another codeword within this set without incurring Type 4 switching. Since  $d_n = 8$ , the maximum number ( $k$ ) of input bits that can be encoded is 3 ( $2^3 = 8$ ) as listed in Table II. Eight 3-bit input data can be encoded to eight 4-bit crosstalk-noise-aware data. A 3-to-4 encoder is used for encoding while a 4-to-3 decoder is used for decoding.

When 3-to-4 bus coding is utilized (the coding scheme that is used in [9]), the eight crosstalk-noise-aware codes are listed in Table III. When one coded data transitions to another coded data, the new data is propagated through the repeaters along the bus. Provided that ground gating technique (with footer sleep transistors) is applied to the repeaters, the sizes of the sleep transistors are determined by the data patterns that are propagated through the repeaters. For example, when the coded data “1011” transitions to “1000”, two repeaters among the eight repeaters in the two consecutive columns experience high-to-low transition at the outputs, as shown in Fig. 4(a). The discharging currents go through the NMOS transistors inside the repeaters as well as the footer sleep transistor to the ground. With higher discharging currents, larger sleep transistors are required to maintain high data transmission rate along the data bus. The worst-case discharging scenario occurs when the coded data “1111” transitions to “0000” or when the coded data “0000” transitions to “1111”, as shown in Fig. 4(b).

For a 32-bit data bus, the bus is divided into 12 groups for encoding. The ten groups with three input bits are encoded to four bits for transmission on the bus. The last two groups with one bit in each group are not encoded. A power/ground wire is inserted between the adjacent groups since boundary wires between the

adjacent groups cannot be guaranteed to avoid the Type 4 switching scenario. The total number of wires that are used for a 32-bit data bus is 55 (42 wires for data transmission + 13 shielding wires), as listed in Table II. For each group of the 4-bit encoded data, the maximum number of discharging repeaters in every two consecutive columns is four, as shown in Fig. 4(b). Therefore, the maximum number of discharging repeaters in every two consecutive columns is 42 assuming a 32-bit data bus (which is encoded to a 42-bit data bus).

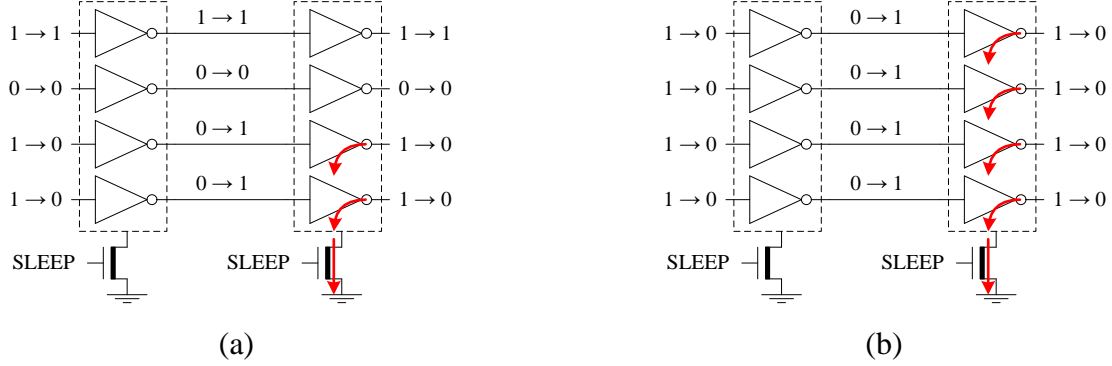


Fig. 4. The influence of data patterns on the sleep transistor size. (a) A data pattern with relatively low discharging currents, which results in smaller sleep transistors. (b) A data pattern with the maximized discharging currents, which results in larger sleep transistors.

Using the 3-to-4 coding scheme however maximizes the worst-case number of discharging repeaters. The footer sleep transistors therefore have to be sized significantly large to avoid serious performance degradation along the data bus. Alternative crosstalk-noise-aware bus coding schemes are explored in the paper for reducing the discharging currents through the footer sleep transistors, thereby minimizing the sizes of the sleep transistors. Provided that 4-to-6 coding scheme is employed, 21 crosstalk-noise-aware codes exist, as listed in Tables II and III. For 4-bit input data, 16 noise-aware codes are sufficient for the coding. Five codes among the 21 noise-aware codes are therefore redundant. Algorithm 1 is proposed to select the 16 required noise-aware codes while minimizing the discharging currents through the repeaters by using this 4-to-6 coding scheme. Based on the analysis for the 3-to-4 coding scheme, the amount of discharging currents that are caused by the transition from one encoded data to another encoded data is maximized when the number of different bits in the two encoded data is maximized. For example, there are 6 different bits between “111111” and “000000” while there are 4 different bits between “101111” to “000010”. The transition from “111111” to “000000” also produces higher discharging currents as compared to the transition from “101111” to “000010”. The encoded data that have the largest numbers of different bits compared to other encoded data are eliminated with Algorithm 1. For the 4-to-6 coding scheme, the maximum number of different bits between any two of the selected 16 codes is four. For a case of 32-bit data bus, the data bus is divided into eight groups for encoding. The eight groups with four input bits are encoded to six bits for transmission on the bus. The maximum number of discharging repeaters in every two consecutive columns is 32 assuming a 32-bit data bus (which is encoded into a 48-bit data bus). The maximum number of discharging repeaters is reduced by 23.81% with the 4-to-6 encoding scheme as compared to the 3-to-4 encoding scheme. The total size of the sleep transistors is therefore reduced with the 4-to-6 encoding scheme as compared to the 3-to-4 encoding scheme, thereby suppressing the leakage power consumption of the repeaters along the bus.

With the alternative bus coding scheme, such as 4-to-6 coding, the number of different bits between any two noise-aware codes is reduced as compared to the 3-to-4 coding. The amount of switching activities is therefore also reduced when the data on the global bus transitions from one to another. The dynamic power consumption, which is linearly related to the switching activities of the signals, is thereby also suppressed with these alternative bus coding schemes as compared to the 3-to-4 coding that is employed in [9].

---

**Algorithm 1** [Selection of power-efficient crosstalk-noise-aware codes]

---

```
1: Given
2:   NA_Code // A set of noise-aware codes
3:   n       // The length of each noise-aware code
4:   ini     // The total number of noise-aware codes
5:   req     // The required number of noise-aware codes
6:
7: Function difference(x, y)
8:   Initialization
9:   diff := 0 // Reset the number of different bits
10:  for i := 1 to n
11:    if x(i) != y(i)
12:      diff := diff + 1
13:    end if
14:  end for
15: end Function
16:
17: Main ()
18:  for i := 1 to ini-1
19:    for j := i to ini
20:      diff := difference(NA_Code(i), NA_Code(j))
21:      Store diff in an array diff_ar
22:    end for
23:  end for
24:  while ini > req
25:    Eliminate the maximum value in diff_ar and the two corresponding noise-aware codes
26:    ini := ini - 2
27:    if ini < req
28:      Add one of the two just eliminated noise-aware codes back to NA_Code and stop
29:    end if
30:  end while
```

---

The maximum number of different bits between any two encoded data (equivalent to the maximum number of discharging repeaters) and the total number of wires that are required for a 32-bit data bus with different encoding schemes are listed in Table II. The maximum number of different bits between any two noise-aware codes can be minimized to 32 with multiple coding schemes, such as 2-to-3, 4-to-6, 6-to-9, and 8-to-12 coding methods, in a 32-bit bus system (the bus width is 32 before coding). The total number of wires that are used for a 32-bit bus system is minimized to 49 with 8-to-12 coding method among the coding schemes that are listed in Table II. However, the encoder and decoder with the 8-to-12 coding method have significant delay, power consumption, and area overheads as compared to coding schemes such as 4-to-6 coding. 4-to-6 coding scheme provides a better tradeoff among the effectiveness in suppressing power consumption, the amount of wires used for the bus coding system, and the complexity of encoder and decoder. The 4-to-6 coding scheme is therefore employed in this study and compared with the conventional bus system without coding as well as the bus system with 3-to-4 coding scheme.

## 4. Optimization and Evaluation of Crosstalk-Noise-Aware Bus Coding Systems

Different on-chip data bus coding schemes are optimized and evaluated in this section. An industrial 40nm low-power multi-threshold voltage CMOS technology is used in this study.

### 4.1. Optimization of Bus Coding Systems

The design and optimization of the encoders, decoders, repeaters, and wires in the bus system are discussed in this section. For a particular coding scheme, the selected crosstalk-noise-aware codes (without redundant codes) are a set of codes without any order. The mapping from the original codes to the selected encoded codes determines the design complexity and power consumptions of the encoder and decoder. A heuristic searching algorithm is used to find the most power efficient mapping between the original data and the coded data. Assume that  $X$  and  $Y$  are two binary codes with the same length.  $X$  and  $Y$  are both either original codes or encoded codes. Define a function  $dif\_bit(X, Y)$  to measure the number of flipping bits between the two codes  $X$  and  $Y$ . For example,  $dif\_bit(000,111) = 3$  and  $dif\_bit(011,110) = 2$ . We define a new parameter *logic similarity* ( $LS$ ), where

$$LS = \sum_{i=1}^7 \sum_{j=i+1}^8 \left| dif\_bit(b_{i1}b_{i2}b_{i3}, b_{j1}b_{j2}b_{j3}) - dif\_bit(e_{i1}e_{i2}e_{i3}e_{i4}, e_{j1}e_{j2}e_{j3}e_{j4}) \right| \quad (1)$$

for the 3-to-4 coding case. The general expression of  $LS$  is

$$LS = \sum_{i=1}^{2^k-1} \sum_{j=i+1}^{2^k} \left| dif\_bit(B_i, B_j) - dif\_bit(E_i, E_j) \right|, \quad (2)$$

where  $B_i$  and  $E_i$  are the original data and the encoded data, respectively.  $k$  is the number of input bits that are to be encoded. For 3-to-4 encoding,  $k=3$ . The value of  $LS$  is related to the complexity and the dynamic power consumption of the encoder/decoder. Larger  $LS$  corresponds to more complicated CODEC and higher power consumption due to the higher switching activities. To achieve the lowest power consumption with the encoders/decoders, an exhaustive searching is performed to find out the mapping from the original codes to the encoded codes with the lowest  $LS$  for both 3-to-4 encoding and 4-to-6 encoding. The mappings with the 3-to-4 coding scheme and 4-to-6 coding scheme are listed in Table IV.

The global interconnects used for the data bus and the ground shielding wires are the top metal layer (Metal 8) in this industrial 40nm CMOS technology. The width of each global interconnect is  $0.4\mu\text{m}$ , which is the minimum width that is allowed in the layout design rule. The distance between the adjacent global interconnect is  $1.5\mu\text{m}$ , which is the minimum distance that is allowed in the layout design rule. The thickness of the Metal 8 is  $1.25\mu\text{m}$ . Assume that after buffer insertion, the bus interconnect is divided into  $N$  segments, each of which has a length of  $l$ . By adopting the optimization method in [8] and the values of parameters from the 40nm CMOS technology, the optimum length  $l_{opt}$  of interconnect between every two repeaters is  $1095\mu\text{m}$ . When low threshold voltage (LVT) transistors with minimum channel length ( $L = 40\text{nm}$ ) are used, the optimum width of the NMOS transistor in the repeaters is  $21\mu\text{m}$ . The width of the PMOS transistor in the repeaters is sized to be  $42\mu\text{m}$  to achieve symmetric pull-up and pull-down strengths in the repeaters.

### 4.2. Evaluation of Bus Coding Systems

Different on-chip data bus coding schemes, including the conventional data bus with ground shielding, the previously published 3-to-4 crosstalk-noise-aware bus coding with ground-gated repeaters, and the newly proposed 4-to-6 crosstalk-noise-aware bus coding with ground-gated repeaters, are evaluated in this section. 32-bit data bus is used in this study. For the conventional data bus with ground shielding, two types of repeaters are examined in this paper, namely repeaters with LVT short-channel ( $L = 40\text{nm}$ ) transistors and repeaters with LVT long-channel ( $L = 45\text{nm}$ ) transistors for leakage current suppression. Alternatively,



repeaters with LVT short-channel ( $L = 40\text{nm}$ ) transistors are used for the two data bus systems with encoding since ground gating technique is effective in suppressing the leakage currents produced by the LVT repeaters. The length of the data bus is assumed to be  $8\text{mm}$  [9]. LVT repeaters are inserted along the data bus for every other  $1095\mu\text{m}$ . 8 columns of repeaters are employed in each of the data bus. The layouts of the four data bus systems (including encoders and decoders) are drawn with Cadence Virtuoso. Post-layout SPICE simulations are performed to evaluate the different data bus systems. The delay and power consumptions of the encoders and decoders are included in the evaluation. The simulation temperature is  $90^\circ\text{C}$ .

For the 3-to-4 and 4-to-6 bus coding schemes, LVT transistors are used for the design of the encoders and decoders. High threshold voltage (HVT) NMOS transistors are used as footer sleep transistors for the encoders, decoders, as well as the repeaters of the 3-to-4 and 4-to-6 bus coding systems. The footer sleep transistors are sized to achieve lower than 10% speed overhead along the critical signal path with the 3-to-4 and 4-to-6 bus coding schemes as compared to the conventional short-channel-repeater-based ground-shielded data bus without any gating. The sleep transistor widths for each column of repeaters in the 3-to-4 and 4-to-6 bus coding systems are  $272\mu\text{m}$  and  $216\mu\text{m}$ , respectively. The total widths of sleep transistors that are used in the 3-to-4 and 4-to-6 data bus systems are  $2328\mu\text{m}$  and  $1912\mu\text{m}$ , respectively, including the sleep transistors used for encoders and decoders as well. The new 4-to-6 bus coding scheme therefore reduces the sleep transistor size by 17.87% compared to the 3-to-4 bus coding scheme. For the data bus with long channel repeaters, the channel widths of the repeaters are increased to achieve lower than 10% speed overhead along the critical signal path compared to the conventional data bus with short channel repeaters. The sizes of the long channel repeaters are ( $W = 52.8\mu\text{m}$ ,  $L = 45\text{nm}$ ) for PMOS transistors and ( $W = 26.4\mu\text{m}$ ,  $L = 45\text{nm}$ ) for NMOS transistors.

The huge LVT repeaters in the conventional data bus system with ground shielding consume significant leakage power, as listed in Table V. The leakage power consumption of all the data bus systems is the average when all the input data are “0” and “1”. While using repeaters with long channel transistors ( $L = 45\text{nm}$ ), the leakage power consumption of the data bus system is reduced by 49.01% as compared to the short-channel-repeater-based data bus with ground shielding. Alternatively, due to the utilization of sleep transistors, the leakage power consumption is reduced by ~99% with both 3-to-4 and 4-to-6 bus coding systems as compared to the conventional ground-shielded data bus system without any gating, no matter when short-channel repeaters are used or long-channel repeaters are used. Furthermore, the 4-to-6 bus coding system reduces the leakage power consumption by 12.5% as compared to the 3-to-4 bus coding system due to the smaller sleep transistors.

The operating frequency of data bus systems is assumed to be  $1\text{GHz}$  for the simulation of active power consumption. The highest active power is consumed when the number of switching bits is 42 and 32 on the coded bus of the 3-to-4 and 4-to-6 encoded data bus systems, respectively. The number of switching bits along the data bus is reduced by the 4-to-6 bus coding scheme compared with the 3-to-4 bus coding scheme. The 4-to-6 bus coding system thereby achieves 18.26% active power savings as compared to the 3-to-4 bus coding system under the worst-case switching scenarios. The long-channel-repeater-based data bus system with ground shielding consumes the highest worst-case active power among all the data bus systems that are evaluated in this paper primarily due to the larger repeater size. The worst-case active power consumption is increased by 30.74% by the long-channel-repeater-based data bus system with ground shielding as compared to the new 4-to-6 data bus system.

Exhaustive testing of the average active power consumption with the different data bus systems is infeasible. The average power consumption is related to the average switching probabilities of the data buses. By considering the code mapping that is listed in Table IV, the average number of switching activities in a 32-bit data bus system can be obtained by exhaustively counting the switching between any two codes (after coding). The new 4-to-6 bus coding achieves 9.24% reduction in terms of the average number of switching compared to the 3-to-4 coding scheme. 64 groups of random data patterns are applied to the four data bus

systems to evaluate the average active power consumption. As listed in Table V, the 4-to-6 bus coding system achieves 6.36% active power savings as compared to the 3-to-4 bus coding system with random data patterns.

With the newly proposed 4-to-6 data bus system, the number of ground shielding wires is reduced significantly as compared to the conventional data bus with ground shielding. The 4-to-6 data bus system therefore reduces the total number of global wires by 12.31% compared to the conventional data bus with ground shielding, thereby avoiding routing congestion in the physical design of highly complicated integrated circuits in advanced technology nodes. The total silicon area can also be reduced with lower routing congestion by the proposed 4-to-6 bus coding scheme.

In order to evaluate the overall performance of the different data bus systems, a comprehensive *Electrical Quality Metric (EQM)* is evaluated next. *EQM* is

$$EQM = \frac{1}{Delay \times P_{leakage} \times (P_{worst\_active} \times P_{average\_active})^{\frac{1}{2}} \times N_{wire}}, \quad (3)$$

where *Delay* is the critical signal path propagation delay.  $P_{leakage}$  is the leakage power consumption of different data bus systems.  $P_{worst\_active}$  and  $P_{average\_active}$  are the worst-case active power consumption and average active power consumption, respectively, of the data bus systems.  $N_{wire}$  is the total number of global interconnects on each data bus. The normalized *EQM* (with respect to the conventional short-channel-repeater-based data bus with ground shielding) is listed in Table V. The new 4-to-6 encoded data bus system achieves the highest *EQM*. The *EQM* is enhanced by 232.21x, 141.59x, and 23.06%, with the 4-to-6 encoded data bus system as compared to the conventional short-channel-repeater-based data bus with ground shielding, the long-channel-repeater-based data bus with ground shielding, and the 3-to-4 encoded data bus system, respectively.

## 5. CONCLUSIONS

A new 4-to-6 crosstalk-noise-aware bus coding scheme with ground-gated repeaters is proposed in this paper for robust low power data bus systems. The proposed crosstalk-noise-aware bus coding scheme reduces the number of global wires that are used in the system, avoiding routing congestion in the physical design of highly complicated integrated circuits. The new 4-to-6 bus coding scheme reduces the number of switching data bits in the system, thereby enabling 17.87% miniaturization of sleep transistors, 12.5% leakage power savings, 18.26% worst-case active power savings, and 6.36% average active power savings, as compared to the previously published 3-to-4 bus coding scheme. The 4-to-6 bus coding scheme also enhance the overall performance of the data bus system by 23.06% compared to the 3-to-4 bus coding scheme. The newly proposed crosstalk-noise-aware bus coding scheme therefore provides a robust and low power solution to on-chip data transmission in complex nanoscale CMOS integrated circuits.

## ACKNOWLEDGEMENT

This work was partially funded by European project CT217 RESIST.

## REFERENCES

1. B. Bowhill *et al.*, "The Xeon® processor E5-2600 v3: a 22 nm 18-core product family," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 1, pp. 92-104, January 2016.
2. S. Rusu *et al.*, "A 45 nm 8-core enterprise Xeon® processor," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 7-14, January 2010.
3. S. Rusu *et al.*, "A 65-nm dual-core multithreaded Xeon processor with 16-MB L3 cache," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 846-852, April 2007.

4. E. Salman, *Switching Noise and Timing Characteristics in Nanoscale Integrated Circuits*, Ph. D. Thesis, University of Rochester, 2009.
5. A. Vittal, L. H. Chen, M. Marek-Sadowska, K. Wang, and S. Yang, "Crosstalk in VLSI interconnections," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 12, pp. 1817-1824, December 1999.
6. V. Adler and E. G. Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 5, pp. 607-616, May 1998.
7. G. Chen and E. G. Friedman, "Low-power repeaters driving RC and RLC interconnects with delay and bandwidth constraints," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 2, pp. 161-172, February 2006.
8. H. Fatemi, B. Amelifard, and M. Pedram, "Power optimal MTCMOS repeater insertion for global buses," *Proceedings of the IEEE/ACM International Symposium on Low Power Electronics Design*, pp. 98-103, August 2007.
9. H. Singh, R. Rao, K. Agarwal, D. Sylvester, and R. Brown, "Dynamically pulsed MTCMOS with bus encoding for reduction of total power and crosstalk noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 1, pp. 166-170, January 2010.
10. B. Victor and K. Keutzer, "Bus encoding to prevent crosstalk delay," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 57-63, November 2001.
11. C. Duan, A. Tirumala, and S. Khatri, "Analysis and avoidance of cross-talk in on-chip buses," *Proceedings of the IEEE Symposium on High Performance Interconnects*, pp. 133-138, August 2001.
12. S. R. Sridhara, A. Ahmed, and N. R. Shanbhag, "Area and energy-efficient crosstalk avoidance codes for on-chip busses," *Proceedings of the IEEE International Conference on Computer Design*, pp. 12-17, October 2004.
13. P. Subramanya, R. Manimeghalai, V. Kamakoti, and M. Mutyam, "A bus encoding technique for power and cross-talk minimization," *Proceedings of the IEEE International Conference on VLSI Design*, pp. 443-448, January 2004.
14. M. Mutyam, "Fibonacci codes for crosstalk avoidance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 10, pp. 1899-1903, October 2012.
15. C.-G. Lyuh and T. Kim, "Low-power bus encoding with crosstalk delay elimination," *IEE Proceedings – Computers and Digital Techniques*, vol. 153, no. 2, pp. 93-100, March 2006.
16. C. Duan, V. H. Cordero, and S. P. Khatri, "Efficient on-chip crosstalk avoidance CODEC design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 4, pp. 551-560, April 2009.
17. X. Wu and Z. Yan, "Efficient CODEC designs for crosstalk avoidance codes based on numeral systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 4, pp. 548-558, April 2011.
18. S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V power supply high-speed digital circuit technology," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 8, pp. 847-854, August 1995.
19. H. Jiao and V. Kursun, "Ground-bouncing-noise-aware combinational MTCMOS circuits," *IEEE Transactions on Circuits and Systems I*, vol. 57, no. 8, pp. 2053-2065, August 2010.
20. H. Jiao and V. Kursun, "Reactivation noise suppression with sleep signal slew rate modulation in MTCMOS circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 3, pp. 533-545, March 2013.

TABLE I. Four Types of Switching Scenarios on Two Adjacent Wires [9]

| Type 1 | Type 2         | Type 3         | Type 4         |
|--------|----------------|----------------|----------------|
| (- -)  | (- ↑) or (- ↓) | (↑ ↑) or (↓ ↓) | (↑ ↓) or (↓ ↑) |

TABLE II. The Performance of n-bit Crosstalk-Noise-Aware Codewords

| $n$ (number of bits in a codeword) | $d_n$ (number of n-bit codewords in a neighbor set) | $k$ (max number of input bits that can be encoded) | Coding scheme | Max number of different bits in a neighbor set | Max number of different bits in 32-bit bus | Total number of wires used for a 32-bit bus |
|------------------------------------|---|--|---------------|--|--|---|
| 1                                  | 2   | 1  | 1-to-1        | 1  | 32   | 65  |
| 2                                  | 3   | 1  | 1-to-2        | 1  | 32   | 97  |
| 3                                  | 5   | 2  | 2-to-3        | 2  | 32   | 65  |
| 4                                  | 8   | 3  | 3-to-4        | 4  | 42   | 55  |
| 5                                  | 13  | 3  | 3-to-5        | 3  | 32   | 65  |
| 6                                  | 21  | 4  | 4-to-6        | 4  | 32   | 57  |
| 7                                  | 34  | 5  | 5-to-7        | 6  | 38   | 53  |
| 8                                  | 55  | 5  | 5-to-8        | 5  | 32   | 59  |
| 9                                  | 89  | 6  | 6-to-9        | 6  | 32   | 55  |
| 10                                 | 144   | 7  | 7-to-10       | 8  | 36   | 52  |
| 11                                 | 233   | 7  | 7-to-11       | 7  | 32   | 56  |
| 12                                 | 377   | 8  | 8-to-12       | 8  | 32   | 49  |

TABLE III. Crosstalk-Noise-Aware Codes with Different Coding Schemes

| Coding Scheme | Crosstalk-Noise-Aware Codes  |
|---------------|--|
| 3-to-4        | 0000, 0010, 0011, 1000, 1010, 1011, 1110, 1111   |
| 4-to-6        | 000010, 001000, 001010, 001011, 001110, 100000, 100010, 100011, 101000,<br>101010, 101011, 101110, 101111, 111010, 111011, 111110<br><b>(000000, 000011, 001111, 111000, 111111)</b> |

TABLE IV. Code Mapping for Crosstalk-Noise-Aware Coding Schemes

| 3-to-4 Coding | 4-to-6 Coding |               |
|---------------|---------------|---------------|
| 000 ↔ 1010    | 0000 ↔ 111110 | 1000 ↔ 000010 |
| 001 ↔ 1011    | 0001 ↔ 101000 | 1001 ↔ 001000 |
| 010 ↔ 1110    | 0010 ↔ 111010 | 1010 ↔ 001010 |
| 011 ↔ 1111    | 0011 ↔ 111011 | 1011 ↔ 001011 |
| 100 ↔ 0010    | 0100 ↔ 101110 | 1100 ↔ 001110 |
| 101 ↔ 0011    | 0101 ↔ 101010 | 1101 ↔ 100000 |
| 110 ↔ 0000    | 0110 ↔ 101111 | 1110 ↔ 100010 |
| 111 ↔ 1000    | 0111 ↔ 101011 | 1111 ↔ 100011 |

TABLE V. Characterization of Bus Coding Systems

|   | Conventional short-channel-repeater-based data bus with ground shielding [2] | Conventional long-channel-repeater-based data bus with ground shielding | 3-to-4 coding [9] | New 4-to-6 coding |
|---|--|---|-------------------|-------------------|
| Critical signal path propagation delay (ps) | 645  | 710   | 707               | 709               |
| Leakage power consumption ( $\mu$ W)        | 177.6  | 90.55   | 0.96              | 0.84              |
| Worst-case active power consumption (mW)    | 22.19  | 28.03   | 26.23             | 21.44             |
| Average active power consumption (mW)       | 15.58  | 17.42   | 16.51             | 15.46             |
| Total number of global wires                | 65   | 65  | 55                | 57                |
| <i>Electrical Quality Metric</i>            | 1  | 1.64  | 188.69            | 232.21            |