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Solar Energy Materials and Solar Cells 185 (2018) 385–391

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Investigation of crystalline silicon surface passivation by positively charged PO_x/Al_2O_3 stacks

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ARTICLE INFO

Keywords:
Surface passivation
Crystalline silicon
Solar cells
Atomic layer deposition

ABSTRACT

We investigate the passivation of crystalline Si (c-Si) surfaces by phosphorus oxide (PO_x) thin films deposited in an atomic layer deposition (ALD) reactor and capped in-situ by ALD Al_2O_3. Passivation is demonstrated on both *n*- and *p*-type (100) Si surfaces, and for PO_x/Al_2O_3 stacks deposited at both 25 °C and 100 °C. In contrast to Al_2O_3 alone, PO_x/Al_2O_3 passivation is activated already by annealing at temperatures as low as 250 °C in N_2 in all cases. Best results were obtained after annealing at 350 °C and 450 °C for films deposited at 25 °C and 100 °C respectively, with similar implied open-circuit voltages of 723 and 724 mV on *n*-type (100) Si. In the latter case an outstandingly low surface recombination velocity of 1.7 cm/s and saturation current density of 3.3 fA/cm^2 were obtained on 1.35 Ω cm material. Passivation of *p*-type Si appeared somewhat poorer, with surface recombination velocity of 13 cm/s on 2.54 Ω cm substrates. Passivation was found to be independent of PO_x film thickness for films of 4 nm and above, and was observed to be stable during prolonged annealing up to 500 °C. This excellent passivation performance on *n*-type Si is attributed partly to an unusually large *positive* fixed charge in the range of 3–5 × 10^{12} cm^{-2} (determined from capacitance–voltage measurements) for stacks deposited at both temperatures, which is significantly larger than that exhibited by existing positively charged passivation materials such as SiN_x. Indeed, passivation performance on *n*-type silicon is shown to compare favourably to state-of-the-art results reported for PECVD SiN_x. PO_x/Al_2O_3 stacks thus represent a highly effective positively charged passivation scheme for c-Si, with potential for *n*-type surface passivation and selective doping applications.

1. Introduction

Effective surface passivation has long been understood to be essential to realizing high-efficiency crystalline silicon (c-Si) solar cells, and has therefore been an important focus of research for many years. Although the materials and methods discovered thus far already enable outstanding passivation of c-Si surfaces, the exploration of new passivating materials remains of interest because these can have properties which make them advantageous for specific applications. This is especially the case as the range of functions a passivation layer is expected to perform continues to expand (particularly with the current interest in passivating contacts). Additionally, by understanding how different materials achieve passivation we deepen our understanding of passivation mechanisms in general.

In the last decade the list of materials known to be capable of passivating c-Si has expanded from the well-established Si-based compounds (SiO_2, SiN_x, and a-Si:H) to embrace a wide variety of newer materials [1], including Al_2O_3 [2], AlN [3], Ga_2O_3 [4], TiO_2 [5], Ta_2O_5 [6], HfO_2 [7], Nb_2O_5 [8], and ZnO [9]. Most of these new materials are metal oxides, and most feature a negative fixed charge at their interface with Si which makes them well-suited to passivating *p*-type Si surfaces, but less well-suited to passivating *n*-type surfaces. For the latter task SiN_x deposited by plasma-enhanced chemical vapour deposition (PECVD) [10], which has been known since the 1980s, remains the preferred solution, due partly to its relatively large positive charge, which has remained unmatched by newer passivation materials.

We have recently demonstrated unprecedentedly effective passivation of InP surfaces using a non-metal oxide, namely phosphorus oxide (PO_x), capped by Al_2O_3 [11]. In this structure, the Al_2O_3 capping layer acts as a moisture barrier to provide chemical stability to the PO_x, which is known to be highly hygroscopic, and therefore unstable when exposed to atmospheric moisture (uncapped PO_x films were observed to undergo rapid visible degradation on exposure to atmosphere). These PO_x films are amorphous and highly transparent, with a wide bandgap (> 5 eV) and a refractive index of 1.66–1.67 at 632 nm, which makes them well-suited to solar cell applications.

As we have recently reported [12], such PO_x/Al_2O_3 stacks can also provide highly effective surface passivation of c-Si. In particular, they

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https://doi.org/10.1016/j.solmat.2018.05.007
Received 15 March 2018; Received in revised form 30 April 2018; Accepted 4 May 2018

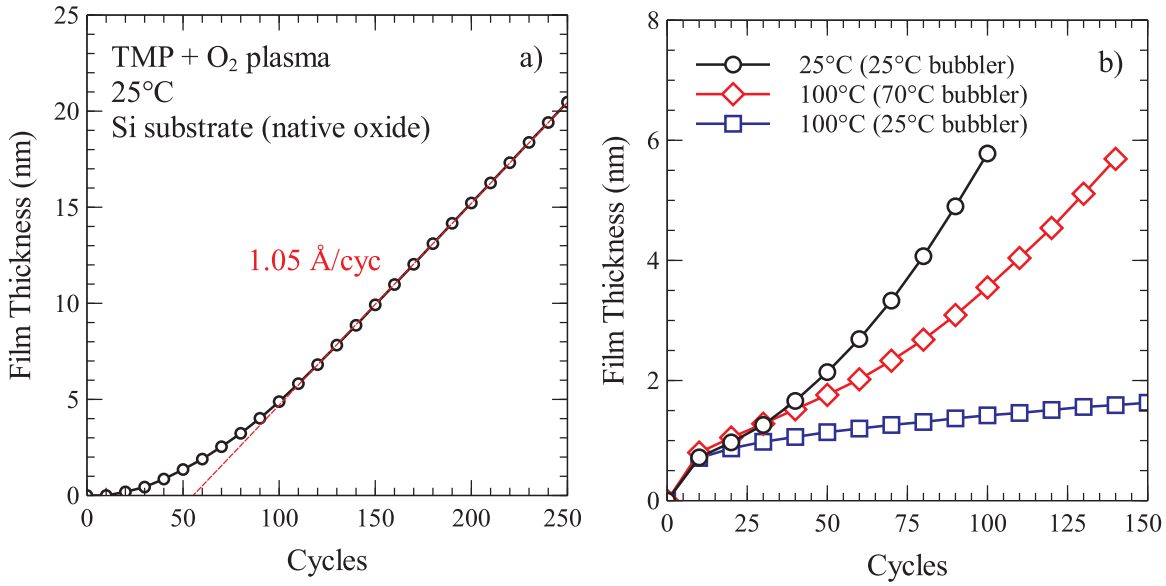

Fig. 1. Film thickness vs number of deposition cycles for PO_x films deposited a) at 25 °C on a polished (100) Si substrate with a native oxide (25 °C bubbler temperature), and b) at 25 or 100 °C on HF-etched, polished (100) Si substrates (for bubbler temperatures of 25 °C and 70 °C). The TMP dose time was 500 ms in all cases (with a 10 s hold step).

provide outstanding passivation of *n*-type surfaces due to their unusually large positive charge. In this work we explore the passivation of these stacks in more detail. We report passivation results for PO_x/Al_2O_3 deposited at both 25 and 100 °C, and on both *n*- and *p*-type Si, and examine the influence of PO_x film thickness and annealing time. We show that PO_x/Al_2O_3 occupies a unique position among existing passivation schemes due to its unmatched positive charge, and compare PO_x/Al_2O_3 passivation performance to state-of-the-art results for PECVD SiN_x.

2. Experimental details

PO_x films were deposited at temperatures of 25 and 100 °C in an Oxford Instruments FlexAL atomic layer deposition (ALD) reactor by exposing samples alternately to trimethyl phosphate (TMP, $(CH_3)_3PO_4$) and an O_2 plasma in a cyclic fashion, with separating Ar purges. Fig. 1a shows the resulting PO_x film thickness measured by in-situ spectroscopic ellipsometry as a function of the number of cycles at 25 °C, which exhibited a linear behaviour following an initial nucleation delay when deposited on Si surfaces with a native oxide (similar behaviour was observed at 100 °C). The steady-state growth-per-cycle (GPC) was not observed to saturate with respect to the TMP dose time, so that this process should be considered as pulsed chemical vapour deposition rather than ALD. On HF-etched surfaces the growth of a thin (~1 nm) interfacial oxide due to O_2 plasma exposure was apparent in the first cycles (Fig. 1b), after which deposition proceeded as on surfaces with a native oxide. ALD Al_2O_3 capping layers were deposited in-situ at the same temperature from trimethyl aluminium (TMA, $Al(CH_3)_3$) and O_2 plasma. The deposited film thickness was 5–6 nm for the PO_x and 14–15 nm for the Al_2O_3, unless stated otherwise.

Symmetric lifetime test structures with PO_x/Al_2O_3 stacks (where the PO_x was deposited first) or Al_2O_3 only were fabricated on 280 µm thick double-side-polished float-zone (100) 1–5 Ω cm *n*- and *p*-type Si wafers, which received a standard RCA clean and HF dip immediately prior to PO_x/Al_2O_3 or Al_2O_3 deposition. Post-deposition annealing was performed in a Jipelec rapid thermal processing system in N_2. Lifetime measurements were performed using a Sinton WCT 120TS photoconductance lifetime tester. The surface saturation current density J_{0s} was determined using the method of Kane and Swanson [13], assuming an intrinsic bulk lifetime given by the model of Richter et al. [14] and an intrinsic carrier concentration $n_i = 8.6 \times 10^9$ cm^{-3} (from the expression of [15] at 25 °C). The upper limit of the effective surface recombination velocity $S_{eff,UL}$ was calculated using the same intrinsic lifetime model [14].

3. Results and discussion

Fig. 2a shows the measured effective excess carrier lifetime τ_{eff} at an excess carrier concentration Δn of 10^{15} cm^{-3} as a function of post-deposition annealing temperature for *n*-type wafers passivated by PO_x/Al_2O_3 stacks or Al_2O_3 films deposited at 25 °C, and annealed consecutively at a series of increasing temperatures for 10 min in N_2. A deposition temperature of 25 °C was chosen for the initial investigations because it is the same as that previously used in the case of InP [1]. The initial lifetime results are quite encouraging, with a peak lifetime of 1.9 ms obtained for the PO_x/Al_2O_3-passivated sample after annealing at 350 °C, corresponding to $S_{eff,UL}$ of 6.8 cm/s. Perhaps more strikingly, the passivation of the PO_x/Al_2O_3 stacks appears to be activated at significantly lower annealing temperatures than in the case of Al_2O_3, with a lifetime of 1.2 ms obtained already after annealing at 250 °C. This clearly shows that the observed passivation is not simply due to the Al_2O_3 capping layer, and suggests that the Si–PO_x surface passivation kinetics are fundamentally dissimilar from those of Si–Al_2O_3.

Closer examination of the injection-dependent lifetime data (Fig. 2b) reveals significant changes in lifetime injection dependence with annealing. The lifetime after annealing at 250 °C is well-described by a single-diode model, with a surface saturation current density J_{0s} of 49 fA/cm^2 per side, suggesting that the surface is strongly accumulated or inverted due to charge in the dielectric stack. Following annealing at higher temperatures the lifetime simultaneously increases in high injection, while decreasing in low injection, such that the surface recombination can no longer be adequately parameterized by J_{0s}. The reason for this is not clear, but may be related to the large hysteresis observed in capacitance–voltage measurements of the same stacks, as discussed later. Interestingly however, the lifetime measured after annealing at 350 °C approaches very close to the intrinsic limit in high injection, which is reflected in an exceptionally high 1-Sun implied open-circuit voltage of 723 mV at 25 °C, and already indicates the exceptional passivation potential of these stacks.

Even better passivation results were obtained for PO_x/Al_2O_3 stacks

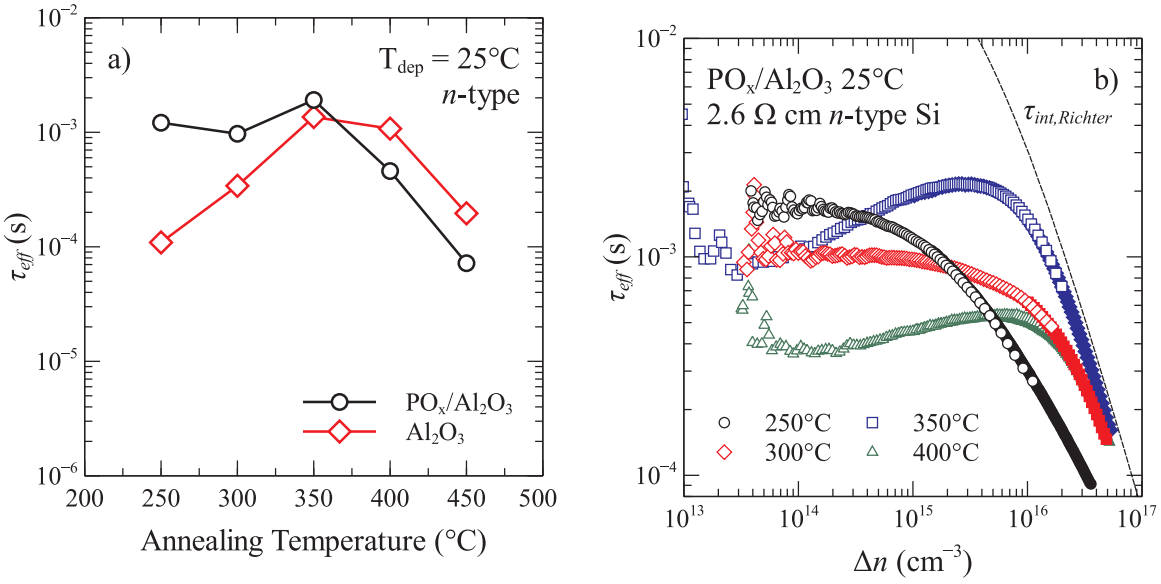

Fig. 2. a) Effective excess carrier lifetime τ_{eff} ($\Delta n = 10^{15}$ cm^{-3}) vs annealing temperature for 2.6 Ω cm *n*-type FZ Si (100) wafers passivated by PO_x/Al_2O_3 stacks deposited at 25 °C, and by the same Al_2O_3 films without PO_x. Annealing was performed consecutively for 10 min at each temperature in N_2. b) Corresponding τ_{eff} vs excess carrier concentration Δn at several annealing temperatures for the PO_x/Al_2O_3-passivated samples. Open (closed) symbols correspond to transient (quasi-steady-state) measurements. The dashed line shows the intrinsic Si lifetime τ_{int} as parameterised by Richter et al. [14].

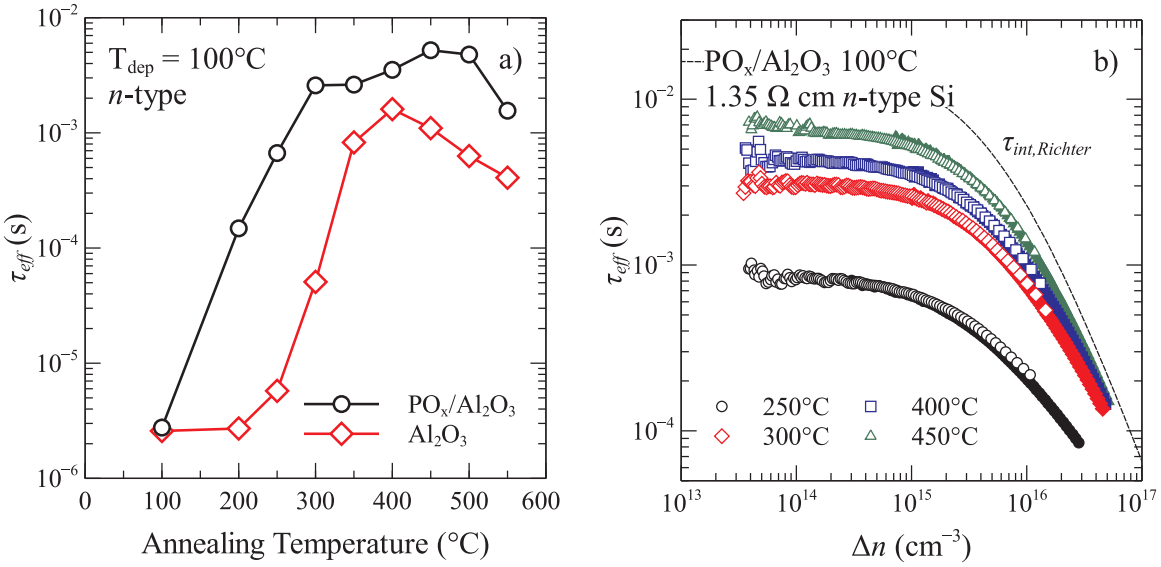

Fig. 3. a) Effective excess carrier lifetime τ_{eff} ($\Delta n = 10^{15}$ cm^{-3}) vs annealing temperature for 1.35 Ω cm *n*-type FZ Si (100) wafers passivated by PO_x/Al_2O_3 stacks deposited at 100 °C, and by the same Al_2O_3 films without PO_x. Annealing was performed consecutively for 10 min at each temperature in N_2. b) Effective excess carrier lifetime τ_{eff} vs excess carrier concentration Δn corresponding to the data of a) for PO_x/Al_2O_3 stacks annealed at the indicated temperatures. Open (closed) symbols correspond to transient (quasi-steady-state) measurements. Dashed lines show the intrinsic Si lifetime τ_{int} as parameterised by Richter et al. [14]. Adapted from [12] with the permission of AIP Publishing.

deposited at 100 °C. Figs. 3a and 4a again show lifetime as a function of annealing temperature, this time for *n*- and *p*-type substrates respectively passivated by PO_x/Al_2O_3 stacks and Al_2O_3 films deposited at 100 °C. Qualitatively similar trends are observed as for the samples passivated at 25 °C. Also in this case, activation of surface passivation is observed following annealing at significantly lower temperatures than for the samples with Al_2O_3 alone, with lifetimes already approaching 1 ms after annealing for 10 min at 250 °C. Again, the PO_x/Al_2O_3-passivated samples demonstrate excellent passivation, comparable to or better than the plasma-ALD-Al_2O_3-passivated control samples (it should be noted that this deposition temperature is not optimal for Al_2O_3 passivation [16]). In particular, for the *n*-type sample we obtain a peak lifetime of 5.1 ms following annealing at 450 °C. This corresponds to an exceptionally low effective surface recombination velocity $S_{eff,UL}$ of 1.7 cm/s. In the case of the *p*-type samples a less impressive but still reasonably low minimum $S_{eff,UL}$ of 13 cm/s (lifetime of 1 ms) is obtained after annealing at 300 °C. The higher deposition temperature also appears to improve thermal stability. While the passivation of the 25 °C PO_x/Al_2O_3 was observed to degrade already on annealing at 400 °C, the passivation of stacks deposited at 100 °C degraded significantly only at 550 °C.

This excellent passivation performance is reflected in the injection-dependence of the lifetime, shown in Figs. 3b and 4b. For the PO_x/Al_2O_3 stacks deposited at 100 °C on *n*-type Si we observe single-diode behaviour at all annealing temperatures, suggesting uniform passivation and strong accumulation or inversion of the surface. Using the

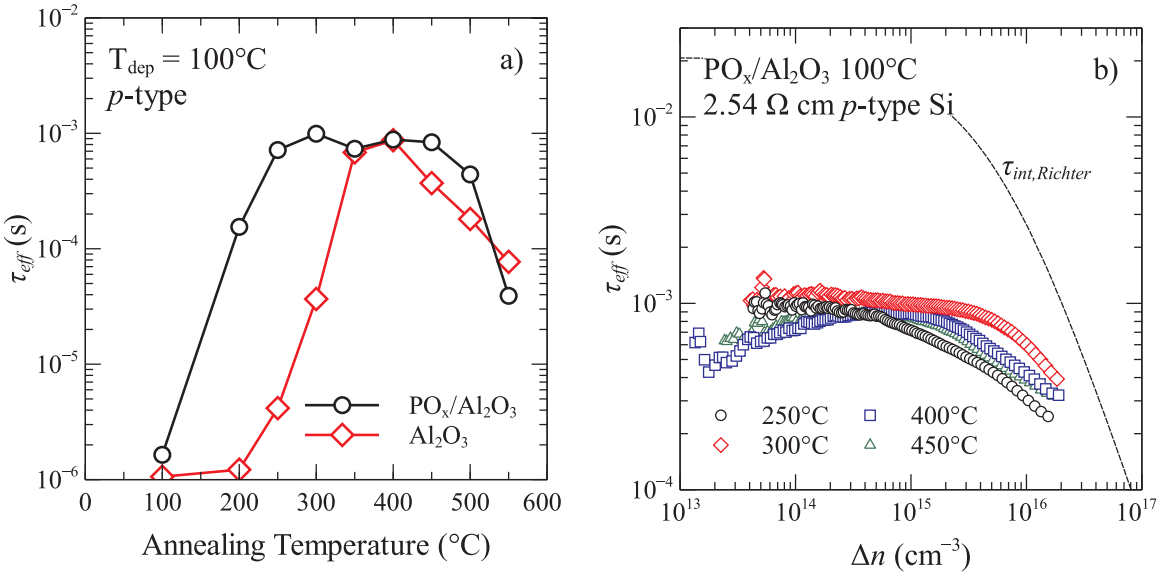

Fig. 4. a) Effective excess carrier lifetime τ_{eff} ($\Delta n = 10^{15}$ cm^{-3}) vs annealing temperature for 2.5 Ω cm *p*-type FZ Si (100) wafers passivated by PO_x/Al_2O_3 stacks deposited at 100 °C, and by the same Al_2O_3 films without PO_x. Annealing was performed consecutively for 10 min at each temperature in N_2. b) Effective excess carrier lifetime τ_{eff} vs excess carrier concentration Δn corresponding to the data of a) for PO_x/Al_2O_3 stacks annealed at the indicated temperatures. Open (closed) symbols correspond to transient (quasi-steady-state) measurements. Dashed lines show the intrinsic Si lifetime τ_{int} as parameterised by Richter et al. [14].

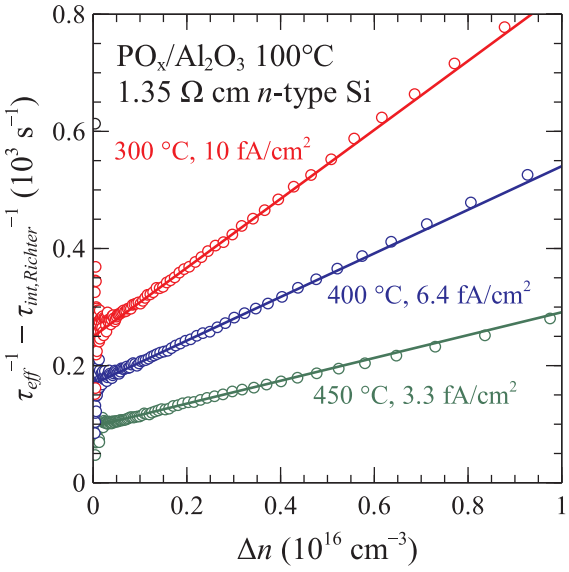

Fig. 5. Auger-corrected inverse effective lifetime τ_{eff} vs excess carrier concentration Δn corresponding to the data of Fig. 4a for an *n*-type FZ Si (100) wafer passivated by PO_x/Al_2O_3 deposited at 100 °C, after annealing at the indicated temperatures. Measurements were performed in transient mode. Lines show linear fits to the data in the range of Δn = 1–5 × 10^{15} cm^{-3}, which were used to extract J_{0s} via the method of Kane and Swanson [13]. The resulting values of J_{0s} are given.

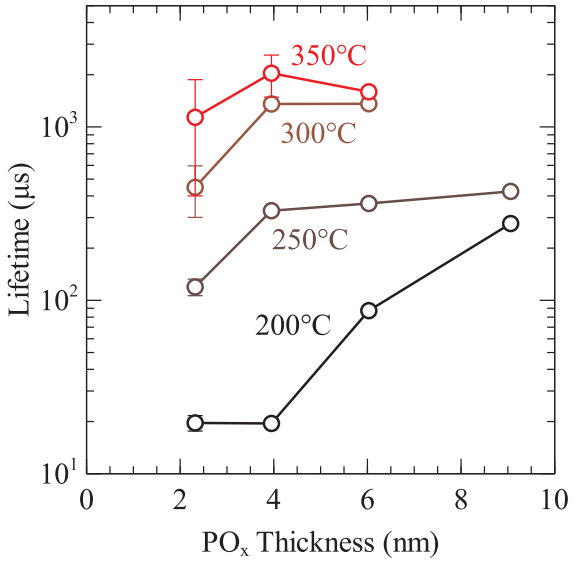

Fig. 6. Excess carrier lifetime τ_{eff} ($\Delta n = 10^{15}$ cm^{-3}) vs PO_x film thickness for *n*-type Si (100) wafers passivated by PO_x/Al_2O_3 stacks deposited at 100 °C, after annealing at various temperatures. Error bars show the spread between measurements of two identically processed samples (in most cases this spread is smaller than the symbol size). Annealing was performed consecutively for 10 min at each temperature in N_2, starting at the lowest temperature. The Al_2O_3 thickness was the same (~14 nm) in each case. The stacks with the thickest (~9 nm) PO_x films exhibited significant blistering and a corresponding drop in lifetime following annealing at 300 °C, therefore we do not include this data in the figure.

method of Kane and Swanson [13], we extract values of 52, 10.5, 6.4, and 3.3 fA/cm^2 for J_{0s} following annealing at 300, 400, and 450 °C respectively (Fig. 5). The latter value of 3.3 fA/cm^2 is exceptionally low, and represents an outstanding level of silicon surface passivation. The corresponding 1-Sun implied open circuit voltage of this sample was calculated as 724 mV at 25 °C. In contrast the injection-dependence for the *p*-type sample is less well-behaved, and appears to show a dip in low injection at higher temperatures. The better performance on *n*-type surfaces, and the fact that no decrease in lifetime in low injection is observed in this case, already hints at a positive fixed charge for the PO_x/Al_2O_3 stack, as will be discussed below.

The passivation does not appear to be overly sensitive to PO_x film thickness. As shown in Fig. 6, lifetime improved only slightly with PO_x thickness for thicknesses of 4 nm and above on annealing at 250 °C. Thicker films (> 9 nm) however exhibited significant blistering on annealing at temperatures of 300 °C or above, with consequent loss of passivation. We speculate that this may be due to density changes occurring in the PO_x around 300 °C (suggested by changes in the refractive index after annealing at this temperature) resulting in significant strain mismatch within the PO_x/Al_2O_3 stack. Therefore, a PO_x

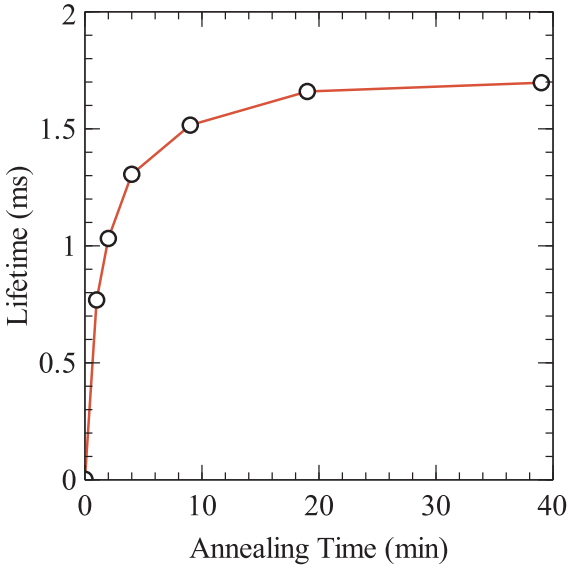

Fig. 7. Excess carrier lifetime τ_{eff} ($\Delta n = 10^{15}$ cm^{-3}) as a function of cumulative annealing time at 300 °C in N_2 for an *n*-type Si (100) wafer passivated by PO_x/Al_2O_3 deposited at 100 °C.

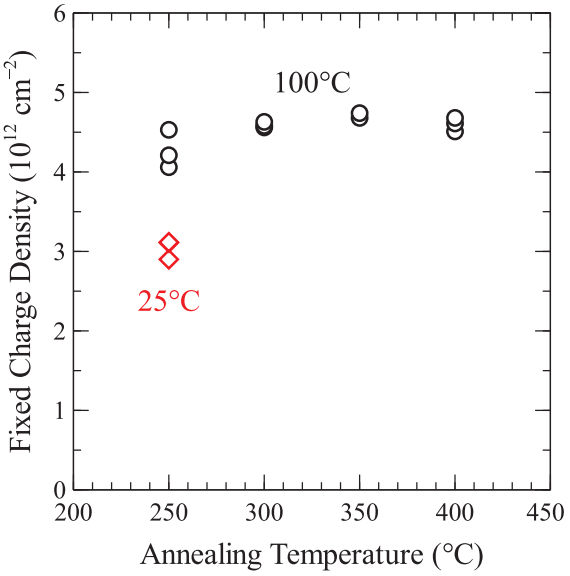

Fig. 8. Fixed charge density determined by high-frequency capacitance–voltage measurements for PO_x/Al_2O_3 stacks deposited on *n*-type silicon at 100 °C and 25 °C as a function of annealing temperature (annealing was performed prior to metallisation for 10 min in N_2).

thickness of around 4–6 nm appears preferable.

Although the primary function of the Al_2O_3 capping layer is to provide chemical stability to the PO_x, it is likely that it also plays a role in the passivation by acting as both a source and diffusion barrier for hydrogen, thereby providing improved hydrogenation of the Si–PO_x interface. Al_2O_3 is well-known to play such a role in other passivating stacks [1]. This might account for the way that lifetime first appears to saturate at 300–350 °C in Fig. 3 before increasing again at 400 °C, since the latter temperature is generally observed to be the threshold for hydrogenation from Al_2O_3. Fig. 7 shows that lifetime saturates already after 20 min when annealing a similar stack at a fixed temperature of 300 °C, at which no significant hydrogenation from the Al_2O_3 is expected, which suggests the increased lifetime at 450 °C is not simply due to the longer duration of annealing 7.

In order to verify the polarity and magnitude of the fixed charge in the PO_x/Al_2O_3 stack, we performed high-frequency (1 MHz) capacitance–voltage measurements on *n*-type metal–insulator–semiconductor (MIS) structures with PO_x/Al_2O_3 stacks deposited at either 100 °C or 25 °C and annealed at various temperatures (the C–V data for the stacks deposited at 100 °C is presented in [12]). Fig. 8 shows the extracted fixed charge density as a function of annealing temperature, which is calculated from the measured flatband voltage assuming all charge to be located at the Si–PO_x interface. These measurements confirm that the PO_x/Al_2O_3 stacks indeed possess an unusually large positive fixed charge. Values of 4.1–4.5 × 10^{12} cm^{-2} are observed for the stacks deposited at 100 °C already after annealing at 250 °C, rising to 4.5–4.7 × 10^{12} cm^{-2}, essentially independent of annealing temperature, for films annealed between 300 °C and 400 °C. Slightly lower values of 2.9–3.1 × 10^{12} cm^{-2} are obtained for the stacks deposited at 25 °C after annealing at 250 °C. We also examined the same 25 °C stacks annealed at 350 °C, however these showed large hysteresis which precluded the measurement of useable C–V curves. It is possible that the unusual lifetime injection dependence observed for the same stacks (Fig. 2) is related to this hysteresis.

The large positive charge of PO_x/Al_2O_3 makes it exceptional among more recent passivation materials. Most new passivation materials for c-Si reported in the last two decades have been strongly negatively charged. This includes Al_2O_3 [2], AlN [3], Ga_2O_3 [4], TiO_2 [5], Ta_2O_5 [6], and Nb_2O_5 [8]. HfO_2 is a partial exception for which both negative and positive Q_f have been reported [7]. The other existing positively charged passivation layers are the long-known SiO_2 and SiN_x. The concentration of positive charge we observe for our PO_x/Al_2O_3 stacks is significantly larger than typically obtained for either of these materials. SiO_2 is only weakly positively charged, with Q_f usually below 5 × 10^{11} cm^{-2} on (100) surfaces. Q_f in SiN_x can be much larger, even up to 5 × 10^{12} cm^{-2} and above [18], but the concentrations reported for SiN_x films which show good surface passivation are typically somewhat smaller, in the range of 3 × 10^{11} to 2 × 10^{12} cm^{-2} [18–21]. For example, in the extensive parametric study of Wan *et al.*, which resulted in some of the best-passivating SiN_x to date, Q_f was found to vary only from 3 × 10^{11} cm^{-2} to just over 1 × 10^{12} cm^{-2} when varying the process parameters over a wide range around stoichiometric conditions [21].

Fig. 9 shows a visual comparison of the different silicon passivation schemes in terms of D_{it} and Q_f. The position of PO_x/Al_2O_3 is indicated based on the data of this work. While we have not yet measured D_{it} directly (the system which we used was not capable of performing quasi-static C–V measurements), it may be inferred to be on the order of 10^{10} eV^{-1} cm^{-2} based on the extremely low surface recombination rates measured, as well as from a comparison of the parallel conductance peaks also measured by C–V with those for Al_2O_3 [12]. This figure illustrates clearly the unique position occupied by PO_x/Al_2O_3 as a strongly positively charged passivation layer for c-Si, which makes it particularly interesting for passivation of *n*-type Si surfaces.

In light of this, it is also interesting to compare the passivation we achieve with PO_x/Al_2O_3 with the best results reported for PECVD SiN_x, which is the established passivation material of choice for *n*-type surfaces. In Fig. 10 we summarise the best passivation results reported in the literature [14,21–25] for SiN_x on *n*-type Si in terms of surface recombination velocity $S_{eff,max}$ calculated assuming an infinite bulk lifetime as a function of dopant concentration (we choose to assume an infinite lifetime in this case because $S_{eff,UL}$ calculated using the intrinsic lifetime model of Richter et al. [14] would result in negative values for some more heavily doped samples [24]). It should be noted that both the results of Richter et al. [14] and the lowest $S_{eff,max}$ values of Chen et al.[23] and Duttagupta et al. [25] are for Si-rich SiN_x, with compositions intermediate between stoichiometric Si_3N_4 and hydrogenated amorphous silicon (a-Si:H). While somewhat better passivation has been reported for such films, they also tend to be both less transparent and less thermally stable [23,25] (like a-Si:H), and are less representative of the SiN_x layers usually employed in commercial silicon

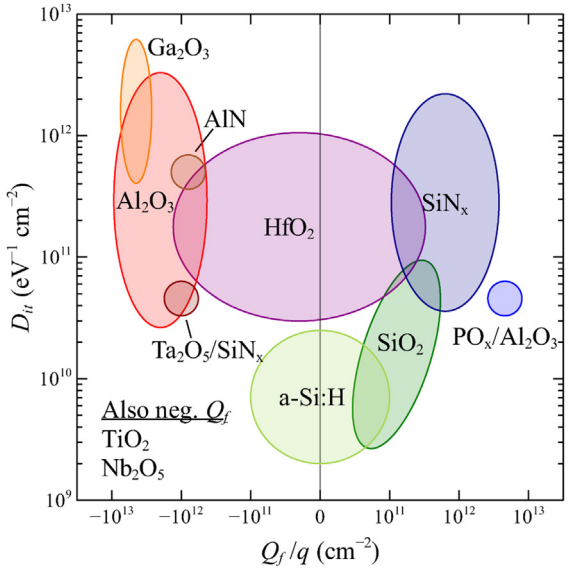

Fig. 9. Schematic comparison of different c-Si surface passivation materials and stacks in terms of interface state density D_{it} and fixed charge Q_f. Adapted with modifications from Cuevas et al. [17]. The approximate position of PO_x/Al_2O_3 is indicated. Additional passivation materials for which the charge polarity is known to be negative, but for which the magnitude of both D_{it} and Q_f has not been reported (TiO_2 [5], Nb_2O_5 [8]), are noted.

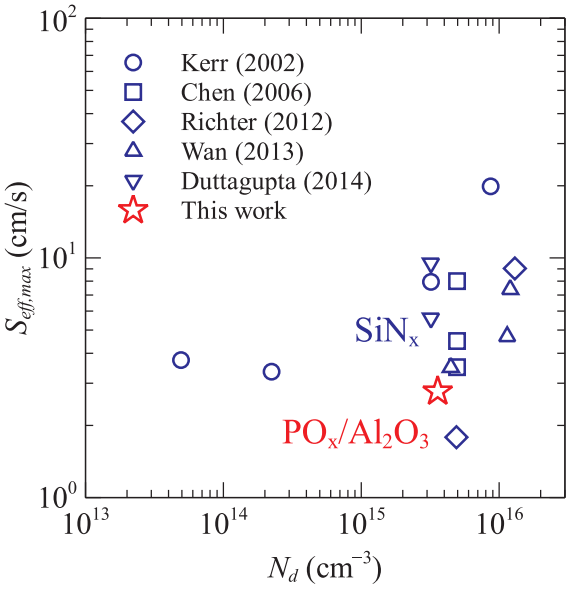

Fig. 10. Summary of $S_{eff,max}$ at $\Delta n = 10^{15}$ cm^{-3} reported in the literature [14,21–25] as exemplary values for PECVD SiN_x on *n*-type silicon as a function of dopant concentration N_d. Our best result for PO_x/Al_2O_3 (deposited at 100 °C and annealed up to 450 °C in N_2) is included for comparison.

solar cells. Regardless, it is clear from this comparison that PO_x/Al_2O_3 already provides passivation of *n*-type Si comparable to or better than state-of-the-art PECVD SiN_x.

Given that the PO_x contains large quantities of phosphorus, which is the standard *n*-type dopant in c-Si, passivation stacks including PO_x may also have the potential to be used as phosphorus sources for selective doping applications (i.e. laser doping), as already demonstrated with e.g. P-doped SiO_2 and phosphosilicate glass (PSG) [26]. The advantage of using PO_x in this case is that it could simultaneously act as a passivation layer for the non-doped areas, allowing a simplified self-aligned process flow for passivation and contacting. Of course in this application it might be desirable to replace the Al_2O_3 capping layer by another material, since Al is a *p*-type dopant in Si and might compensate the P-doping from the PO_x. In principle it would be possible to replace the Al_2O_3 with another material capable of acting as a moisture barrier, such as SiNx, SiO_2, or TiO_2. The latter two materials could also function as anti-reflection coatings for PO_x deposited as a front-side passivation layer. The integration of PO_x with such alternative capping layers will be the subject of future investigation.

4. Conclusions

We have demonstrated excellent levels of c-Si surface passivation with PO_x/Al_2O_3 stacks deposited at both 25 and 100 °C on *n*- and *p*-type (100) Si surfaces. Significant passivation is observed already on annealing at temperatures as low as 250 °C in N_2, while best results are obtained after annealing at 350 °C and 450 °C for films deposited at 25 and 100 °C respectively, with similarly high implied open circuit voltages of 723 and 724 mV. Films deposited at 100 °C however show better performance at lower injection levels, with an effective surface recombination velocity $S_{eff,UL}$ as low as 1.7 cm/s and J_{0s} of 3.3 fA/cm^2 obtained on 1.35 Ω cm *n*-type (100) Si, and $S_{eff,UL}$ of 13 cm/s on 2.54 Ω cm *p*-type Si. Passivation is shown to be essentially independent of PO_x thickness above 4 nm, though blistering is an issue for thicker films (> 9 nm) annealed above 300 °C. PO_x/Al_2O_3 stacks deposited at both temperatures exhibit an unusually large positive charge in the range of 3–5 × 10^{12} cm^{-2} which results in excellent passivation of *n*-type Si surfaces. The obtained passivation levels are shown to be comparable to those for state-of-the-art PECVD SiN_x, demonstrating the outstanding passivation potential of such stacks.

Acknowledgements

The authors thank B.W.H. van de Loo, B. Macco, J. Melskens, and M.A. Verheijen for useful discussions and feedback, C.A.A. van Helvoirt and J. van Gerwen for technical support, and H.W. van Zeijl for assistance with the C–V measurements. Al contact evaporation and C–V measurements were performed at the Delft University of Technology. The authors acknowledge financial support for this research from the Top consortia for Knowledge and Innovation (TKI) Solar Energy programs "COMPASS" (TEID215022) and "RADAR" (TEUE116905) of the Ministry of Economic Affairs of the Netherlands.

Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.solmat.2018.05.007.

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