Dimmable integrated CMOS LED driver based on a resonant DC/DC hybrid-switched capacitor converter


DOI: 10.1002/cta.2512

Document status and date:
Published: 01/08/2018

Document Version:
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher’s website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the “Taverne” license above, please follow below link for the End User Agreement:
www.tue.nl/taverne

Take down policy
If you believe that this document breaches copyright please contact us at:
openaccess@tue.nl
providing details and we will investigate your claim.

Download date: 16. Aug. 2019
Dimmable integrated CMOS LED driver based on a resonant DC/DC hybrid-switched capacitor converter

Juan C. Castellanos¹ | M. Turhan¹ | Marcel A.M. Hendrix¹,² | Arthur van Roermund¹ | Eugenio Cantatore¹

¹ Eindhoven University of Technology, Eindhoven, The Netherlands
² Philips Lighting Research, Eindhoven, The Netherlands

Correspondence
Juan Castellanos, Eindhoven University of Technology, Eindhoven, The Netherlands. Email: j.castellanos@tue.nl

Funding information
The Netherlands Organisation for Scientific Research Domain TTW former Stichting voor de Technische Wetenschappen (STW), Grant/Award Number: 12759

Summary
This paper presents a 7.7-mm² on-chip LED driver based on a DC/DC resonant hybrid-switched capacitor converter operating in the MHz range with and without output capacitor. The converter operation allows continuously dimming the LED while keeping control on both peak and average current. Also, it features no flickering even in the absence of output capacitor and for light dimmed down to 10% of the nominal value. The capacitors and switches of the LED driver are integrated on a single IC die fabricated in a low-cost 5 V 0.18-µm bulk CMOS technology. This LED driver uses a small (0.7 mm²) inductor of 100 nH, which is 10 times smaller value than prior art integrated inductive LED drivers, still showing a competitive peak efficiency of 93% and achieving a power density of 0.26 W/mm² (0.34 W/mm³).

KEYWORDS
CMOS integrated circuit, DC-DC power converters, dimmable LED driver, light-emitting diodes, switching converters, zero-current switching (ZCS)

1 | INTRODUCTION

Light-emitting diodes (LEDS) have reached competitive light output efficiency when compared to conventional lighting sources.¹ Special drivers are required to operate these solid-state lighting sources. Their goal is to control the DC current of the LEDs (thus adjusting the light emission, ie, dimming the LED) and bridge the difference between input voltage and LED voltage, using high-efficiency conversion techniques. Efficiency and dimming are not the only requirements that LED drivers have to accomplish. Issues like thermal management,² color stability,² flickering,³ and limited space in the luminaries, as well as demand for high reliability and embedded communication, make it increasingly more interesting to implement LED drivers using integrated circuit (IC) or system-in-package integration. A smart LED driver IC can provide a low-cost and compact form factor solution which embeds CMOS-based intelligence. This last feature can be used for calibration and compensation,⁴ on-chip measurements together with sensors (eg, to monitor light quality), and communication ability (eg, for internet-of-things applications). Additionally, IC integration can be exploited to reduce the number of external components, as will be demonstrated in this paper by eliminating the output capacitor.

This is an open access article under the terms of the Creative Commons Attribution-NonCommercial-NoDerivs License, which permits use and distribution in any medium, provided the original work is properly cited, the use is non-commercial and no modifications or adaptations are made.

© 2018 The Authors. International Journal of Circuit Theory & Applications Published by John Wiley & Sons Ltd
Nevertheless, keeping a competitive power efficiency while scaling the size of the LED driver components to enable IC or SiP integration is challenging.

Three converter topologies are widely used by commercial LED drivers: linear regulators, inductive converters, and switched capacitor converters.

Linear regulators and constant current regulators are suitable for IC integration; however, they have poor efficiency. Examples of integrated LED modules using linear drivers can be found in Lin and Chen and de Samber et al.

Inductive switching converters are the most common topology used in high-efficiency LED drivers. In off-line applications, these converters are attractive because of their simplicity, low number of components, and inductive isolation, e.g., Flyback-based LED driver. In most cases, resonant topologies using soft switching are chosen because of their better efficiency, even in DC-supplied LED drivers. However, inductive converters use high-quality and large-power inductors, which are expensive components in size and price. Moreover, large inductors with low DC resistances cannot be easily integrated on-chip, as demonstrated by Fang et al, Wang et al, and Villar and Alarcon which show examples of small on-chip inductors using nonconventional CMOS process or bond wires of 5.2 μH, 390 nH, and 26.73 nH with DC resistances of 2.3, 0.14, and 1.08 Ω respectively. Therefore, new topologies enabling reduced inductor size are required to place the inductor on a compact package or even on-chip.

Switched capacitor converters (SCCs) are widely used in fully integrated switching power supplies. However, they suffer from charge transfer losses between the capacitors and linear losses when the voltage conversion ratio deviates from the nominal value determined by the specific topology.

New topologies using hybrid switched capacitor converters (H-SCCs) have been proposed to improve the performance of the SCCs and enable the miniaturization of inductive converters. In H-SCC, charge transfer losses are reduced using soft charging of the capacitors. Pilawa-Podgurski et al proposed a 2-stage topology where a SCC operates at low frequency using high-voltage switches, and an inductive stage using low-voltage switches operates at higher frequency. A more compact converter is proposed by Lei and Pilawa-Podgurski, where a Dickson switched capacitor (SC) topology is operated together with an inductor to achieve resonance. However, soft switching is not achieved in this converter because of the interconnections among the flying capacitors, and the efficiency is decreased by the hard switching operation. The discrete resonant SC converter in Martins et al uses a variable inductor to control the peak current in resonance; however, it still uses large passives. The on-chip resonant SC converter proposed in Kesarwani et al makes use of soft switching (zero-current switching (ZCS)), resulting in a more compact and efficient solution. Nevertheless, the voltage regulation strategy used in this reference (dynamic off-time modulation) only allows the converter to reduce the output voltage below its nominal value. Turhan et al proposed a control strategy which maintains ZCS and makes possible to increase the nominal SC output voltage, adding 1 active switch. This discrete implementation uses 5 switches in total (3 active and 2 passive—implemented with diodes) and operates at 50 kHz.

This paper proposes a compact and high-efficiency dimmable LED driver, which exploits a DC/DC resonant H-SCC built with 1 SC cell implemented in a CMOS 0.18-μm IC and using a small 0.7 mm² 100 nH discrete inductor. The on-chip converter topology here discussed takes inspiration from the discrete implementation, but focuses on miniaturizing the LED driver, to obtain a mid and low-power LED driver with miniature size. Small size can be extremely useful in applications such as LED torches, camera lights, and alike. Exploiting IC integration of the switches and flying capacitor, compared to Turhan et al the operation frequency is increased to 3.5 MHz and the flying capacitor is decreased from 670 to 16 nF and the inductor from 5 μH to 100 nH. The input voltage is decreased from 45 to 5 V and the output power from 45 to 2 W. The final LED driver volume is only 6 mm³, while the sole inductor in Turhan et al has a volume of about 380 mm³. Also, compared to Turhan et al, active switchless is used, and analog IC circuitry is integrated with the power train to create the supply voltage needed to drive the power switches and replace the discrete diodes with on-chip metal-oxide-semiconductor field-effect transistors. Additionally, it is shown that the output capacitor of the converter can be eliminated, while avoiding flicker even when the light is dimmed to 10% of the nominal value. The driver exploits a 3-phase control, called quasi-resonant operation able to bridge higher and lower LED voltages with respect to the base SC conversion ratio (2:1). Section 2 describes the topology and operation principle. Section 3 presents the design considerations, including modeling, minimization of the losses, choice of the inductor and flying capacitor values, and design of additional on-chip circuitry. Section 4 discusses the output capacitor elimination. Section 5 presents the simulation results and performance comparison versus other types of switching converters. Section 6 shows the experimental results. Conclusions are drawn in Section 7.
TOPOLOGY AND OPERATING PRINCIPLE

Figure 1 shows the proposed resonant H-SCC converter using 1 SC cell. This topology consists of 4 power switches, 1 flying capacitor, 1 inductor, and 1 optional output capacitor ($C_{out}$). The on-chip power train is composed of 5 V NMOS transistors and 1 flying capacitor ($C_{fly}$). The output is filtered by an SMD (or PCB-integrated) air-core inductor and an (optional) SMD output capacitor. This topology uses an inductor in series with the LED load, which makes it a perfect candidate for a current-controlled topology. Transistors $Q_3$ and $Q_4$ emulate the function of 2 diodes, $D_3$ and $D_4$, respectively. The integrated zero-current detection (ZCD) circuit discussed in Section 3.3 is used to control $Q_3$ and $Q_4$ with very low conduction voltages in a commercial CMOS process. The H-SCC is designed to drive a 700 mA LUXEON Rebel LED, LXML-PWN2.

The basic operation mode of this converter is exploiting resonance between $C_{fly}$ and $L$. The inductor current waveform and the gate-source voltage ($V_{GS}$) of the power switches in this mode of operation are shown in Figure 2. Power switches $Q_1$ and $Q_3$ are switched on when the control signal $\phi_1$ is activated; while switches $Q_2$ and $Q_4$ are switched on when the control signal $\phi_2$ is activated. In pure resonance, an output voltage $V_{out} = V_{in}/2$ is generated under no load conditions. This can be demonstrated imposing charge conservation to the flying capacitor between the 2 phases ($\phi_1$, $\phi_2$).

There are 2 main advantages in the pure resonant mode. The first is the reduced size of the required passive components when compared with conventional inductive converters at the same switching frequency. Indeed, in pure resonant operation, the apparent frequency of the inductor current $I_L$ is twice the switching frequency (as one can see from the shape of $I_L$ in Figure 2): This halves the size of the needed inductor.

The second advantage is the reduction of the switching losses because of the ZCS. To achieve ZCS, $Q_3$ and $Q_4$ should block the reverse currents from the load to the power train potentially created by the resonant operation. Therefore, as we already noticed, those switches should work as diodes. The internal control signals $\phi_1$ and $\phi_2$ turn on $Q_3$ and $Q_4$ when the corresponding diodes should conduct (Figure 2), while the integrated ZCD circuitry turns $Q_3$ and $Q_4$ off when the inductor current crosses zero. Alternatively, inherent ZCS operation can be performed by the LED diode when the output capacitor is removed. Both cases will be investigated experimentally in Section 6.

The fixed output voltage at $V_{in}/2$ is the main disadvantage of the resonant operational mode, especially considering the variability of the LED forward voltage in production (LEDs are typically divided in several bins, with different forward voltages). A variable output voltage must be enabled to build practical LED drivers. The basic resonant operation can be further extended to enable output voltages above and below $V_{in}/2$. Using switching frequencies below the
resonance frequency \( f_0 \) will produce output voltages lower than \( V_{in}/2 \). This mechanism is called dynamic off-time modulation.\(^{18}\) On the other hand, switching frequencies above \( f_0 \) can be used to increase \( V_{out} \), but this makes ZCS impossible and leads to higher switching losses because of the hard switching. In this mode of operation, the H-SCC operates as the classical 3-level buck converter in CCM.\(^{22}\) To provide an output voltage above \( V_{in}/2 \) while preserving ZCS, in this work is used an additional state where the inductor is charged directly from \( V_{in} \), ie, exploiting inductive energy accumulation. Changing the duration of this additional state enables to control the output voltage and thus the LED current while maintaining ZCS. The equivalent circuits for each operational state of the H-SCC are shown in Figure 3. A detailed description of all different states is provided in this section.

State 1 (Figure 3A, S1): In this state, the inductor \( L \) is charged using the switches \( Q_1 \) and \( Q_2 \). The charge in the flying capacitor is kept unchanged. This state is enabled when the “third phase” (\( \phi_3 \) in Figure 4) is active. In this state, the current of the inductor increases linearly as:

\[
I_L(t) = \frac{(V_{in} - V_{out})}{L} t
\]  

FIGURE 3 Equivalent circuits of the H-SCC converter in state 1 (A), state 2 (B), state 3 (C), and state 4 (D)

FIGURE 4 Inductor current waveform and gate control signals. Full state sequence: S1 \( \rightarrow \) S2 \( \rightarrow \) S3 \( \rightarrow \) S1 \( \rightarrow \) S4 \( \rightarrow \) S3
where \( V_{in} \) is the input voltage and \( V_{out} \) is the output voltage of the converter, as well as the forward voltage of the LED. Increasing the duty cycle of the third phase (\( D_{\phi_3} = t_{\phi_3}/T \)) increases the output voltage (or LED current). This functionality is explained in detail in Turhan et al.19

State 2 (Figure 3B, S2): In this state, the current flows from \( V_{in} \) through \( Q_1, C_{fly}, Q_3, \) and \( L \) to the LED load. This state is the first part of the resonance operation of the H-SCC. The current waveform in this state, which is enabled by \( \phi_1 \), can be observed in Figure 4. The current in the inductor is described by:

\[
I_L(t) = i_0e^{-at}\cos(\omega_d t) + \frac{2(V_{in} - V_{out} - V_{c1})}{Z} + i_0R_{ESR}e^{-at}\sin(\omega_d t)
\]  

(2)

where \( i_0 \) and \( V_{c1} \) are the inductor current and voltage across the capacitor \( (C_{fly}) \) at the end of state 1, \( \omega_d \) is the resonance frequency, given by \( \omega_d = \sqrt{\frac{1}{LC_{fly}}} \), and \( \alpha = R_{ESR}/2L \), and \( Z \) is the impedance given by \( Z = \sqrt{4L/C_{fly} - R_{ESR}^2} \). \( R_{ESR} \) represents the series resistance in the path of the inductor current, ie, on-resistance of the switches, inductor resistance, and capacitor ESR. Neglecting the effect of this resistance, (2) is identical to the expression presented in Turhan et al.19

State 3 (Figure 3C, S3): This state starts when the inductor current reaches \( I_L = 0 \), and the switches \( Q_3 \) or \( Q_4 \) are switched off by the integrated ZCD circuitry to avoid a negative current in the inductor. In this state, the current for the LED is entirely supplied by the output capacitor \( (C_{out}) \), or in case this capacitor is removed, the LED voltage decreases slightly below the turn-on value, the current flowing through the LED becomes very small, and it is supplied by the internal LED capacitance. This state guarantees ZCS in the next state. The modulation of the duration of this state, \( \phi_{off} \) in Figure 4, can be used to reduce the average output current (or output voltage).

State 4 (Figure 3D, S4): In this state, the current flows from the flying capacitor \( C_{fly} \) through \( Q_4, Q_2, \) and \( L \) to the LED load. The current waveform in this state, which is enabled by \( \phi_2 \), can be observed in Figure 4. The current of the inductor is described as:

\[
I_L(t) = i_0e^{-at}\cos(\omega_d t) - \frac{i_0R_{ESR}-2(V_{c2}-V_{out})e^{-at}\sin(\omega_d t)}{Z}
\]  

(3)

where \( V_{c2} \) is the capacitor \( (C_{fly}) \) voltage from the previous state.

The full working sequence of the H-SCC converter is \( S1 \rightarrow S2 \rightarrow S3 \rightarrow S1 \rightarrow S4 \rightarrow S3 \), as shown in Figure 4. With this sequence, the maximal freedom of choice in conversion ratio is obtained. Other working sequences are also possible: The pure resonance operation exploits only the state sequence \( S2 \rightarrow S4 \) (Figure 2, \( V_{out} = V_{in}/2 \)). To decrease the output voltage below \( V_{in}/2 \), the sequence of states \( S2 \rightarrow S3 \rightarrow S4 \rightarrow S3 \) (Figure 5A) can be used. On the other hand, to increase \( V_{out} \) above \( V_{in}/2 \), the sequence of states \( S1 \rightarrow S2 \rightarrow S1 \rightarrow S4 \) (Figure 5B) can be used.

**3 | CONVERTER DESIGN**

**3.1 | Converter optimization procedure**

To optimize the design variables, an analytic model of the losses in the H-SCC using the basic resonance mode was created. The optimization searches for the optimal power efficiency and power density; hence, a multiobjective optimization based on the weighted-sum method was performed; the objective function \( (F) \) is set as:

\[
F = \lambda \eta_n + P_{dn} \times (1 - \lambda)
\]  

(4)

where \( \lambda \) is the weight of the efficiency, \( \eta_n \) is the normalized power efficiency, and \( P_{dn} \) is the normalized power density. The complementary weight in \( F \) allows to optimize the converter looking for the best power efficiency without considering the power density (\( \lambda = 1 \)) or looking for the most compact design without considering the power efficiency (\( \lambda = 0 \)). The normalized values are computed as \( X_n = X/X_{max} \) where \( X \) is the power efficiency (\( \eta = P_{out}/P_{in} \)) or power density (\( Pd = P_{out}/A \)) for a specific range of capacitor sizes. Here, \( P_{out} \) is the output power of the converter, \( P_{in} \) is the input power of the converter and can be computed as \( P_{in} = P_{out} + P_{losses} \), \( P_{losses} \) is the total LED driver dissipation (or total...
losses), and $A$ is the total occupied area. The explored design space includes the parameters switching frequency, size of the gate drivers (number of stages and tapering factor—see Section 3.3), size, and $W/L$ ratio of switches for a given range of capacitor sizes. LUXEON Rebel series LEDs have an optical area around 7.35 mm$^2$ and a package area of 13.69 mm$^2$; if the size of the LED driver IC is constrained to 6.34 mm$^2$, then the IC can fit together with the LED in the same package. Therefore, this area $A$ was considered the upper limit for the size of the capacitor, which is responsible for the largest area consumption in the IC. A small footprint (0.72 mm$^2$) power inductor family (Coilcraft PFL1005) was used as inductor, and the optimization was repeated for each inductor in the family, to find the inductor enabling best efficiency.

The optimization of the topology is based on the basic resonance operation mode. It is assumed $V_{in} = 5V$ and a LED with nominal on-voltage of 2.5 V: With this choice, thus, the converter in resonance operation ($V_{out} = V_{in}/2$) provides exactly the nominal current to the LED. The loss model accounts for conduction, driving, and switching losses. Further details are provided in this section.

### 3.1.1 Conduction losses

These losses are associated with the resistance of the path where the current flows in the resonant states S2 and S4: $R_{ESR} = 2R_{on} + DCR$, where $R_{on}$ is the on-resistance of the switches, which depends on the gate drive voltage and $DCR$ is the DC resistance of the inductor. The resistance of the bond wires and shunt sensing resistance can also be added to $R_{ESR}$. The effective resistance at resonance $R_{EFF}$ given in Kesarwani$^{18}$ was used to compute the conduction losses:

$$P_{cond} = R_{EFF} \times I_{LED}^2$$

where $I_{LED}$ is the LED current, $R_{EFF} = \frac{1}{4f_0C_f} \tanh \left( \frac{R_{ESR}}{8f_0L} \right)$, and $f_0$ is the resonance frequency, which, in this case, is equal to the switching frequency.
To compute $I_{LED}$, a SPICE model of the LUXEON Rebel series LED was used together with the expression of the loaded output voltage: $V_{out} = V_{in}/2 - R_{EFF,ILED}$.

### 3.1.2 Switching losses

Because the switching occurs with ZCS, the switching losses associated with the Miller plateau of the switch gate voltage can be neglected. However, switching losses associated with the input and output capacitances of the switches ($C_{iss}$, $C_{oss}$) and with the bottom plate parasitic capacitance must be taken into account. The input capacitance losses are defined as:

$$P_{swIiss} = \sum_{i=1}^{N_{sw}} C_{iss} f_0 V_{gate}^2$$

where $N_{sw}$ is the number of switches in the power train and $V_{gate}$ is the gate voltage of the switch. The output capacitance losses are defined as:

$$P_{swOoss} = \sum_{i=1}^{N_{sw}} C_{oss} f_0 V_{ds}^2$$

where $V_{ds}$ is the drain-source voltage that the switches have to withstand in the off-state. Finally, the bottom plate capacitance losses are given by the expression:

$$P_{swWBP} = \beta C_{fly} f_0 \left(\frac{V_{in}}{2}\right)^2$$

where $\beta$ is the technology-dependent coupling factor between the bottom plate of the flying capacitor and the substrate.

### 3.1.3 Driving losses

Tapered buffers are used to drive the gates of the power switches according to the digital control signals. An optimized inverter sizing was used, based on the energy consumed by each buffer in the tapered buffer and the rise/fall time. The power losses in the tapered buffers are named $P_{driver}$. More details on the model used for these losses are given in Villar et al.

The total dissipation ($P_{losses}$) is modeled by the sum of $P_{cond}$, $P_{swIiss}$, $P_{swOoss}$, $P_{swWBP}$, and $P_{driver}$. It is used to compute the power efficiency in (4).

The 0.18-μm CMOS process was characterized to estimate the on-resistance ($R_{on} = 1457[\Omega \mu m^2]$), input capacitance ($C_{iss} = 3.53[fF/\mu m^2]$), output capacitance ($C_{oss} = 1.44[fF/\mu m^2]$), and parasitic coupling factor ($\beta = 0.004$). As mentioned before, the on-resistance depends on the gate voltage of the switch. Hence, the optimization also takes into consideration gate voltages below the nominal value of the switches (5 V), to reduce the switching losses associated to the input capacitance. The actual voltage applied to the gate of the switches can be generated on-chip without any external component, as described in Section 3.2. A model of the inductance and DCR values for the inductor family Coilcraft PFL100S was also used in the optimization.

The Pareto front results of the multiobjective maximization for $L = 100 \text{ nH}$ and $0 < \lambda < 1$ in (4) are shown in Figure 6 on the efficiency versus power density plane. Every point corresponds to an optimal combination (maximum $F$) of the parameters previously mentioned according to the chosen maximum capacitance area and value of $\lambda$.

![Figure 6](https://wileyonlinelibrary.com)
shows a trend where giving more weight to the efficiency will increase the final area of the IC. A design with $\lambda = 0.03$ and $L = 100$ nH was finally chosen, which corresponds to $f_o = 3.5$ MHz, $C_{fly} = 16$ nF, $Ron_{SW} = 0.069\Omega$, and $A = 4.02$ mm$^2$. The breakdown of the losses for the optimized design is shown in Figure 7.

3.2 | Self-biasing gate driving scheme

The driving voltage to turn on the power NMOS switches is generated on-chip using bootstrap circuits assisted by the flying capacitor of the H-SCC. The implementation is illustrated in Figure 8. In $\phi_1$ (green), the switches $Q_1$ and $Q_3$ are turned on; thus, $C_{s2}$ and $C_{s4}$ are charged to $V_{in} - V_c$ and $V_c$, respectively, being $V_c$ the voltage over the flying capacitor. In a similar way, in $\phi_2$ (blue), the transistors $Q_2$ and $Q_4$ are closed; thus, $C_{s1}$ and $C_{s3}$ are charged to $V_{in} - V_c$ and $V_c$, respectively. The voltages generated on the bootstrap capacitors ($C_{sx}$) are used to supply the gate drivers.
3.3 | Gate driver

The gate driver is used to switch on and off the large power switches in the H-SCC, and it is also integrated on-chip. It is composed of 2 main blocks: a level shifter and a tapered buffer (Figure 9). A conventional level shifter is used to translate the digital control signal $\phi_1$ or $\phi_2$, from a low-voltage domain (between $V_{DD} = 1.8$ V and Gnd) into a high-voltage domain (between $V_{drive}$ and $V_S$), being $V_S$ the source voltage of the power switch. The voltage $V_{drive}$ is provided by the aforementioned self-bias gate driving scheme. The tapered buffer interfaces the high-impedance output of the level shifter with the large input capacitance of the power switch ($Q_x$). The design of the tapered buffer is based on a basic 5 V inverter cell ($L_{min} = 0.7 \mu m$ and $W_p/W_n = 3 \mu m/1 \mu m$); the tapering factor ($\kappa = 3.38$) and the number of scaled inverters ($n = 7$) are designed according to the size of the power switch ($W/L = 512 \times 60 \mu m/0.7 \mu m$). These parameters are computed by the aforementioned optimization algorithm.

3.4 | Zero-current switching and zero-current detection

As mentioned before, transistors $Q_3$ and $Q_4$ (Figure 1) emulate the function of 2 diodes, $D_3$ and $D_4$, respectively. The cathode of $D_3$ is connected to the inductor, and the cathode of $D_4$ is connected to the flying capacitor. Switches $Q_3$ and $Q_4$ are turned on using the control signals $\phi_1$ and $\phi_2$ (Figure 4). At the same time, an integrated ZCD circuit monitors the source and drain potentials ($V_{ds}$) of $Q_1$ and $Q_4$. $Q_1$ is used as monitor device instead of $Q_3$ for convenience in the design. If a $V_{ds}$ changes its polarity, the corresponding diode, $D_3$ or $D_4$, should be switched off (to avoid current flowing from cathode to anode), and thus, $Q_3$ and $Q_4$ are immediately switched off pulling down the gate terminal.

The low side (ZCD$_{LS}$) detection to control the switch $Q_4$ and the high side (ZCD$_{HS}$) detection to control the switch $Q_3$ are implemented using 4 circuit blocks, as shown in Figure 10. Only the high side circuit is shown in this figure, as the ZCD$_{LS}$ circuit is similar to ZCD$_{HS}$.

**FIGURE 10** High-side zero-current detection block diagram

**FIGURE 11** Gm transconductor, latch and output amplifier used in high-side zero-current detection [Colour figure can be viewed at wileyonlinelibrary.com]
The first ZCD_HS block is a transconductance amplifier (gm), which provides high input impedance and transforms $V_{ds}$ in a differential current signal. The circuit implementation is shown in Figure 11. The bulk connection of the input transistors increases their threshold voltage $V_{th}$. This provides a proper bias point to the input pair when the common mode voltage is close to the rail $V_{in}$.

The second ZCD_HS block is a current-input latch composed of MP5-MP8 (Figure 11). To reduce power consumption and delay, this circuit is supplied by $V_{DD}$, which is a DC voltage lower than $V_{in}$. The third block is an output amplifier, which creates a logic swing from the comparator output (Figure 11). To save power, the previous stages of the ZCD_HS and ZCD_LS are turned on only in $\phi_1$ and $\phi_2$, respectively.

Finally, the fourth ZCD_HS block is a D flip-flop (Figure 10), which avoids undesired triggering produced by ringing at the input of the ZCD detection. A delay in the preset of the flip-flop creates a blanking time used to avoid false detections at the beginning of the phases $\phi_1$ and $\phi_2$ (Figure 4); indeed, zero crossing detection is always performed at the end of a phase.

4 | OUTPUT CAPACITOR ELIMINATION

The output capacitor ($C_{out}$) plays 2 important roles in existing topologies of LED drivers. The first is to reduce the output voltage ripple, which also improves the stability of the voltage-based control loop. The second functionality is voltage buffering when an on/off control is used to dim the intensity of the light. In some cases, a large value of the output capacitor is recommended, eg, 4.7 $\mu$F for the LM3549 LED driver. However, large values of $C_{out}$ come typically together with poor reliability, especially when using electrolytic capacitors, and additional volume/area occupancy.

LED loads demand a current control from the converter, to control the light output. In inductive topologies without $C_{out}$, the current ripple is determined by the value of the inductor. In the proposed H-SCC, elimination of $C_{out}$ is possible. In the basic resonance mode of the H-SCC (states S2 and S4), the LED current ripple is limited by the converter impedance ($Z$), as discussed in Section 2. When $C_{out}$ is absent, $I_{LED} = I_L$ and $V_{out} = V_{LED}$ changes with the varying current though the LED. However, because of the exponential relationship between current and voltage in the LED, the change in $V_{LED}$ is negligible, and thus, Equations (1), (2), and (3) for the states S1, S2, and S4 are still approximately valid. In state S3, $V_{LED}$ decreases slightly below the switch-on value and the current in the LED becomes very small. For this reason, the LED capacitor is sufficient to keep the LED voltage just below its turn-on value. It can be concluded that, even in the absence of $C_{out}$, $V_{LED}$ is approximately constant in all states of the switching sequence, and thus that the analysis in Section 2 can be applied also to the case without output capacitor. This will be confirmed experimentally in Section 6 (Figure 17).

The diode characteristic of the LED ensures ZCS operation when $C_{out}$ is eliminated, even if $Q_1$ and $Q_4$ would not be switched off when the inductor current crosses the zero point. If $C_{out}$ is removed, the power losses because of its ESR and the cost/reliability issues related to $C_{out}$ will be avoided too. No additional conduction losses are added to the converter, as the average current and the RMS current in the power train are very similar to the ones observed when $C_{out}$ is present, as discussed above.

In functionality, the proposed H-SCC can provide 2 more features without additional circuitry: fast dimming control and peak current control. The dimming of the light intensity exploits average current control adding to the switching sequence a state S3 of variable duration. The resulting average dimmed $I_{dim}$ current is related to the output current in the absence of dimming $I_0$: $I_{dim} = I_0 T_0/T$, where $T$ is the duration of all states and $T_0$ is the duration of S1, S2, and S4. The MHz range of the driver makes possible to achieve dimming current, even at 10% of the nominal current load, without suffering from perceivable flickering, as will be experimentally demonstrated in Section 6. Also, the elimination of $C_{out}$ makes possible fast dimming, which is required in applications such as displays or visible light communications.

Damages and color drift in the LED can be avoided controlling the peak current. For example, the LXML-PWN2 LED sets the maximum peak pulsed current at 1200 mA for pulses shorter than 5 ms. Choosing suitable limits to the duration of $\phi_3$ (state S1), the peak current can be kept below the advised maximum, while dimming can still be performed, according to the sequence in Figure 4.

5 | COMPARISON TO OTHER SWITCHING CONVERTERS

A simulation study to compare the performance of the main topologies of LED drivers is presented in Figure 12A. It includes a 2:1 SCC, a buck converter, and the H-SCC described in this paper, with and without $C_{out}$. The total volume occupation of the passives and switches was kept similar for all the options (Figure 12B). Also, the same load (LED LXML-PWN2) and 100 nH inductor (PFL1005) were used when performing circuit-level simulations.
The SCC used in this comparison uses the same size of flying capacitor and power switches as the proposed H-SCC. The dimming was achieved with frequency modulation. The synchronous buck converter uses switches twice larger than the H-SCC to maintain the same area, and it has the same inductor value as the H-SCC. The output current of the buck converter is controlled by the duty cycle, while the switching frequency was optimized to obtain the best efficiency in the LED current range. For the H-SCC, output powers below the nominal, the converter was operated using state S3 ($\phi_{\text{off}}$). The nominal power is the one achieved with the basic resonance state, i.e., $V_{\text{LED}} = \frac{V_{\text{in}}}{2}$. For higher output powers, state S1 ($\phi_3$) is used.

This comparison shows the performance advantage of the H-SCC solution in efficiency. Also, it shows the limitation of the SCC to reach higher output powers, while the H-SCC can reach large power using its $\phi_3$ functionality. The performance of the buck converter is limited by the switching losses of larger switches and the small size of the inductor; also, small duty-cycle values (lower than 0.1) are required to decrease further the LED current. The H-SCC without $C_{\text{out}}$ is more efficient at low output powers, while it provides similar performance to the version with $C_{\text{out}}$ at larger output powers.

### EXPERIMENTAL RESULTS

The H-SCC LED driver previously discussed is implemented using a 0.18-μm commercial CMOS technology. N-MOS switches and capacitors are rated at 5 V. Figure 13 shows a die photo, where the flying metal-insulator-metal (MIM) capacitor, the power switches, and the gate drivers have been highlighted.

Using MIM capacitor not only provides reasonable capacitor density (4.1 fF/μm²) but also allows to place switches and circuits under the capacitor to save area in the design. Therefore, the area of the die is limited by the size of $C_{\text{fly}}$. The effective area of the whole converter, including the SMD inductor (PFL1005), is 7.74 mm², while the effective volume of the driver is 6 mm³, considering the height of the SMD component as the limiting dimension.
The power switches are physically implemented through the parallel connection of a $32 \times 16$ array of 5 V N-MOS transistors using minimum length (which is 0.7 $\mu$m for 5 V transistors in the technology used) and $W = 60 \mu$m. Each transistor in the array has an on-resistance of 34.7 $\Omega$. To decrease interconnection resistance and reduce electromigration effects, several metal layers are stacked to interconnect the transistors in the array. Moreover, guard rings are used to decrease the switching noise coupled to the substrate. The 4 switches $Q_1$ to $Q_4$ are placed to minimize interconnection length.

An LXML-PWN2 LED is used to measure the performance of the proposed H-SCC at $V_{in}=5$ V. The gate-source voltages produced by the self-biasing scheme have 2 V amplitude. The waveforms obtained when implementing the sequence $S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_1 \rightarrow S_4 \rightarrow S_3$ (Figure 4) are shown in Figure 14. The ZCD functionality can be observed in the same figure, where $V_{GS3}$ and $V_{GS4}$ are turned off when the inductor current $I_L$ becomes zero. Also, experimental waveforms of the inductor current and flying capacitor voltage are shown in Figure 14.

A step transition of $t_{\phi3}$ from 0 to 80 nanoseconds is shown in Figure 15. At $t_{\phi3} = 0$, the output voltage for $V_{in} = 5$ V is not enough to switch on the LED; while increasing the duration of $t_{\phi3}$, the LED current starts to flow through the inductor. Current peaking is very limited.

**FIGURE 14** Measured gate voltage, flying capacitor voltage, and inductor current waveform in a sequence using $S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_1 \rightarrow S_4 \rightarrow S_3$ [Colour figure can be viewed at wileyonlinelibrary.com]
The H-SCC efficiency using the output capacitor at $V_{in} = 5$ V is measured for several combinations in the time duration of S1 and S3; steps of 10 nanoseconds were used to generate the control signals. The reported efficiency includes all the losses in the power train and the gate drivers. The measurements are shown in Figure 16 together with the results of simulations that include the resistance of the interconnections between the PCB die and the tracks inside the IC. The resistance of these interconnections is measured to be 134 mΩ for each power connection ($V_{in}$, $V_{out}$, and $Gnd$). The peak experimental efficiency using $C_{out}$ is 90.2%, while the minimum efficiency is 82.9%.

The H-SCC converter without the output capacitor was tested too. The LED voltage and current waveforms are shown in Figure 17. As discussed in Section 4, the LED voltage remains rather constant, while the current peak is controlled by the duration of S1. The average current through the LED is controlled by varying the duration of S1 and S3. The peak current is set to 0.7 A using S1, and the average LED current is dimmed to 10% using S3; in this case, the switching frequency is reduced to 925 kHz.

The IEEE Standard 1789-2015 recommends 3 kHz as lower limit for the dimming frequency for no observable effect level of flicker. The spectrum of the LED current from Figure 17, which is shown in Figure 18, reveals no observable flickering for this dimming point. At low frequencies (<3 kHz), the only observable component is at DC.

In Figure 19, the efficiency of the H-SCC without using the output capacitor was measured at $V_{in} = 5$, 4.5, and 4 V. In this case, the maximum experimental efficiency is 93.0% (at $V_{in} = 4$ V), while the minimum efficiency is 83% (at $V_{in} = 5$ V). The maximum measured LED power is 2.05 W. Using the size of the inductor and the effective size of the chip, the power density is 0.26 or 0.34 W/mm³. The measurement setup is shown in Figure 20 with the SMD inductor, LED, and the IC.

**FIGURE 15** Measurements results of step change in phase 3 time ($t_{\phi 3}$), from 0 to 80 nanoseconds. Logic switch signals (red). CH2: $V_{out}$ (purple, 2 V/div). CH4: inductor current $I_L$ (green, 0.34 A/div) [Colour figure can be viewed at wileyonlinelibrary.com]

**FIGURE 16** Measurement and simulation results at $V_{in} = 5$ V. Efficiency for varying output current delivered to the LXML LED, using the $C_{out}$ [Colour figure can be viewed at wileyonlinelibrary.com]
Figure 21 shows the performance of state-of-the-art fully integrated SC voltage converters in the efficiency versus power density plane. Good efficiencies are obtained with the proposed H-SCC using low-cost bulk CMOS technologies. Similar results using resonant SCCs have been obtained recently by Kesarwani et al.18 and Schaef et al.31

The measured performance of the presented on-chip H-SCC LED driver is summarized in Table 1. In the same table, the converter is compared to state-of-the-art on-chip DC-supplied LED drivers and commercial drivers. The efficiency of the H-SCC here described is compatible with the state-of-the-art integrated DC-inductive LED drivers, while using 10 times smaller inductor values and no additional external components.
FIGURE 19  Measurement results at several input voltages. Efficiency for varying output current delivered to the LXML LED without $C_{out}$
[Colour figure can be viewed at wileyonlinelibrary.com]

FIGURE 20  Measurement setup using LED LXML-PWN2 and PFL1005 inductor
[Colour figure can be viewed at wileyonlinelibrary.com]

FIGURE 21  State-of-the-art of fully integrated capacitive DC-DC converters. Adapted from Steyaert et al.14 [Colour figure can be viewed at wileyonlinelibrary.com]
CONCLUSION

The first miniature H-SCC IC-integrated LED driver capable to control the output average and peak current with high efficiency has been presented. Its S1 and S3 states make possible the operation with a wide selection of LED forward voltages, so that no binning of the LEDs is needed. A peak efficiency of 93% was achieved reaching a power density of 0.26 W/mm² (0.34 W/mm³). The operation of this converter without output capacitor shows efficiencies from 83% to 93% depending on the output current and no light flicker of the LED load even when dimming the light to 10% of the nominal value. The use of a small inductor (<1 mm²) makes negligible the inductive area used by the driver. This work is compared to commercial LED drivers and state-of-the-art literature works that have similar specifications, showing higher efficiency than previous SCC solutions and a 10× smaller inductor than previous integrated inductive LED drivers while keeping comparable efficiency. The benchmark against integrated SC voltage converter solutions from literature shows, for our H-SCC approach in bulk CMOS, excellent efficiency and a power density comparable with the best state of the art. Our LED driver on-chip aims at mid-power and low-power applications where small form factor is an important advantage, eg, LED torches, camera lights, cellphones, personal digital assistants, and retrofit lamps. Monolithic integration of the power train (power switches and flying capacitor) and analog circuitry (eg, ZCD, gate drivers, and self-biasing scheme) reduce parasitic components, enabling switching frequencies in MHz range with lower power losses. This, together with the possibility to eliminate the output capacitors and the use of the H-SCC approach, which greatly scales down the inductor size needed in the converter, enables a LED driver with state-of-the-art efficiency and a volume of only 6 mm³.

ACKNOWLEDGMENTS

This work was supported in part by the ASLS Research Program under Project 12759, in part by The Netherlands Organisation for Scientific Research Domain TTW, and in part by Philips Lighting.

ORCID

Juan C. Castellanos http://orcid.org/0000-0001-6422-2575

REFERENCES


13. Ng V. Switched Capacitor DC-DC Converter: Superior where the BuckConverter has Dominated, PhD Dissertation, University of California, Berkeley, December 2011.


27. Linear Technology, “400mA single wire camera lens charge pump,” LTC3218 datasheet.


33. Texas Instruments, “TPS6105x high-power white LED driver,” TPS61054 datasheet, September 2004 [Revised September 2015].


How to cite this article: Castellanos JC, Turhan M, Hendrix MAM, van Roermund A, Cantatore E. Dimmable integrated CMOS LED driver based on a resonant DC/DC hybrid-switched capacitor converter. Int J Circ theor Appl. 2018;46:1485–1502. https://doi.org/10.1002/cta.2512