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Automatic Generation of In-Circuit Tests for Board Assembly Defects

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Abstract — The components and the solder joints that are made during assembly are the ultimate goal of the component manufacturer. The tests to check the quality of the assembly are performed after the assembly process is completed. We present a method to automatically generate in-circuit tests for board assembly tests. The approach is based on the graph representation of the design of the board and the manufacturing processes that are used to make the board. The method is implemented in the software tool AutoGen. The tool is used to generate tests for the board assembly defects. The tests are generated based on the the design files of the device-under-test (DUT). The data that is needed is component information (e.g., reference designator (refdes [5]), type, value, tolerance) and interconnection data, i.e., the nets that describe the connections between the components on the board. Since the possibilities to test components are limited by the capabilities of the board tester, the tool needs to know the capabilities of the board tester, such as (1) the voltage and frequency range of the signal generators, (2) the sensitivity and measurement ranges of the tester, (3) the impedance patterns obtained for a known-good (“golden”) board. For further computation, we convert the netlist into an undirected multigraph $G = (V, E)$, where $V$ denotes the set of vertices and $E$ the set of edges. Contrary to what one might intuitively expect, we found that in our application representing components by edges and nets by vertices works best. However, multi-pin components, such as transistors and ICs, do not fit this representation, and therefore these components are represented by a vertex as well, with edges representing the pins of the component. In the graph net-vertices are marked to either have probe access or not. The edges are provided with a label that contains the refdes, component type, and value and tolerance.

1 Introduction
In board assembly, electronic components are soldered onto a printed circuit board (PCB). Boards contain a mix of passive and active discrete components, as well as (digital) integrated circuits (ICs). We distinguish components based on through-hole technology (THT) and surface-mount technology (SMT). THT components, of which the leads are inserted into holes in the PCB, have been largely replaced by the much smaller SMT components which are placed on top of the board. Board assembly suffers from defects, and hence the assembled PCBs need to be tested. The bare PCB as well as the components are assumed to be fault-free. There are various ways in which the PCBs can fail during manufacturing tests by their respective suppliers. Hence, what need to be tested after board assembly is whether or not the components are correctly soldered onto the PCB. Defects considered are expressed in the PCOLA-SOQ [1] score; this method assigns a coverage score to Presence, Correctness, Orientation, Linearity, and Alignment and that (1) the granularity of the clusters is as small as possible, and (2) any alternative (‘false’) paths between two target probe points are neutralized by guarding them with additional probes.

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It might happen that a collapsed structure is still not reachable by probes on either end, e.g., edges e8, e9, and e10 of Figure 2(c). If this is the case it can be concluded that probe access has to be added to reach the components within this structure.

### 3.2 Subgraphs

A structure is tested by connecting a source probe to one of the vertices of the structure, a measurement probe to the other, and executing a test routine. However, since the structures are tested while having been soldered onto a PCB, there might be paths other than the SUT that allow current to flow from source to measurement. These paths are called false paths.

Note that false paths can only be simple paths; a net cannot have multiple voltages at the same time and current cannot flow through it more than once. A closer look at these false paths reveals an interesting property, viz., that edges being in a false path of the SUT are both a reflexive and a symmetric relation. If one observes that each false s, m-path of an edge \( e = \{ s, m \} \) together form a simple cycle, the rest of the proof is trivial. From this it follows that the connected components can be split into subgraphs that for each edge e contains itself and all of its false paths. This split happens to be equal to the biconnected components [6] of the graph.

### 3.3 Minimal Guard Set

If a false path is not guarded it likely will influence the measurement. However, if too many nets are guarded in a false path, components are shorted between two guarded nets, which negatively influences the guard ratio. Moreover, since the impedance of these components might be dependent on the frequency, the ideal set of nets that are guarded is dependent on the selected frequency that will be used to test the structure. The goal of the minimal guard set algorithm is to find all possible sets of vertices that guard all false paths with as few components shorted between guards as possible. It does this by first discovering all paths. Next vertices without probe access are removed since these cannot be guarded. These paths are then sorted on length to prevent that a path gets guarded twice because it coincides with a shorter path. Finally the algorithm recurses the paths, selecting new nets to guard if the path wasn’t already guarded by a previously selected net. All other vertices in the path are marked as ‘not preferred’ since selecting these would cause components to be shorted between guards.

### 3.4 Maximal Voltage

The maximum voltage that can be safely applied to a net is typically limited by the active components that can be reached from that net. As mentioned in Section 3.1 a maximal safe voltage can be assumed in order to prevent damages to all paths between a source probe and active components are forced to a potential of \(-0V\), this is not necessary. Guard and measurement probes exactly do this. Therefore by discovering if there are any paths from the source probe to an active component, without crossing either an guarded or a measured vertex, the measurement can be determined to be limited by a safe voltage.

### 3.2 Test Mapping

Isolated structures contain only a single component, and therefore it is easy to create a library of test cases that can be mapped on the isolated structures of the DUT to cover all the cases. However, for compound structures this is not true since this can consist of multiple different components, in multiple different combinations. To maximize the test coverage a generic test method is needed that tries to map a test on a structure if there is no test found in the test library. We deploy both solutions to get the best of both worlds.

### 3.2.1 Library Test Mapping

The library test mapping procedure maps tests from a pre-defined test library onto the structures of the DUT. This library contains product-independent tests, which all specify a so called mold which defines which combinations of components can be covered by the test, and a test mapping procedure.

If an (expanded) structure and a mold are isomorphic [7] such a mapping from test to false path measurement probes to the reachable vertices of the structure is preserved, and all of the labels of the mold and structure match, then the mold matches and the mapping procedure will continue. Figure 3 shows an example of a compound mold. Only structure 2 matches since it contains the right component types, the combined value of the capacitors is within the specified range, while the orientation is irrelevant.

### 3.2.2 Generic Test Method

All structures that could not be covered by a test defined in the test library are handed to the generic test method (GTM). The generic test method is a method that tries to map a test as effective as possible, regardless of what is inside that structure. The generic test method can only perform impedance measurements and is therefore more limited than the tests in the library.

To determine the frequencies to test a structure at, the generic test method has to determine at which frequencies the components in the structure are visible. Just like the components inside the structure, the impedance of the structure itself has a tolerance. Using modified nodal analysis [8] the currents through and voltages over each component can be determined. If the current through a component within the structure is large enough to be not within the tolerance of the structure, it is not current-dominated and its presence can be determined. Analogous, if a component is not voltage-dominated, it can be determined to be both correct and live.

Using this principle, the PCOLA-coverage can be determined for each of the test frequencies by scanning the frequency domain for the SUT. By selecting as few as possible frequencies that result in maximal coverage, the efficiency can be optimized. In order to determine the guard ratio, the impedance of the false path is determined next. Finally a suitable voltage is selected that is lower than the determined maximal voltage, but high enough for the board tester to perform a reliable measurement. From these potential tests, all tests that are superflous are removed.

### 4 Experimental Results

We selected three boards for consumer and industrial applications from the Protridge Technologies product catalog for our experiments: (1) the QA board is specially designed for qualification of the ICT tester hardware, (2) the EQDM board is designed towards maximum ICT access, and (3) the ECU board is the first board that has a test running in production that is generated using this tool. For the largest board in this comparison, EQDM, that has over 3000 components, generating the test takes about 15 minutes on a PC with a Core i7-6820HQ CPU at 2.7 GHz and 8 GB of DDR4 RAM at 2.133 GHz.

The tests generated for the ECU board are executed using set of 15 boards. 252 of the 299 tests (84,28%) prove to be stable with \( f_{\text{cutoff}} \geq 2 \) [9, 47 tests required a minor change to e.g., limits or frequency in order to get a stable test. The generated test for the QA board ran successfully, none of the tests steps proved to be unstable.

### 5 Conclusion

The graph representation of a board design has proven to be a versatile tool that allows for relative easy computation of the the false paths and the impedances between certain nets. It allows unreachable structures to be collapsed into reachable component structures and decomposing the graph into its biconnected components greatly reduces the mapping complexity. The minimal guard set algorithm finds all possible combinations of vertices to guard. If these guard sets are optimal, it can then be determined what the maximal voltage is that can be applied to a net.

Tests in a pre-defined library of tests can be mapped onto the structures in the DUT. These tests specify a so called mold, which determines what kind of structure can be covered by that test. As soon as mapping procedure continues, Structures not covered by a tests are then handed by the generic test method. By utilizing the PCOLA-QSQ properties the effectivity of a proposed test can be optimize and guaranteed, and superflous tests are automatically removed.

Future work entails adding support for: (1) active component, (2) shorts testing, (3) automatically selecting the most stable test.

### References


