Challenges in testing TSV-based 3D stacked ICs: test flows, test contents, and test access

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Challenges in Testing TSV-Based 3D Stacked ICs: Test Flows, Test Contents, and Test Access

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Abstract

Three-dimensional stacked ICs (3D-SICs) based on Through-Silicon Vias (TSVs) have many attractive benefits and hence are quickly gaining ground. Testing such products for manufacturing defects is still fraught with many challenges. This paper provides an overview of those challenges and their emerging solutions, categorized in the areas of (1) test flows, (2) test contents, and (3) test access.

1 Introduction

Vertical stacking of multiple integrated circuits offers dense integration of possibly heterogeneous technologies with a small area footprint. The semiconductor industry is preparing itself now for vertical interconnection of multiple stacked tiers by means of TSVs [1–3]. In comparison to conventional wire-bonded interconnects, TSVs promise to increase the interconnect bandwidth and performance while lowering power dissipation and overall manufacturing cost. Consequently, TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities [4, 5] and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

A lot of research and development work has been done, is being done, and still needs to be done to enable TSV-based 3D integration. One of the first challenges to be addressed was the development of processing recipes to be able to manufacture TSVs. Typical TSV dimensions are 5 μm diameter and 50 μm height (see Figure 1). Etching and properly filling TSVs with such a large aspect ratio is not an easy task [6, 7]. A normal wafer is much thicker than the TSV height, and hence the wafer needs to be thinned down to make the TSV extend out of the wafer's back-side to connect to the next tier. Wafer thinning and thin-wafer handling [8], back-side processing, bonding [9, 10], and packaging of die stacks are also on the list of technology challenges. To be able to monitor the processing, in-line inspection [11], metrology [12], and failure analysis tools need to be upgraded to cope with this new type of circuits.

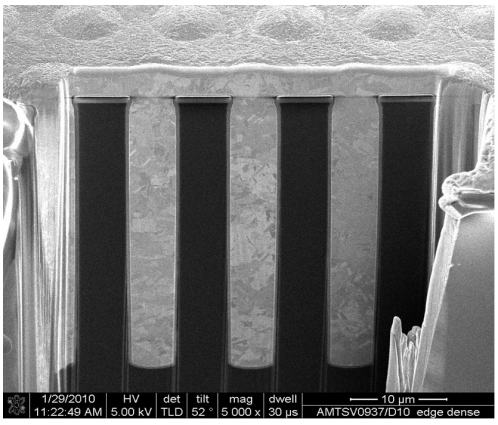


Figure 1: Cross-section photo of Through-Silicon Vias with aspect ratio 10:1.

Research and development work on 3D integration also addresses design issues. The impact of 3D processing on the operation of the circuit needs to be assessed and compensated for [13, 14]. This includes the effects of TSV proximity on transistors and metal interconnect, mechanical stress and warpage (especially of thinned wafers), thermal stress (as the vertical stack might block heat dissipation) [15], etc. New design methods and software tools need to be developed that handle 3D designs [16, 17], from high-level architectural trade-offs including hardware-software co-design, down to three-dimensional transistor netlist and layout [18].

Like all ICs, these new TSV-based 3D-SICs also need to be tested for manufacturing defects, in order to guarantee sufficient outgoing product quality to the customer. Whereas 3D-SICs require most of today's advanced test and Design-for-Test (DfT) approaches, simply because they are composed of advanced IC designs in advanced technology nodes, they also have some unique test challenges of their own [19, 20]. These challenges pertain to (1) test flows, (2) test contents, and (3) test access. This paper provides an overview of these challenges and their solutions, to the extent that they already exist.

2 3D Test Flows

Most conventional single-die chips have a test flow consisting of two tests: a *wafer test* and a final *packaged test*. The test flow for 3D-SICs is potentially a lot more complex; their manufacturing process consists of many more steps and hence has many more potential natural test moments. As shown in Figure 2, we distinguish between (1) *pre-bond die tests*, (2) *post-bond stack tests*, and (3) *packaged tests*. Pre-bond and post-bond tests are both wafer probe tests; we distinguish between them, as they are distinctly different in their purpose, test contents, and test access.

In a dis-integrated production flow, intermediate products which are building blocks for one company, are final products for another company. For example, DRAM dies to be stacked on top of logic dies are intermediate products in view of the overall stack, but are final products for the DRAM maker. In such a setting, the supply contract typically requires that the intermediate products (DRAMs, in our example) are tested with final-test quality, including at-speed and burn-in tests. The delivered products are termed *Known-Good Dies* (KGD) [21], or, in case of die stacks, *Known-Good Stacks* (KGS) [20].

In an integrated production flow, where absolute KGD/KGS quality is not required, the test coverage and quality for intermediate products becomes

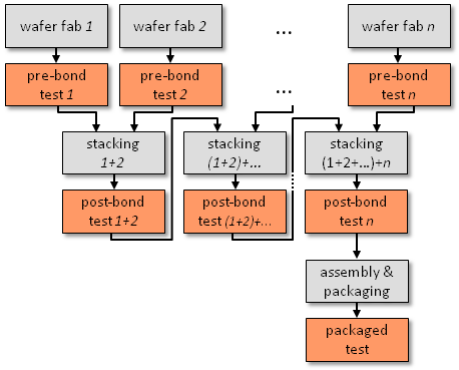


Figure 2: Overview of potential 3D test flows.

an economical optimization criterion, governed by the following cost-benefit trade-off [20]:

$$(1 - y) \cdot d \cdot p > t \tag{2.1}$$

where

- y is the fabrication yield,
- d the detectable fraction of faulty products given a particular test
- p the preventable costs per product, and
- t the cost of executing that particular test on a single product.

Yield y is a complex product of die yield, TSV yield, bonding yield, and packaging yield. Parameters d and t are interrelated and both determined by the test coverage and quality; a better, more comprehensive test is able to filter out more faulty parts, but will typically also be more expensive to execute. The preventable product costs p depend on the moment in the production flow at which the test is carried out; the earlier in the flow a faulty part is detected, the more wasted costs can be prevented downstream. For example, a bad die which is detected during pre-bond testing can be excluded from further stacking and packaging, and hence saves wasting other good dies and a package. If that same bad die is not detected during pre-bond testing, but only during post-bond testing, the good die(s) that is (are) already stacked to it, will be wasted, and only downstream packaging costs can be prevented. Preventable product costs p also depend on the stacking approach. In the case that individual dies are stacked (in Die-to-Wafer (D2W) or Die-to-Die (D2D) stacking approaches), pre-bond test results can be utilized to avoid stacking good to bad die or vice versa. This is different in a Wafer-to-Wafer (W2W) stacking approach, where one cannot avoid stacking an individual bad die. However, pre-bond die test results can still be exploited to achieve limited stack yield increases by means of wafer matching on the basis of the wafer maps of repositories of pre-tested wafers [22, 23].

Only if the yield of a die is sufficiently low and the cost of the other die(s) in the stack is sufficiently high, *pre-bond testing* for that die pays off. In that case, are we only testing the regular circuitry in the die, or do we also want to include tests for (1) TSV defects and/or (2) 3D processing steps such as wafer thinning? Testing for TSV defects on not-yet-thinned wafers requires dedicated DfT and test methods, as one side of the TSV is still buried in the thick substrate [24–26]. Testing through TSVs and testing for wafer thinning defects as part of the pre-bond die test requires wafer probe access on thinned wafers, which brings about a whole new set of challenges as outlined in Section 4.1. The cost/benefit trade-off of performing all these tests during pre-bond testing has to be balanced against testing for these defects as part of the post-bond stack test, which is typically easier and more complete, but later in the flow. Early studies show that some form of pre-bond testing pays off in many practical cases [20, 27].

Post-bond tests can be carried out on both partial stacks and/or the final stack. The more complete the stack, the smaller the preventable product costs p; for the final stack, only the packaging costs can be prevented. Important while determining the contents of a post-bond test is to determine what has already been tested before (in preceding pre-bond or partial post-bond tests) vs. what is still untested circuitry. It seems obvious to focus on the latest inter-die connection which obviously is still untested, but if stacking operations can cause new additional defects, re-testing already tested circuitry might pay off too [27].

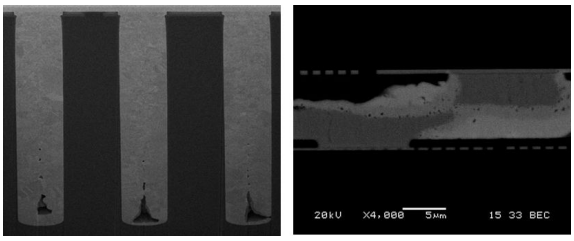
Note that the economic test optimization for intermediate products described above does not affect the outgoing product quality of the final packaged product, under the assumption that the final packaged stack is thoroughly tested, independent of choices for pre-bond and post-bond test. Also note that the cost-benefit trade-off offered by all these wafer test options should by no means be considered static. A typical manufacturing process matures during the life-time of a product, allowing for cost reduction by omitting certain tests on intermediate product stages.

3 3D Test Contents

For 3D-SICs, the majority of conventional wafer processing steps remain intact, and hence their defects and fault models are what we are used to from (advanced) ICs, and the corresponding test contents is 'business-as-usual'. New test content is to be expected for (1) the TSV-based interconnects, which form an entirely new structure, and (2) new intra-die defects due to new additional 3D processing steps.

3.1 Test of TSV-Based Interconnects

TSV-related defects might occur either in the fabrication of the TSV themselves, in the bonding of the TSVs to the next tier, or during the life time of the 3D stack. During the fabrication of TSVs, (micro-)voids, for example due to quasi-conformal plating, might lead to (weak) opens in TSVs (see Figure 3(a)). Pinholes in the TSV oxide might lead to shorts between TSV and substrate. Ineffective removal of the seed layer might lead to shorts between TSVs. The bond quality might be negatively impacted by oxidation or contamination of the bond surface, height variation of the TSVs, or particles in between the two dies. Mis-alignment during bonding, in either x, y, or (tilted) z direction, might lead to opens or shorts (see Figure 3(b)). In case of Cu-Sn micro-bumps, the tin might squeeze out due to TSV height variation and cause shorts in between them.



(a) (b)

Figure 3: Examples of interconnect defects: (a) TSVs containing micro-voids, and (b) mis-aligned micro-bumps.

Once the interconnects are formed, they actually serve as 'wires' between two tiers. From board-level interconnect testing, there is a large body of existing work with respect to test pattern generation [28] which we can leverage, such as the Counting Sequence Algorithm [29], the Modified

Counting Sequence Algorithm [30], and the True/Complement Test Algorithm [31]. These algorithms detect all (hard) open and shorts through a set of digital test patterns that can be kept small, as it grows only logarithmically with the number of interconnects. This is an attractive feature, as the number of TSV-based interconnects is potentially very large. The test algorithms rely on the presence of full controllability respectively observability at all interconnect inputs respectively outputs; this requirement is fulfilled by the DfT architecture described in Section 4.2.

Open challenges with respect to testing TSV-based interconnects are the detection of weak defects and timing faults, defects in 'infrastructure' TSVs (power, ground, clocks), and the implementation of effective and efficient redundancy and repair resources [32].

3.2 New Intra-Die Defects

An important question is whether the 3D processing steps induce new intra-die defects, of which the corresponding fault behavior is not covered by conventional tests. If that is the case, new fault models and tests will need to be added to the existing test suite.

Wafer thinning is one such 3D processing step that can cause new defects. The TSV processing only allows for limited TSV heights (say, 10 to 100μm) and aspect ratios (say, 10:1) [6]. In order to expose the TSV tips at the back-side for bonding to another die, the wafer needs to be thinned down. This is an area for further research; early results indicate degradation of some *I-V* characteristics, shifts in device performances, and limited yield losses due to wafer thinning [33, 34].

Thermal dissipation and thermo-mechanical stress are other causes of concern. Integrated circuits heat up during operation. In densely packed stacks of thinned dies, the heat density might pile up quite high, and has little way of escaping. The heat generated might easily impact the correct operation of the various dies, especially since some dies are more heat-sensitive (e.g., DRAMs) than others. Due to the different Coefficients of Thermal Expansion (CTEs) of the various materials in the stack, the stack might also suffer from thermo-mechanical stress, causing further malfunction.

4 3D Test Access

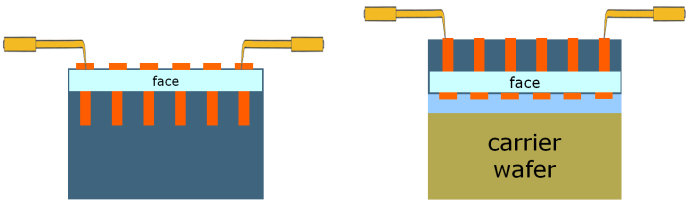
Test access deals with delivery of test stimuli and responses from the test equipment to the appropriate Circuit-Under-Test (CUT) and vice versa. Test access is different for pre-bond and post-bond testing. In this section, we subsequently discuss the test access challenges (1) from the test equipment to the chip I/Os and back through wafer probing and (2) from the chip I/Os into the CUT and back through on-chip DfT.

4.1 3D Wafer Probe Access

In *pre-bond* testing we need to probe the individual dies. For the die holding the external I/Os (such as wire-bond or flip-chip pads) – this is typically the bottom die – this is 'business-as-usual'. However, the other (non-bottom) dies receive all their functional signals (for power, ground, clocks, control, data) through TSVs. These TSV-based I/Os are typically too small, too dense, too fragile, and too numerous to be probed with conventional probe technology. Today's probe technology, using either cantilever or vertical probes, goes down to a minimum pitch of 35μm [35], has a maximum probe count of several thousands, and makes significant scrub marks in order to achieve a proper electrical contact. Today's TSV-based I/Os are denser than that and continue to scale down. The most relaxed TSV bonds are based on Cu-Sn micro-bumps [36], but have already achieved pitches of 20μm. Direct Cu-Cu TSV bonds have TSV tips of 5μm diameter and 10μm pitch, which might come in many thousands (the 10μm pitch allows TSV densities up to 10k/mm^2), are made of fragile copper, and do not tolerate scrub marks that inhibit downstream Cu-Cu bonding on the same surface.

Until probe technology makes a significant improvement in scaling down the pitch, increasing the probe count, and reducing scrub mark damage (possibly through contactless probing [37]), the only solution to enable pre-bond testing is to equip the non-bottom dies with additional probe pads, sized such that today's probe technology can handle them. This comes with an area penalty, and hence the number of extra pads should be minimized; on-chip DfT such as Reduced Pin-Count Testing (RPCT) [38] can help with this.

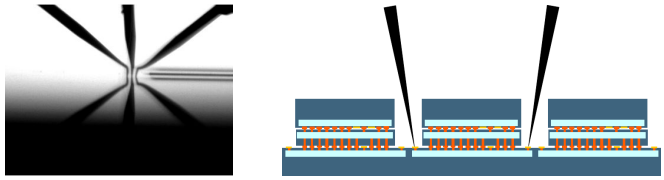
For pre-bond testing, we have two options for wafer probe access: probing on a not-yet-thinned die, or probing on a thinned-down die. Figure 4(a) shows front-side probing of a not-yet-thinned die. This has as drawback that the TSVs are still buried in the thick substrate and hence can only be accessed from one side, which constraints their test possibilities [24–26]. Thinning defects are not covered in this stage, as the wafer is not thinned yet. Figure 4(b) shows probing of a thinned-down die. The thinned wafer is mounted on a temporary carrier wafer for mechanical strength. This implies that the front-side is inaccessible for probe needles, and probing can only be done at the back-side. Potentially, we can now test through the TSVs and also cover wafer thinning defects, but back-side probing of a thinned wafer on carrier is still fraught with challenges with respect to probe damage.



(a) Front-side on thick wafer (b) Back-side on thinned wafer

Figure 4: Pre-bond wafer probe options on (a) a thick or (b) a thinned-down die.

In *post-bond* testing, the wafer test access is typically through the regular functional (wire-bond or flip-chip) pads of the bottom die of the stack. This is largely 'business-as-usual' as far as probe technology is concerned. The challenges for post-bond stack testing are in the wafer handling within the probe station, especially in the case of D2W stacking. On top of the bottom wafer, stacks consisting of one or multiple dies stick out. If that top side is the probe side of the wafer, the stacks might obstruct the probe station's contact view, making probe needle positioning difficult (see Figure 5(a)). Also, during probe needle movement, we need to make sure that the needles do not collide with the stacks (see Figure 5(b)). On the other hand, if we probe on the bottom side of the wafer, the stacks create a very non-planar surface, which is difficult to keep stable on the chuck.



(a) (b)

Figure 5: Wafer access challenges for post-bond stack test: die stacks (a) obstructing the contact view (here: top die is only 25 μm), and (b) the probe needle movement.

4.2 3D Design-for-Test Architecture

In [39, 40], a 3D DfT architecture is proposed that supports (1) pre-bond die testing, (2) post-bond stack testing (of both partial and complete stacks), and (3) board-level interconnect testing. This architecture is depicted in Figure 6. On top of the conventional die-internal DfT (such as scan chains, Test Data Compression, BIST, JTAG, etc.), the key component in this architecture is a test wrapper per die. This wrapper is based either on IEEE Std 1500 or on IEEE Std 1149.1 and has the following features: (1) a serial (one-bit) and scalable parallel (n-bit) test access mechanism, (2) *TestTurns* from and to the stack's external I/Os, (3) additional probe pads for all non-bottom dies allowing for pre-bond testing, (4) *TestElevators* that carry test data up and down through the stack in post-bond testing, and (5) a hierarchical instruction register chain that prevents unbridled growth of the test instruction sequences.

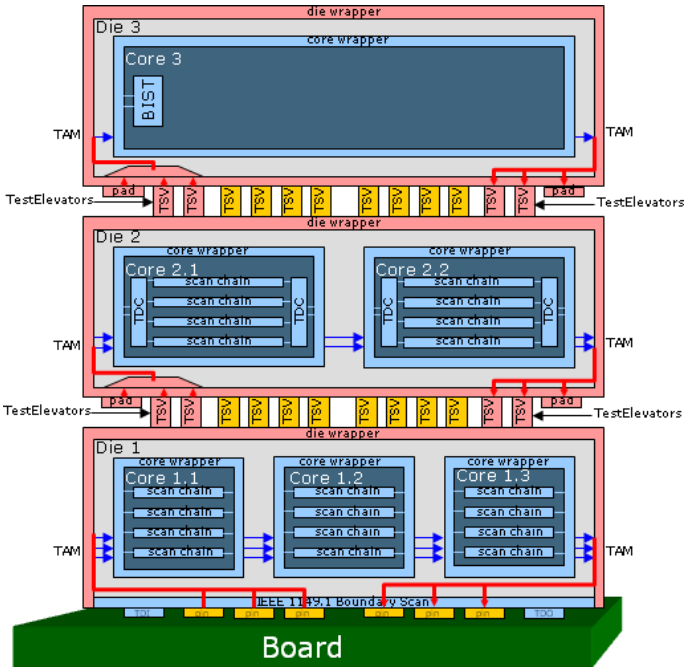


Figure 6: Overview of a 3D DfT architecture based on die-level wrappers.

5 Conclusion

Like all ICs, 3D-SICs also need to be tested for manufacturing defects. 3D-SICs require most of today's advanced test and DfT approaches. In addition, they have some unique test challenges of their own.

A 3D *test flow* contains many more potential wafer test moments and hence requires more complex, cost-benefit trade-offs that might evolve during the maturization of the production process. With respect to 3D *test contents*, the TSV-based interconnect is a new structure causing defects, for which open/short faults can be covered with an effective and efficient digital 'counting' test. New intra-die defects caused by 3D processing steps such as wafer thinning are another cause of concern, particularly if conventional test sets would not cover them. For 3D *test access*, there are two categories of challenges. Wafer probe technology is not fully ready yet for TSV-based 3D-SICs. Inside the dies, DfT architectures are being defined that transport test signals up and down through the stack.

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