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Silicon Interposer Based QSFP-DD Transceiver Demonstrator with >10 Gbps/mm^2 Bandwidth Density

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Abstract *Through a single optical interface, a 250 µm pitch two-dimensional 2×8-channel optical transceiver is integrated on a lithographically patterned silicon interposer, offering 200 Gb/s data input and output duplex within an area of 6 mm × 6 mm.*

Introduction

Presently, the demand of data communication is increasing in an unprecedented rate. Supported by ever more optical interconnects, data centres are scaling up with a factor of 1000 every 10 years, and optical transceivers are evolving to deliver higher radix and higher bit rates [1]. Meanwhile, as the performance of integrated circuits (IC) improves, off chip interconnections become a limiting factor, since both data rate and pin counts reach their limit in the current electronic package [2]. Optical access for off-chip data communication may be a solution, as long as small form factor transceivers can be offered. To achieve high radix, high bit rate as well as small form factor, opto-electronic packaging is the main challenge, a holistic consideration on both electrical and optical interfaces is necessary.

Comparing with wire bonding for electrical interconnects, flip chip bonding can be used to connect with the designed circuitry, and the resulting assembly can be much more compact, achieving near chip size package. Besides, flip chip bonding features improved RF performance, with low reflections and losses [3].

Silicon carrier has been demonstrated to poses good properties such as CMOS technology compatibility, high thermal conductivity and similar coefficient of thermal expansion (CTE) with chips. In [4] proposed transceivers are based on an active CMOS carrier. However, extra processes of optical vias occupy a lot expensive area of CMOS and lead to a lower yield. Passive silicon interposers can be fabricated through back-end-of-line (BEOL) processing to achieve a lower cost. However, in the scheme [5], complex optical and electrical through silicon vias (TSV) delay its introduction into high volume manufacturing.

Standard optical interfaces, PRIZM® light turn system, for chip access only support up to 12 channels, which is a limit for higher radix and high bandwidth density. (The light turn system takes around 1 cm^2, for instance.) To couple more light channels in a small area, a single connector for all channels is required.

Silicon interposer with one layer electrical interface and low cost optical TSVs has been developed for a chip scale transceiver demonstration, which will definitely enable the step-forward into cost-effective transceiver sub-modules [3]. Recently, we have demonstrated the high potential of the 2D assembling scheme by using a single optical interface, working at 10 Gb/s [6].

In this paper, an ultra-compact concept 2 × 8-channel bidirectional transceiver, using four pairs of 25 Gb/s chip sets and decoupling capacitors, is proposed for the emerging 200 and 400 Gb/s application code. We assemble a complete duplex 200 Gb/s transceiver with 8 × 25 Tx & Rx channels and show excellent performance of complete platform. This silicon based transceiver features an extreme small form factor and PRIZM® MT ferrule compatibility, and shows high potentials in chip to chip interconnections.

Scheme of the Assembly

Figure 1 and 2 offer a side view and top view images, and demonstrate of the fully assembled sub-module.

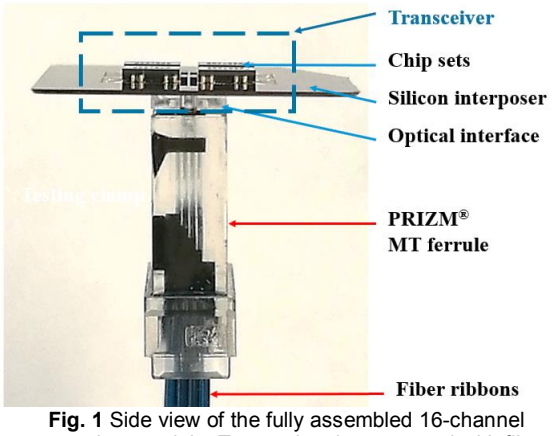

Fig. 1 Side view of the fully assembled 16-channel transceiver module; Transceiver is connected with fiber ribbons through OI.

The lithographically patterned passive silicon interposer provides the optical vias and metal traces used for the full assembly of the BiCMOS

[7] and optoelectronic GaAs dies [8]. Four optical arrays are aligned back to back to create a 2 × 8-channel optical inputs/outputs (I/O) with a pitch of 250 µm, by using the outside 8 channels, available in a 2 × 12-channel MPO connector. Four BiCMOS ICs are placed closely to the optics through coupled electrical traces (see Fig. 2). In addition, the silicon interposer is also designed to enable the placement of decoupling capacitors for power rails filtering. A robust single optical interface is attached at the backside of silicon, to couple all the channels with standard fibre ribbons through PRIZM® MT ferrule.

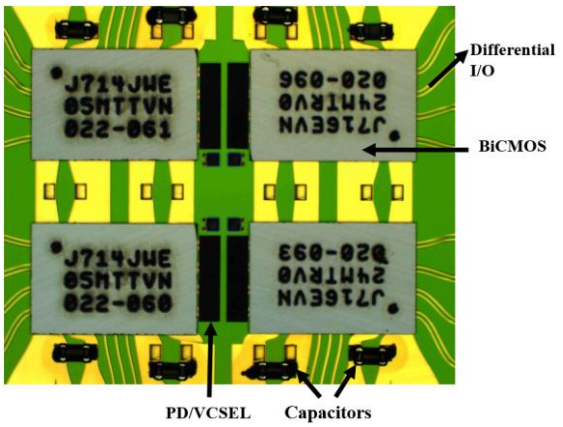

Fig. 2: Top view of the transceiver assembly on a silicon interposer, including four pairs of flip-chip bonded optical arrays and BiCMOS ICs. In total, eight capacitors are assembled.

In addition, the electrical I/Os are fan out to the edge of the silicon interposer for further connection to standard 1D 250 µm pitch. The form factor of the assembled sub-module is only 6 mm × 6 mm, and 1. 2 mm thick. To realize the optical interface, we employ the light coupling mechanism between two PRIZM® MT ferrules, for ease of alignment. Optical interface (OI) is realized in 3 mm × 6 mm, which connects with its mated ferrule. The thickness of OI, which is adjusted to fit the silicon interposer and get the best light coupling out, is only 0.7 mm. Previously, we have demonstrated the capability of this platform to support up to 4 rows of optical channels [6]. Together with this OI concept the interposer platform can be scaled up to support up to 4 × 16 optical channels.

Fabrication and Assembly

A cleaved 1-inch silicon sample is used to demonstrate a wafer level fabrication process. In order to optimize the distance between optics and OI, the wafer is thinned down to 180 µm in KOH solution. After that, a metal layer is sputtered on top of deposited silicon nitride mask (SiN_x, 200nm thick). Only one step of photolithography is performed for opening of the traces for electro-plating. Another plating is followed using the same seed layer, for bump formation. The optical TSVs are made by double side silicon etching, with the square openings for each channel. At same time, cleaving lines are also etched.

After processing, the silicon interposer is easily cleaved thanks to the cleaving lines. The micro image in Fig. 3 shows the coupled trace for the connection between optics and electronics. The length is shortened to less than 250 µm. Besides, traces are tightly coupled and impedance matched with TIA input/VCSEL load, for the purpose of minimum crosstalk and reflection.

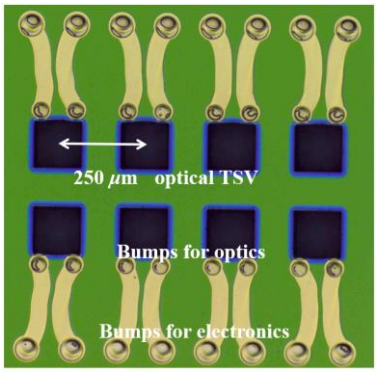

Fig. 3: Tightly coupled and extreme short electrical connections between optics and electronics on silicon, and wet etched optical vias (square openings) for each channel. The green color indicates 220 nm thick SiN_x on top of silicon.

Photonics and electronics dies are flip chip bonded with a die bonder. After a heat reflow (270 °C), the gold pads on the optics and the plated bumps on silicon interposer are connected. Two VCSEL arrays and two PD arrays are aligned one by one. The micro photo is taken from backside. For alignment check. After that, 4 BiCMOS ICs are also reflowed (230 °C) on the die bonder. Finally, the fabricated OI, is mounted at the backside of silicon interposer by epoxy (60 °C). Figure 1 and 2 shows the complete transceiver module, on the silicon interposer, taken under microscope.

Fig. 4: Micrograph taken from the interposer's backside, the apertures of the PD/VCSEL can be seen through OTSVs.

Experimental Results

For characterization the assembled transceiver is connected via a standard PRIZM® MT ferrule with the OI through the guiding pins. An MPO to LC pairs break up cable allows for access to single channels. A commercial QSFP28 module is used as a high speed light source/photo detector.

A 25.7 Gb/s non return to zero (NRZ) with a 2^{31}-1 pseudo random bit sequence (PRBS) signal is fed by multiple differential RF probes (signal-signal) through fan-out pads of the silicon

interposer of each channel.

In the transmitter (TX) test, the converted optical signal is detected by a QSFP28 module through the fan out LC fibre. The eye patterns of the electrical output from the QSFP28 is captured by an oscilloscope. While in the receiver test, the optical signal, with 25.7 Gb/s 2^{31}-1 PRBS sequence, is detected. The differential electrical outputs, with pre-emphasis enabled, are displayed on the oscilloscope. The excellent testing results of all channels are shown in Fig. 5, without using the clock data recovery (CDR) function on the assembled ICs to enable lower power consumption. All channels are working uniformly, and eye patterns are clearly open.

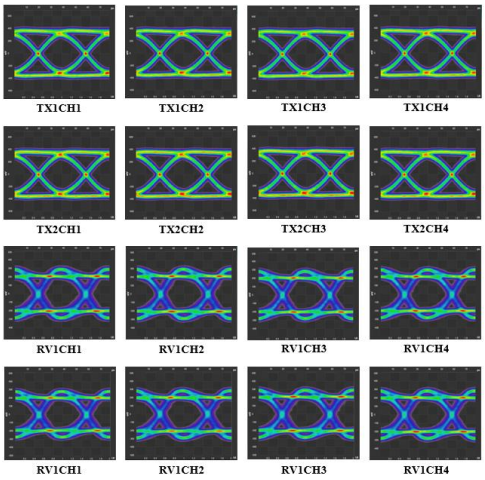

Fig. 5: Eye patterns of 2 × 4-channel transmitter (TX) and 2 × 4-channel receiver (RV).

Receiver sensitivity is also tested for BER at 25.7 Gb/s PRBS 2^{31}-1. The optical power is calculated from the photo current detected by each photodiode via the BiCMOS ICs. The receiver sensitivity curves of 2 × 4-channel receivers, are shown in Fig. 6, left. All channels are working error free (10^{-12} level) with optical power of -6 dBm, with the spread only 0.6 dB.

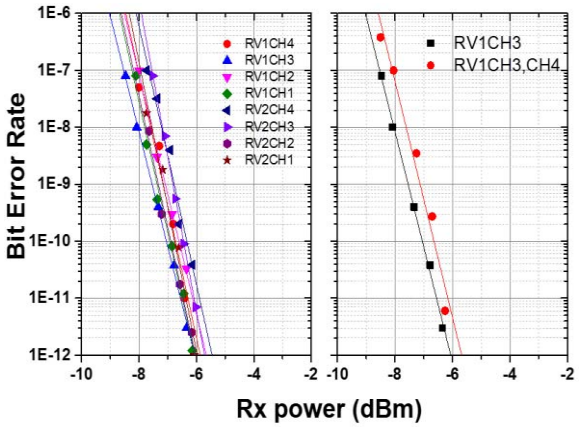

Fig. 6: Left: BER curves of all receiver channels. Right: Crosstalk penalty, characterized by BER curve of CH3, working alone and together with CH4.

In addition, optical power crosstalk to adjacent channel is measured to be below -40 dBm. The effect of electrical channel crosstalk is also characterized by testing the penalty at the receiver. Two adjacent channels of RV1 (CH3, CH4) are fed with 25.7 Gb/s optical signals simultaneously, and BER curves of CH3 operating alone and together with CH4 are measured (see Fig. 6, right). Minimal crosstalk is measured (<0.4 dB).

Conclusions

In this work, we integrate an ultra-compact transceiver with four pairs of electrical and optical dies. The extreme short electrical connection is designed as coupled traces. The pitch of 2D optical ports is 250 µm in both x, y directions, and 16 lanes are used for a duplex 200 Gb/s QSFP-DD assembly. A single compact optical interface is employed for optical access within an area of 3 mm × 6 mm, enabling up to 64 lanes.

During performances testing, clear eye patterns for all the 16 channels are captured at 25.7 Gb/s. The uniform BER curves of receiver channels and small crosstalk effect are also measured. The excellent testing results indicate that higher data capacity can be easily achieved on this platform, if PAM modulation or more channels are used.

Acknowledgements

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