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A Compact 10b SAR ADC with Unit-Length Capacitors and a Passive FIR Filter

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Abstract—This paper presents a compact 10b SAR ADC in 65nm CMOS with an integrated passive FIR filter for anti-aliasing. Conventional switched-capacitor DACs are usually implemented with unit elements for best matching performance, at the cost of increased chip area. Instead, this work proposes a unit-length capacitor implementation, which minimizes the number of components and thus minimizes area, while also achieving good linearity (INL of 0.39LSB, DNL of 0.55LSB, and SFDR of 75dB) despite using a small LSB capacitor of 125aF. The 10b SAR ADC occupies only 36×36µm, thanks to the small-size DAC, and by placing the ADC circuits directly under the capacitors. The ADC was tested at 10MS/s and 30MS/s, and achieves an ENOB of 9.18/9.10bit with a FoM of 4.1/4.4fJ per conversion-step, respectively. Besides the ADC, a passive analog FIR filter is added to implement an anti-aliasing filter. The topology is based on a passive charge-sharing network, and thus only consumes power for the clock phase generation and switch drivers. A 4× time-interleaved 15-tap passive FIR filter is implemented, which can realize >42dB out-of-band rejection and 4× decimation, while occupying only 53×90µm. The filter and ADC together consume 39.2µW for an output rate of 10MS/s.

I. INTRODUCTION

SAR ADCs have become very popular in the last decade for a large range of applications, from low-power sensor interfaces to wireless receivers and high-speed communication standards [1]. Particular advantages are the excellent power-efficiency, relatively simple design and portability to newer technologies. However, SAR ADCs require a relatively large chip area, and they usually require an external anti-aliasing filter. In this work, as an extension from [2], a prototype ADC is presented that alleviates these disadvantages.

In terms of chip area, a SAR ADC is usually limited by the size of the switched-capacitor DAC. Because both the total capacitance and the number of capacitors grows exponential with the resolution N of the ADC, its area quickly dominates the entire ADC. Besides the obvious advantage that less area would reduce costs, it becomes especially essential in array-based interfaces where the available area per element is limited, for instance in phased array antennas or radar, image sensors, ultrasound imagers and neural interfaces. At present, the chip area of Nyquist ADCs with an SNDR of at least 50dB is usually beyond 100×100µm [1], unless advanced technologies (≤28nm) are used. This area is too large to enable for instance pixel-level integration of ADCs in ultrasound arrays. The use of a split capacitor array [3] or multiple layout units [4] can reduce area, but at the cost of linearity. Alternatives using hybrid DACs or charge injection cells [5] have been proposed, but are not yet competitive in performance to regular capacitor-based SAR ADCs. Therefore, instead of proposing an entirely new architecture, this paper preserves the well-established switched-capacitor topology, but proposes a new capacitor layout technique to save chip area. Instead of using unit capacitor cells which are area inefficient, this work uses unit-length scaling. This results in a regular layout structure characterized by accurate matching and a small chip area. The implemented 10b SAR ADC occupies only 36×36µm, has an LSB capacitance of only 125aF, and nonetheless achieves an ENOB of 9.18b at 10MS/s while consuming 24µW.

In terms of filtering, a SAR ADC is a Nyquist converter and thus requires an external anti-aliasing filter, as opposed to for instance Delta-Sigma Modulators. This filter is not only required to suppress out-of-band interferences, but also to minimize the noise bandwidth before sampling takes place. Conventionally, an active filter can be placed in front of the ADC. However, this costs additional power. Alternatively, analog switched-capacitor filters can be integrated inside a SAR ADC [6], [7]. While it is conceptually attractive to reuse the SAR ADC capacitors as the filter capacitors, it results in a relatively complex switched-capacitor network, which moreover cannot be integrated with the capacitor layout proposed in this work. Therefore, this work proposes a standalone analog passive FIR filter, the output of which is sampled by the ADC by means of charge sharing. By separating the filter and ADC functions, they can be designed independently, and the implementation becomes more simple. The FIR filter has 15 taps and offers 42dB out-of-band rejection while consuming 15.2µW.

The organization of this paper is as follows: Section II discusses the new DAC layout technique, while Section III introduces the passive FIR filter. Measurements are given in Section IV and conclusions are drawn in Section V.

II. UNIT-LENGTH DAC LAYOUT TECHNIQUE

This section first reviews the common approach for implementing an accurate binary-scaled capacitor-based DAC by means of unit elements. Next, the proposed approach is presented and analyzed in general. The section is concluded by presenting the detailed implementation of a 10b DAC using the proposed method.

A. Conventional approach: unit-element capacitors

The conventional approach to implement an N-bit capacitive DAC for a SAR ADC is to implement $2^N - 1$ unit
capacitors, and to group these in binary-scaled sets to create the DAC. The unit-element approach is well established, as it ensures correct capacitor matching. An example for a 3b DAC (with 7 unit elements) is sketched in Fig. 1, where the units are made with finger capacitors [8]. To minimize power consumption and chip area, ideally one would like to minimize the size of the unit capacitor towards the fundamental noise limit, ignoring mismatch for the moment, since that is not a fundamental limit. For example, for a 10b ADC with 1V signal swing, a unit capacitor of 125aF is sufficient to meet the kT/C sampling noise requirements. However, it is not straightforward to implement this, and therefore most ADCs are oversized, leading to an increase of power consumption and chip area. In order to get closer to the fundamental limit, there are several challenges to deal with: first of all, a custom capacitor layout should be developed to reach this small value in the first place. Secondly, the capacitor mismatch needs to be improved, otherwise such small unit will not achieve sufficient linearity. Lastly, as Fig. 1 already shows, once the capacitor size is small, the interconnect starts to become important for the overall area and also increases power losses. For instance, the differential 10b array of 250aF unit capacitors in [9] occupies 115×80µm in 65nm CMOS. From this area, only 15% is effectively used by the capacitors while the remaining 85% is used for interconnect, dummies, and spacing. In [10], an entire 10b SAR ADC is made in only 33×35µm using an advanced 20nm CMOS process, and an area efficient binary-scaled DAC based on unit elements is implemented, but the achieved total area would become much larger when ported to an older technology node. Overall, the binary-scaled array based on unit elements is not able to reach the capacitor noise limit in an area-efficient and power-efficient manner, in particular when older technology nodes (>28nm) are used.

B. Proposed approach: unit-length capacitors

To overcome the limitations discussed in the previous paragraph, not only the capacitor value but also the amount of interconnect should be minimized. This is done by using a unit-length rather than a unit-element approach. It is known that changing the length of a metal strip will change its capacitance, and it is also known that this relation is not accurate, since edge effects do not scale with the length. To solve this, the length difference between two strips rather than the absolute length of a single strip is used to define the capacitances. In this way, edge effects are compensated thanks to subtraction, and accurate scaling of the effective capacitance proportional to the length difference can be achieved. Fig. 2 shows an exemplary sketch of the new DAC layout for a 3b converter, together with a schematic model. Six relevant capacitors are formed, each from an input node to the shared output node of the DAC. Each DAC bit \( i \) drives two capacitors \( C_i \) and \( C_i' \) that are both coupled to the DAC output but with opposite control polarity. For instance, the LSB \( b_0 \) drives both \( C_0 \) and \( C_0' \), but with opposite signals \( b_0 \) and \( \overline{b_0} \). That implies that if \( C_0 \) and \( C_0' \) would be equal, their impact on the output voltage would cancel out when switched. However, by making the metal of \( C_0 \) an amount \( \Delta \) longer and the metal of \( C_0' \) an amount \( \Delta \) shorter than their average, the effective capacitance is determined by the total length difference \( 2\Delta \). A binary-scaled array can now be made by scaling \( \Delta \) in binary steps as shown in Fig. 2. Thus, \( 2^N \) capacitors are sufficient to build the DAC instead of \( 2^N - 1 \). Note that systematic capacitance errors, such as caused by the vias or the metal strip ends are compensated by the oppositely switched element. Therefore, accurate binary scaling can be achieved. Moreover, the regular layout pattern with constant metal density is less likely to suffer from systematic mismatches. Since \( \Delta \) can be set with fine granularity (for instance 5nm steps in 65nm CMOS), very small effective capacitors can be designed. A further advantage is that it is now possible to design matched capacitors that are non-integer multiples of each other. E.g. if the smallest capacitor has \( \Delta = 1\mu m \), one can not only design capacitors of \( 2\Delta, 3\Delta, \ldots \), but also for instance \( 1.2\Delta = 1.2\mu m \), with an equally good matching. This is different from the unit-element approach, where only integer multiples of the unit can be implemented accurately, as fractional units introduce systematic mismatch.

In practice, it is not convenient to scale all \( N \) bits by means of \( \Delta \), as this would result in long metal strips of...
Moreover, this would also result in a large percentage of ‘negative’ capacitance ($C^\prime_i$), which is disadvantageous in terms of mismatch, noise, power and area. As a solution, the DAC can be segmented, where the LSBs are scaled using $\Delta$, and the MSBs use a unit-element approach. An example sketch of a segmented DAC (with 3b binary and 2b unary) is shown in Fig. 3. Within the 3b binary segment, good matching is achieved thanks to length scaling ($\Delta$, 2$\Delta$, 4$\Delta$). Within the 2b unary segment, good matching is achieved thanks to unit elements (either one element or two elements of 8$\Delta$). Matching between the binary and unary segments is also assured, as the unit element of the MSB array (8$\Delta$) is length-scaled by 2$x$ compared to the largest LSB element of 4$\Delta$. Thanks to segmentation, the form factor of the layout can be made more practical. Also note that the binary segment has a relatively large contribution of ‘negative’ capacitance, while the unary cells have very little ‘negative’ capacitance. Thus, by assigning sufficient bits to the unary segment, the amount of ‘negative’ capacitance can now be minimized.

All in all, the proposed layout technique from Fig. 3 has three benefits that help to minimize chip area: first, very small LSBs can be made thanks to using the length difference. This can reduce the total capacitance and thus reduces area for the MSB capacitors. Second, less components are needed as opposed to a binary-weighted array with unit elements, which also results in area savings. Third, the interconnect is more simple thanks to the lower component count, and can be placed under the capacitors such that it does not take extra area.

C. Signal-range, noise and mismatch analysis

The idea of ‘subtracting’ two large capacitors $C_0$ and $C^\prime_0$ to effectively create a small one has a negative impact on matching and noise. However, the level of impact can be controlled by segmentation as will be discussed in this section.

Assume the $N$-bit DAC is segmented in $N_b$ binary bits and $N_u = N - N_b$ unary bits. According to the model in Fig. 2, this implies there are in total $N_b + 2^{N_u} - 1$ elements, each composed of a $C_i$ and a $C^\prime_i$. Since $C_i + C^\prime_i = 2C_m$ and $C_i - C^\prime_i = C_{i,eff}$ with $C_{i,eff} = 2^i \cdot 2C_\Delta$ for $0 \leq i \leq N_b$, the total capacitance at the output node of the DAC $C_{tot}$ and the total effective capacitance $C_{eff}$ can be expressed as:

$$C_{tot} = (N_b + 2^{N_u} - 1)2C_m$$  \hspace{1cm} (1)

Further, if the unary cell is designed such that the entire length of the metal strip is used, it implies that its ‘negative’ capacitance $C^\prime_i$ is near zero, thus: $C_i = 2C_m - C^\prime_i \approx 2C_m$ and $C_{i,eff} = C_i - C^\prime_i \approx C_i \approx 2C_m$, with $i = N_b$. Hence:

$$C_{N_b,eff} = 2^{N_b}2C_\Delta = 2C_m$$  \hspace{1cm} (3)

With the above three equations, the ratio of $C_{eff}/C_{tot}$ can be expressed as a function of $N$ and $N_u$. From there, the impact on signal range, noise and mismatch can be determined.

As for any switched-capacitor DAC, the relative full-scale range $FS$ is given by the capacitive division ratio:

$$FS \propto \frac{C_{eff}}{C_{tot}}$$  \hspace{1cm} (4)

The full-scale goes to 100% if $C_{tot}$ equals $C_{eff}$, but will be lowered when the ‘negative’ capacitance increases, which happens for a higher number of binary bits $N_b$. The SNR (Signal-to-Noise Ratio) depends on the signal power, which is proportional to $FS^2$, and the noise power, which is proportional to $kT/C_{tot}$. Thus, while a larger $C_{tot}$ reduces the signal power, it also reduces the noise power, albeit not as fast. As a result, SNR gradually degrades with increasing $C_{tot}$ and thus also with increasing $N_b$:

$$SNR \propto 10\log_{10} \left( \frac{C_{eff}^2}{C_{tot}^2} \frac{kT}{C_{tot}} \right)$$  \hspace{1cm} (5)

In terms of mismatch, we analyze the standard deviation of the DNL error for the mid-code transition, as this is usually the point with the largest impact from mismatch. At this code, all bits in the digital code toggle, and thus all capacitors are switching and contributing to the DNL error. Hence, the standard deviation of this DNL error is proportional to the square root of $C_{tot}$. When normalized to the LSB, which is $2C_\Delta \propto C_{eff}$, the penalty in mismatch can be expressed as:

$$\sigma \propto \sqrt{\frac{C_{tot}}{C_{eff}}}$$  \hspace{1cm} (6)

The impact on signal range, SNR and mismatch according to the above equations is visualized in Fig. 4 for a 10b DAC. The relative performance change is shown as function of the number of unary bits $N_u$. For high $N_u$, the full-scale and mismatch approximate 100% and the relative SNR is at 0dB, which means that the performance is equal to a conventional DAC design. When $N_u$ goes down and $N_b$ goes up, the performance gradually degrades. To take most advantage of the unit-length scheme while limiting the performance loss, a
compromise should be selected. For instance, for a segmentation with 6 binary bits and 4 unary bits, the full scale is reduced to 76%, the SNR is degraded by 1.2dB and mismatch impact is increased by 15%. These are relatively mild losses while the number of elements is reduced from 1023 to 42.

**D. Overall DAC and ADC implementation**

Based on the proposed scheme, a 10b DAC was implemented with 6 binary bits and 4 unary bits. Fig. 5 shows a detailed figure with all dimensions of the layout for each of the capacitors. Here, $\Delta$ is set to 200nm, a pitch of 500nm is used and metal layers 6 and 7 are stacked in parallel to increase the capacitor density, resulting in an effective LSBCapacitor of 125aF. In practice, the lowest two bits are not implemented as differential capacitors of $2 \times 125aF$ and $2 \times 250aF$. Instead, only single-ended elements with a double value (250aF and 500aF) are used. This gives the same differential voltage step, has negligible impact on performance, yet helps a bit more to reduce chip area and power losses. Since the capacitor layout is manually drawn, there is no mismatch data available prior to design. However, similar as in [8], it can be predicted that the matching is reasonably good for the small unit element, since the capacitor plate-to-plate distance $d$ of 130nm is relatively large, which results in a larger capacitor area which improves matching. Metal layers 4 and 5, which are directly under the capacitor array, are used to form a ground shield. The active circuits of the ADC (logic, comparator, S&H) and their interconnect are placed directly underneath the DAC. The capacitive structure is entirely drawn by hand, using regular metal layers. A normal parasitic-extraction tool is used to extract the actual capacitor values for verification. The total DAC capacitance seen at the output node is about 250fF of which 125fF is effective (determined by $C_{\Delta}$), while the remainder is due to ‘negative’ capacitance and parasitics to ground. This results in a signal range which is 50% of rail-to-rail. Overall, the 10b differential DAC array including dummy shielding takes less than $36 \times 36\mu m$. Besides a reduction of area for the capacitors, the proposed topology also saves area and power for the interconnect, since less wiring is needed and the wiring is short as the circuits are placed directly under the DAC. In comparison to the 10b binary-scaled DAC discussed earlier (Section II-A), this DAC occupies $7 \times$ less area, while it has the additional advantage that circuits can be placed underneath.

The overall ADC uses a relatively conventional design approach. As shown in Fig. 6, the differential input is directly sampled on the capacitive DAC. All bits are implemented differentially, except for the two lowest bits which are single-ended. The ‘negative’ capacitors $C'_i$ use the same control signals as the regular capacitors $C_i$, but inverted. Since all these signals ($b_i$ and $\bar{b}_i$) are already required for the regular capacitors, no extra logic or drivers are required for the newly added ‘negative’ capacitors. However, the extra load of approximately 20% more capacitance leads to a similar increase in driver strength, power, and area, but this adds only 1% to the total ADC power and 2% to the total ADC area according to simulations. A modified conventional switching scheme [8] was applied to the DAC to maintain a constant common-mode and to simplify the logic implementation. Moreover, this scheme requires only one reference level (equal to the supply) and ground. While in theory this scheme is not so power efficient, in practice this is not very important since the DAC power consumption is already very low thanks to the small capacitor values and short interconnect. A common asynchronous SAR architecture is re-used [9], and it requires no modifications to drive this DAC. The comparator uses the low-power topology from [11]. The ADC operates from a 1.0V supply, which is also used as the DAC reference voltage.

A more detailed view of the ADC layout is shown in Fig. 7. Seven out of nine available metal layers are used, where layer 1 to 3 are used for the ADC circuits, layer 4 and 5 form a ground shield above the active circuits, and the capacitive DAC is placed on top using metal layers 6 and 7. The capacitor elements are placed vertically, with dummies on the left, right and middle. The positive and negative half of the DAC are placed in a centrosymmetric fashion by mirroring and flipping the array of elements. Together with a shield around the perimeter of the DAC, the total size is $36 \times 36\mu m$. To connect the inputs of the DAC to the logic and the outputs to the comparator and S&H, small holes are made in the ground shield to allow vertical connections from the DAC to the circuits underneath. The shield cannot be made in one metal layer, as technology rules do not allow a single large piece of metal and DRC requirements would also require large holes within such a shield to make vertical connections. Therefore,
two layers of metal (4 and 5) act as shield, where alternating and overlapping narrow strips are used rather than one solid square.

III. 4× Time-Interleaved 15-Tap Passive FIR Filter

This section first reviews the various options for anti-aliasing in a digitization chain. After that, the proposed passive analog FIR filter is introduced and analyzed. The section concludes by discussing the final implemented circuit.

A. Anti-aliasing filter solutions

Fig. 8 shows several possibilities to implement an anti-aliasing filter, assuming 5MHz cut-off bandwidth. A high-order analog filter can be used, but this is power hungry and requires calibration to set the filter coefficients accurately. Alternatively, the analog filter can be relaxed or even omitted when the ADC is oversampled (e.g. 4×) and additional filtering and decimation is performed digitally. However, this increases speed and power for both ADC and digital circuits. A third solution is to implement an analog FIR filter prior to (or integrated with) the ADC. References [6], [7] re-use the DAC capacitors in a SAR ADC to implement an analog switched-capacitor filter prior to digitization. In this work, the filter capacitors and ADC capacitors are separated, since it simplifies the switching network and design procedure. Moreover, as very small capacitors are employed in this work, the penalty for not re-using the same capacitors is less relevant. An analog FIR filter will be implemented that performs steep filtering and decimation before the ADC, thereby relaxing the remaining analog filter requirements and reducing the ADC’s speed. The FIR filter works at 40MS/s (4× OSR) to reject frequencies beyond the signal bandwidth of 5MHz. Then, it decimates the analog data stream to 10MS/s prior to the ADC, which also operates at 10MS/s to correctly digitize the 5MHz signal band.

B. Proposed passive analog FIR filter

Fig. 9 shows the concept of a passive analog FIR filter, based on the charge-sharing principle. The example shows a differential implementation with \( k = 15 \) taps, where the output is also charge-shared with a SAR ADC. In total \( k + 1 = 16 \) clock cycles are required to produce one output sample: in the first 15 cycles (\( \varphi_0 \) to \( \varphi_{14} \)) the input signal is sampled on a set of capacitors (\( C_0 \) to \( C_{14} \)). The floating output nodes are shorted in phase \( \varphi_{14} \) to reset the differential output voltage. In the 16th cycle \( \varphi_{15} \), all capacitors in the FIR filter are shorted, while the ADC also samples the output voltage. The charge-sharing that occurs at that moment implements a weighted
 summation of delayed samples, given by the equation:

\[ V_{\text{out}} = \frac{1}{C_{\text{FIR}} + C_{\text{ADC}}} \sum_{i=0}^{14} C_i V_{\text{in}}(i) \]  

(7)

where \( C_{\text{FIR}} = \sum C_i \) and \( V_{\text{in}}(i) \) is the input signal sampled at clock phase \( \varphi_i \). Note that the figure only shows positive filter coefficients. Thanks to the differential structure, negative coefficients can be implemented easily by cross-connecting a capacitor from the positive input node to the negative output node (and vice-versa).

The FIR filter is a sampled data system, like the ADC. Therefore, in order to be effective as an anti-aliasing filter, the FIR filter should be oversampled as compared to the ADC:

\[ f_{\text{FIR}} = \text{OSR} \cdot f_{\text{ADC}} \]

(8)

As explained before, a single FIR filter requires \( k + 1 \) cycles to produce one output sample, thus it decimates the data rate inherently by \( k + 1 \). This can be compensated by time-interleaving \( p \) parallel filters, leading to the relation:

\[ f_{\text{ADC}} = \frac{p}{k + 1} f_{\text{FIR}} \]

(9)

Thus, the oversampling ratio can be expressed as a function of the number of filter taps \( k \) and the number of time-interleaved paths \( p \):

\[ \text{OSR} = \frac{k + 1}{p} \]

(10)

From performance point of view, a certain OSR can be chosen to sufficiently relax the preceding analog filter. Then, the number of taps \( k \) can be decided to achieve the desired filtering performance (filter steepness and out-of-band rejection). Together, this then decides the number of parallel channels \( p \) that is required. In the implemented prototype, an OSR of 4× is used with a 15-tap filter, thus 4 channels need to be time-interleaved.

Since the entire FIR filter is passive, it does not consume energy except for the switch drivers and clock phase generator. The passive charge sharing with the ADC is also free of power consumption, but leads to a signal attenuation factor equal to \( C_{\text{FIR}}/(C_{\text{FIR}} + C_{\text{ADC}}) \). Fig. 10 shows the attenuation as a function of the ratio between the FIR and the ADC capacitance, and its impact on SNR. The model here only includes kT/C sampling noise from the ADC and FIR filter, where \( C_{\text{ADC}} \) is set to 250fF and a fixed full-scale range of the ADC of 1V is assumed. For a large FIR capacitance, the attenuation is minimum and the overall SNR approximates the SNR of the ADC, which is 65.8dB. For smaller FIR capacitance, more attenuation occurs which results in a penalty in SNR. For the circuit implementation that will be discussed later, \( C_{\text{FIR}} = C_{\text{ADC}} \), and thus the attenuation is 6dB and the SNR loss is <1dB.

C. Analysis of imperfections

Various imperfections in the FIR filter can affect the SNR or linearity of the system. To analyze these, a behavioral model was built for a filter with \( \text{OSR} = 4, k = 15, p = 4, C_{\text{FIR}} = 250fF \). The imperfections that were modeled are: kT/C sampling noise, random channel-to-channel offsets and gain errors; random time-skew errors that are either applied between the channels (4 skew errors), or individually per sampling switch (4-15 skew errors); random capacitor mismatch (applied individually to all 4-15 capacitors). Fig. 11 shows an example output spectrum of the FIR filter for a single-tone input at 1.7MHz (the -3dB bandwidth of the FIR filter) when all types of errors are applied simultaneously with magnitudes \( \sigma_{\text{offset}} = 0.1mV, \sigma_{\text{gain}} = 0.05\%, \sigma_{\text{time-skew}} = 100ps \), and \( \sigma_{\text{cap}} = 0.5\% / \text{fF} \). Note that the magnitudes of the errors are for illustration only, they do not necessarily match the circuit implementation that will be discussed later. The effects that can be observed in the spectrum are similar to what happens in a time-interleaved ADC: the offset errors result in tones at multiples of \( \frac{1}{p} f_{\text{ADC}} \), while gain and time-skew errors result in tones at multiples of \( \frac{1}{p} f_{\text{ADC}} \) and \( f_{\text{in}} \). Interestingly, capacitor mismatch, which changes the filter characteristic per channel, does not introduce harmonic distortion, but only results in a (frequency-dependent) gain/phase error, and thus appears in the same way in the spectrum as gain errors do. For further analysis, Monte Carlo simulations (1000 runs) are done using the same errors as before. As a reference, Fig. 12(a) first shows the SNDR and SFDR histograms of a time-interleaved ADC with identical noise, gain, offset and time-skew errors, but without capacitor mismatch. Fig. 12(b) shows the histograms for the FIR filter when the time-skew is applied per channel. As can be seen, the performance of the time-interleaved FIR filter is similar to that of a time-interleaved ADC. Therefore,
the knowledge in the field of time-interleaved ADCs (in terms of achievable performance as well as mismatch correction techniques) could apply to the FIR filter as well. Fig. 12(c) shows the FIR filter performance when the time-skew errors are applied individually to each sampling switch. In this case, the SNDR and SFDR improve several dB’s as compared to the situation of Fig. 12(b). Despite the fact that there are now more individual error sources, the randomness of the time-skew error is now partially averaged, which leads to this slight performance improvement.

D. FIR filter implementation

According to the presented concept, Fig. 13 shows the 15-tap analog FIR filter implementation. A timing circuit generates 16 non-overlapping 2.5MHz clocks (\(\varphi_{0:15}\)) and a 10MHz ADC clock from the 40MHz master clock. Phases \(\varphi_{0:15}\) are level shifted to 1.6V using thick-oxide devices to drive the NMOS switches in the switched-capacitor FIR filter, such that a rail-to-rail input range can be achieved. While bootstrapped switches [12] could offer better performance without requiring a higher supply voltage, NMOS switches are chosen here as their performance is sufficient when boosted to 1.6V, while it simplifies the implementation to drive the 60 sampling switches. The FIR filter uses two supplies: 1.2V for the clock generation, and 1.6V for the level shifters and switch drivers. The filter weights are set by the values of the 15 capacitors as shown in the figure. With these coefficients, a low-pass filter is obtained that achieves 42dB suppression beyond 5MHz. However, as the filter is time-discrete, it also has passbands at multiples of 40MHz. Therefore, the filter can be used to convert a baseband signal or to perform down-conversion of a bandpass signal. As the filter characteristic only depends on the clock rate and the capacitor ratios, precise filtering can be achieved without any calibration. Programmable clocks or capacitors could be used for frequency/filter tuning. Since \(C_{FIR} = C_{ADC} \approx 250fF\), a rail-to-rail input to the FIR filter results in a 50% signal range at the FIR output, which matches to the 50% input range of the ADC (see Section II).

Since the capacitor matching within a single FIR channel is not so critical, a more simplified layout is adopted. Fig. 14 shows a top-view of the floorplan. Finger capacitors are used where metal layers 5, 6, and 7 are connected in parallel. Metals 4 and 8 implement a ground shield. The finger lengths are varied to scale the capacitors to the intended value, which is confirmed by post-layout extraction. The switches to connect the capacitor to the input or output node are placed underneath the capacitor itself.

E. Discussion on the proposed passive analog FIR filter

After discussing the design and implementation of the proposed passive analog FIR filter, it is here compared against the more classical approach of oversampling an ADC followed by digital filtering and decimation. Recall that both options were shown previously in Fig. 8 as solution 2) and 3).

In terms of relaxing the preceding analog anti-aliasing filter, both approaches achieve the same result as the first sampling occurs at 40MS/s in both cases. The required clock frequencies are also the same in both cases, namely 40MHz for the initial domain, gradually going down to 10MHz in the later stages once decimation is performed. In terms of noise, it was shown earlier that the proposed solution has 1dB SNR penalty due to passive charge sharing between the FIR and the ADC.
On the contrary, the ADC in the conventional scenario has 6dB in-band SNR improvement thanks to oversampling 4×. However, if a 10bit ADC is kept, this also means that the ADC’s power will increase by the same factor 4×, while the digital backend then requires 11bit resolution to maintain the ADC’s SNR after decimation. Alternatively, a 9bit ADC could be used at 40MS/s, which together with the 6dB SNR improvement would be equivalent to the 10bit ADC in the proposed scheme. In theory (following Schreier’s FoM), the power consumption of a 9bit 40MS/s ADC is identical to that of a 10bit 10MS/s ADC, but in reality the 10bit ADC may achieve lower power since low-resolution ADCs are often not at the noise-limit and thus less efficient. In the most ideal case where the ADCs consume equal power, the proposed scheme most likely still is the most power-efficient solution as the passive FIR filter is expected to consume less than a digital filter that requires several multipliers and adders. Regarding loading the preceding analog stage, both the ADC-first and the proposed approach present a switched capacitor load to the earlier stage. In this work, the total FIR capacitance for a filter is about 250fF and 4 channels are interleaved. Since only a subset of the FIR capacitors is connected to the input at each time, the maximum load is approximately 63fF. This is relatively low, and expected to be smaller than the input capacitance of a 9bit or 10bit ADC. However, due to the attenuation of the passive FIR filter, the reduced load is offset against the higher required input swing, demanding more gain from the preceding front end. Alternatively, as shown earlier in Fig. 10, a larger FIR capacitance could be used to trade-off between required gain and load capacitance.

Overall, the best SNR is probably achieved with the conventional system using an oversampled ADC and digital decimation, however this comes at the cost of higher power. For low-power applications where SNR is more relaxed, the proposed solution can be a more power-efficient approach.

### IV. Measurement Results

The ADC and filter are integrated together in 65nm CMOS (Fig. 15), occupying 0.0013mm² and 0.0048mm², respectively.

First, stand-alone ADC measurements are discussed. 10 samples were measured to characterize chip-to-chip variation. Fig. 16(a) shows the measured INL and DNL of the worst chip out of these 10 samples (chip #2), which reaches an INLmax of 0.46LSB and DNLmax of 0.60LSB. To isolate systematic non-linearities from random non-linearities, Fig. 16(b) shows the averaged INL and DNL curves from all 10 samples. The ‘noise-like’ pattern in the DNL and the spikes around codes 128 and 895 are attributed to systematic error sources. As a last step, Fig. 16(c) shows the INL and DNL of chip #2 again, but now after subtracting the average component. This pattern is more consistent with random comparator mismatch. In more detail, Table I shows the measured INLmax and DNLmax of all 10 samples, both before and after subtracting the average component. While only a limited set of 10 samples could be measured, these results suggest that the proposed DAC implementation achieves good linearity despite the small units, and that at present the systematic error sources still dominate over the random error sources. The dominant systematic error in the DNL, causing spikes around codes 128 and 895 is most likely caused by temporary dynamic effects, like DAC or reference settling, or an incomplete comparator reset. This is confirmed by measuring two new samples which are identical to the ADC in this work, except that their internal asynchronous clock is slowed down by ≈17% by adding more delay in the self-oscillation loop. The DNL spikes around codes 128 and 895 of these two new samples are about 2× lower than the present design, confirming that the errors are related to timing. This could be solved either by reducing the internal clock rate as in this experiment, or by adding redundancy to the SAR algorithm [13].

For comparison, Fig. 17 shows the measured max (INLmax, DNLmax) of the presented work in comparison to other 10b SAR ADCs. A trend line (with σ ∝ 1/√C) is also shown. This work achieves better linearity compared to prior art with sub-fF unit capacitors [9], and performs almost as good as designs with substantially larger units [14], [15], [16]. Note that the 10b ADCs in [14] and [16] use a 9b DAC with units of 1.5fF and 5fF, which is equivalent to units of 0.75fF and 2.5fF when normalized to the 10b LSB for a fair comparison.

![Fig. 15. Die photo and layout view in 65nm CMOS.](image)

![Fig. 16. Measured INL and DNL (worst chip out of 10 measured samples): (a) overall INL/DNL, (b) systematic component only, (c) random component only.](image)
Dynamic measurement results of the ADC are shown in Fig. 18. At the intended speed of 10MS/s, the ADC achieves 9.19b ENOB and consumes 24µW, leading to a FoM of 4.1fJ/conversion-step. From 10 measured samples, the average ENOB is 9.18b with a range from 9.16b to 9.21b. The ADC operates up to 30MS/s, where the ENOB reduces to 9.10b at Nyquist, leading to a FoM of 4.4fJ/conversion-step. Based on simulations, the ADC power breakdown is as follows: the DAC including the inverters required to drive the DAC capacitors consumes about 15%, the ADC logic 21%, the comparator with self-oscillation logic 55%, and the S&H 9%. This confirms that the DAC can be made low power thanks to using small units and short interconnect, even though a conventional switching scheme is used.

The measured results of filter and ADC together are shown in Fig. 19. The filter clocked at 40MS/s consumes 15.2µW. The transfer curve shows a -3dB bandwidth of 1.7MHz, and the stop-band above 5MHz has >42dB rejection until the next passband around 40MHz. As shown, when two -6dBFS in-band tones are applied around 40MHz, they are filtered and down-modulated to the baseband, achieving 51dB of IMD3. When one of the tones is placed out of band (45.377MHz), this tone is suppressed by 43dB by the filter. The spurious tones which occur due to mismatches in the time-interleaved FIR filter are indicated. As can be seen, the highest spur at 2.5MHz still remains under -60dBFS. The harmonic distortion of the FIR filter, showing up as IMD3 in the two-tone test, is in practice more limiting than the interleaving spurs. The output-referred noise of the entire system was measured to be 0.54LSB, which is dominated by ADC noise. The overall system consumes 39.2µW, of which 51% is used in the comparator and ADC logic, 11% in the DAC, 27% in the 1.6V switch drivers and 11% in the filter logic.

Table II shows a performance summary and comparison against low-area and power-efficient Nyquist ADCs [17], [10], a low-power radio baseband [18], and prior-art filter-integrated ADCs [6], [7]. Compared to [17], [10], this work has a competitive area thanks to the capacitor implementation, even though this work is implemented in a far older technology node. More clearly, Fig. 20 shows that this work achieves an area reduction of >10× compared to other Nyquist ADCs with

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**Figure 17.** Max. INL/DNL for 10b ADCs versus unit capacitor size.

**Figure 18.** Measured ADC spectrum at 10MS/s, and ENOB versus input frequency at 10MS/s and 30MS/s.

**Figure 19.** Measured performance of filter plus ADC: filtering function and 2-tone performance.

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**Table I**

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**Table II**

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* Estimated from plots
\* Reconfigurable, 1 setting shown
At 1.1F
At 5MHz (F_{sample}/2) and higher
At 5MHz (F_{sample}) and higher
At 1.1F_{sample}
Excluding systematic non-linearity
INLmax [LSB]
DNLmax [LSB]
\* Overall non-linearity
Sample
INLmax [LSB]
DNLmax [LSB]
\* Excluding systematic non-linearity
INLmax [LSB]
DNLmax [LSB]
\*
similar SNDR in >28nm nodes as listed in [1]. Fig. 20 also benchmarks this work in terms of power-efficiency. Compared to all ADCs >1MS/s from [1], this work has a competitive efficiency overall and the highest efficiency for the 65nm node. With respect to the filter, this work shows better filtering with lower area and power compared to [18], [6], [7].

V. CONCLUSION

This work combines a small-area 10b SAR ADC with a passive analog anti-aliasing filter. With 39.2µW total consumption, the proposed overall system is more efficient than conventional oversampling of the ADC (where the ADC alone would already consume 4×24µW) followed by digital filtering. A new DAC layout technique is used in the ADC to minimize the capacitance towards the fundamental noise limit. Due to the custom design, mismatch information is not available a-priori. Nonetheless, the measured results show that this 10b ADC achieves a small area of only 36×36µm and state-of-the-art efficiency while also achieving high linearity given the 125aF LSB capacitance.

REFERENCES

[2] P. Harpe, “A 0.0013mm² 10b 10MS/s SAR ADC with a 0.0048mm² 42db-rejection passive FIR filter,” in proc. CICC, 2018.

Pieter Harpe (SM’15) received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands, in 2004 and 2010, respectively. In 2008, he started as researcher at Holst Centre / imec, The Netherlands. Since then, he has been working on ultra low-power wireless transceivers, with a main focus on ADC research and design. In April 2011, he joined Eindhoven University of Technology where he is currently an Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly workshop on Advances in Analog Circuit Design (AACD) and analog subcommittee chair for the ESSCCIRC conference. He also served as ISSCC ITPC member and IEEE SSCS Distinguished Lecturer and is recipient of the ISSCC 2015 Distinguished Technical Paper Award.

Fig. 20. Area and energy consumption benchmark, data from [1].