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Application of Optical Proximity Correction for 193 nm Deep UV enabled InP Photonic Integrated Circuits

(Student Paper)

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ABSTRACT

We present the first-time application of rule-based optical proximity correction for InP based photonic integrated circuits fabricated with 193 nm deep UV lithography. Simulations of the lithography process were used to systematically predict and preserve pattern fidelity of sidewall gratings to find optimal correction parameters. Optical proximity corrected designs were exposed in ArF resist, demonstrating high correlation with lithography simulation results and exhibiting up to 70% improved pattern fidelity.

Keywords: Optical Proximity Correction, Pattern Fidelity, Sidewall Grating, Deep UV, InP, Photonic Integrated Circuits

1. INTRODUCTION

Photonic integrated circuits (PICs) are increasing in complexity which drives a need for improved reproducibility and scalability of the manufacturing process [1], [2]. This is causing tighter tolerances on the fabrication process of such devices, and subsequently has led to the application of more advanced generations of lithography equipment for PIC fabrication [3], [4].

High resolution lithography using 193 nm light sources has been applied for years in traditional electronics semiconductor manufacturing. For InP photonics however, the application of such manufacturing capability has only recently been demonstrated for foundry scale processing [5]. The combination of non-contact lithography, reduced mask overlay errors and improved critical dimension control offer considerable advantages for reproducibility and manufacturing tolerance. The NanoLab@TU/e cleanroom in Eindhoven offers access to a lithography process that can image structures with a minimum feature sizes down to 90 nm. The need for minimum feature sizes enabled by this fabrication technology is not immediately evident from the dimensions of basic components such as a photonic waveguide. However, the absolute dimensions, roughness and overlay of these structures, have a large impact on the performance of these PICs, requiring more advanced patterning than equally dimensioned structures in traditional electronics.

In contrast to electronics where most chips have a Manhattan (orthogonal structures) type layout, PICs have less conventional shapes like curves, tapers and sub-wavelength shape modulations in various orientations as shown in Fig. 1. With some of these features reaching very small dimensions, it becomes necessary to apply Optical Proximity Correction (OPC) to realize optimal pattern fidelity in the image transfer process. Existing OPC methods have been specifically adapted for photonics to deal with the deviating shapes and orientations [6], [7]. For photonics it is not enough to look at quantifiers like width and length. It is required to look in multiple directions and quantify pattern fidelity as a figure of merit for the matching quality with the design intent.

This paper presents the simulations of the DUV projection lithography process using the GenISys LAB software, and the first-time application of rule-based OPC to optimize pattern fidelity for an InP sidewall grating demonstrator device. The simulation output was used to create an OPC enabled reticle and patterning experiments were conducted to verify the simulation outcome.

Figure 1: Examples of geometries in PICs: Bends (Left), Tapers (Middle), Subwavelength modulation features (Right).

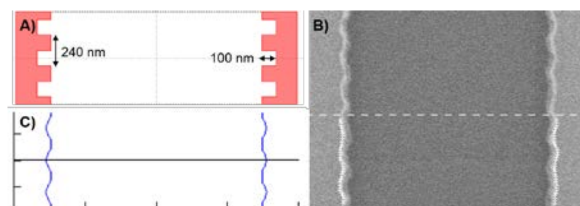

Figure 2: 1.5 µm waveguide design with sidewall grating at 240 nm pitch and width modulation of 100 nm per side (A), SEM image of fabricated resist pattern (B) and simulated resist pattern (C).

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2. OPTICAL PROXIMITY CORRECTION

An InP deep ridge waveguide with a nominal width of 1.5 µm and a sidewall grating with a period of 240 nm and width modulation of 100 nm per side was used as a demonstrator design and is illustrated in Fig. 2A. When this structure is imaged using the NanoLab@TU/e lithography process [8], the intended shape of the design is severely degraded due to diffraction and a combination of the resist and developer properties as shown in the SEM image in Fig. 2B. This can be accurately predicted using a calibrated resist and developer model and the exact illumination conditions of the exposure tool in the simulation software, as presented in Fig. 2C

The purpose of performing OPC, is to improve the resist pattern to have better match with the design-intent by pre-correcting for systematic fabrication limitations and artefacts. This is realized by introducing small dimensional changes or sub-resolution features which individually are too small to be resolved but will impact the diffraction pattern of total the exposure. When the exposed pattern is accurately predicted it becomes possible to run an entire design of experiments (DOE) of OPC variations minimizing a quantifier that describes the pattern mismatch. Fig. 3 illustrates how the pattern mismatch is quantified by performing a logical exclusive-or (XOR) operation on the intended design and simulated resist pattern from Fig. 2A and 2C respectively. The surface area of the resulting polygon can easily be extracted as a function of the applied OPC design parameters [7].

Figure 3: Resulting mismatch pattern by performing XOR logical operation on Design and Simulated resist pattern.

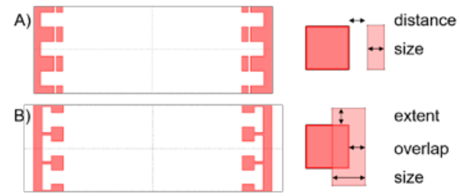

Figure 4: Scatter bar (A) and Hammerhead (B) OPC rule types applied to demonstrator design.

3. PARAMETER OPTIMIZATION

In this work we have applied two types of OPC rules. Fig. 4A shows the application of a scatter bar to the sidewall grating design which is parametrized by a size and distance. Fig. 4B shows the application of a hammerhead to the same design which is parametrized by a size, extent and overlap. Both rules were combined and applied to the initial sidewall grating design and all OPC parameters were varied at 3 levels using a 3^5 full factorial design of experiments. The resulting corrected designs were individually run through a lithography simulation followed by the resist and developer simulation. For these simulations, a calibrated ArF coating layer stack was used on top of a silicon nitride hard mask and an InP substrate. For illumination conditions annular illumination was used with a numerical aperture of 0.75 and inner and outer sigma settings at 0.55 and 0.85 respectively. Focus offset and dose were chosen based on optimal focus energy matrix settings with the standard design prior to applying OPC rules.

The resulting resist profiles were collected for each variation and the XOR surface area was derived comparing the result to the intended sidewall grating design. A model was constructed parametrizing the XOR surface area as a function of the 5 parameters and their interactions. Fig. 5 shows the predictions of the constructed XOR surface area model as a function of the simulated area for each parameter variation. This figure also shows the XOR surface area of the reference design without OPC applied, signified by the red dashed line at 0.64 µm^2. The advantage of applying OPC to the design is clearly shown in this figure. Most OPC variations are resulting in smaller XOR surface area corresponding to a better pattern fidelity. In optimal combinations, up to 70% improvement in fidelity is possible resulting in only 0.19 µm^2 XOR surface area.

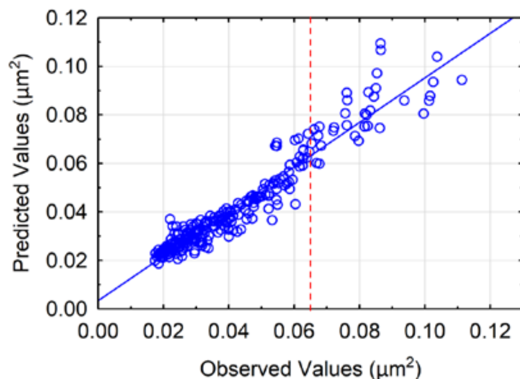

Figure 5: Model predicted surface area as a function of observed surface area of OPC parameter simulations in blue, with linear fit and reference level without OPC as red dashed line.

Feature	Scatter bar (nm)		Hammerhead (nm)		
	size	distance	size	extent	overlap
OPC-1	40	20	75	50	75
OPC-2	50	20	75	50	75
OPC-3	40	10	90	40	75
OPC-4	40	20	60	60	60
OPC-5	40	10	75	50	60
OPC-6	50	30	60	60	60

Table 1: Best simulated OPC parameter combinations of Scatter Bar and Hammerhead.

4. RETICLE AND IMAGING RESULTS

A total of six optimal OPC parameter combinations were extracted from the entire dataset and listed in Table 1. A reticle was fabricated with test structures having these different OPC rule combinations applied. The devices were exposed on an InP substrate with a silicon nitride hard mask in a focus-energy matrix. Best exposure results for each of the OPC rule combinations were collected using a Hitachi S9200 Scanning Electron Microscope (SEM). The SEM images of the resist patterns of the three best OPC enabled sidewall gratings are shown in Fig. 6, in decreasing order of simulated pattern fidelity, at optimum dose and focus. In each corner of these images, the corresponding OPC enabled design is shown as well as the simulated resist profile in the center.

These resist profiles should be compared to the exposure result of such device without OPC as was shown in Fig. 2B. All OPC designs show a significantly improved pattern fidelity. The simulated results show excellent correlation with the fabricated resist patterns. This supports our claim that the effect of OPC corrections can be simulated, making the application and optimization of OPC parameters at the software level an ideal method for generating InP structures with optimal pattern fidelity on a high-throughput exposure tool.

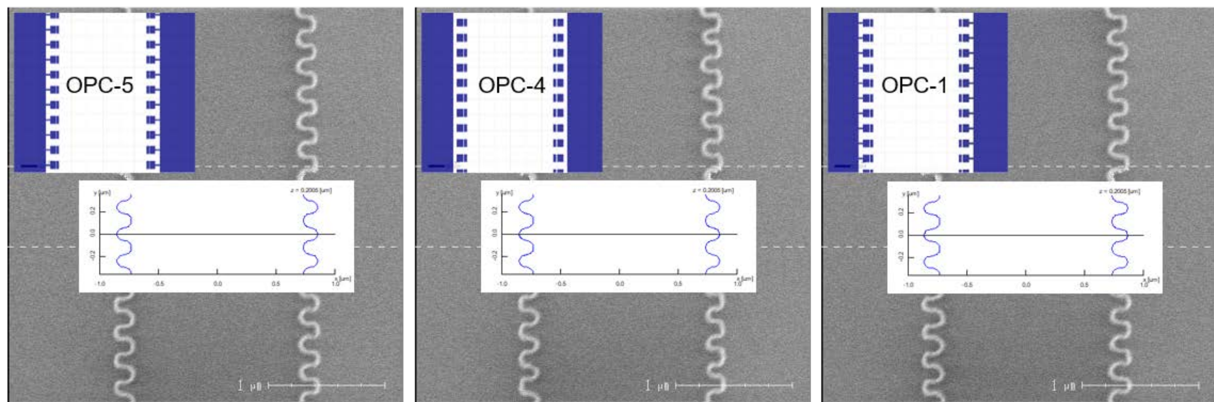

Figure 6: SEM images of sidewall gratings with best OPC rule designs in the top left corners and simulated resist pattern in the center.

5. CONCLUSIONS

Rule-based OPC was demonstrated for InP PICs using a sidewall grating device as a demonstrator. Pattern fidelity was optimized by performing an XOR operation on simulated resist profiles and the intended design and minimizing the surface area. Best OPC enabled structures show 70% improved pattern fidelity compared to a reference design without OPC applied. Well-defined OPC rules derived from simulations are the way forward to match fabricated device geometries with the design intentions.

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