Past, present, and future of InP-based photonic integration

Cite as: APL Photonics 4, 050901 (2019); https://doi.org/10.1063/1.5087862
Submitted: 05 January 2019 . Accepted: 27 March 2019 . Published Online: 30 May 2019

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Past, present, and future of InP-based photonic integration

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ABSTRACT
The application market for Photonic Integrated Circuits (PICs) is rapidly growing. Photonic integration is the dominant technology in high bandwidth communications and is set to become dominant in many fields of photonics, just like microelectronics in the field of electronics. PICs offer compelling performance advances in terms of precision, bandwidth, and energy efficiency. To enable uptake in new sectors, the availability of highly standardized (generic) photonic integration platform technologies is of key importance as this separates design from technology, reducing barriers for new entrants. The major platform technologies today are Indium Phosphide (InP)-based monolithic integration and Silicon Photonics. In this perspective paper, we will describe the current status and future developments of InP-based generic integration platforms.

I. INTRODUCTION: SIMILARITIES AND DIFFERENCES BETWEEN PHOTONIC AND ELECTRONIC INTEGRATION

Already in the first publications on integrated photonics—known at the time as “integrated optics”—it was assumed that photonic integration would follow the same path as microelectronic integration (Miller, 1969; Tien, 1977). And indeed, we see a lot of similarities. Figure 1 shows a clear exponential increase of photonic chip complexity (measured as the number of components integrated on a single chip), similar to Moore’s law in electronics, albeit with a slightly smaller gradient (Smit et al., 2012).

In the early years, significant research and development focused on the creation of the building blocks necessary for higher functionality circuits. The arrayed waveguide grating (AWG) was a particularly important example of a circuit element enabling larger scale integration. This de/multiplexing device enabled parallel circuit elements such as lasers and modulators to be combined to create wavelength multiplexed circuits, a technology which now underpins the modern internet. The blue dots in Fig. 1 show the advances in Photonic Integrated Circuit (PIC) complexity enabled with the AWG. Tens of components were feasible at the start of the millennium, and as integration with lasers and modulators has matured, hundreds of components are now being integrated. The most sophisticated circuits including lasers, modulators, detectors, and multiplexers have more than 1000 components in one chip. One such example is a Terabit/second optical transmitter (Summers et al., 2014). With conventional Indium Phosphide (InP)-based integration technology, it will be difficult to push integration levels much higher. However, in PICs where the light is confined in a thin membrane, such as silicon photonics, passive components can become smaller and higher integration densities are possible. The highest number of components per chip reported so far is 4096 for a 64 x 64 phased array realized in Silicon Photonics (Sun et al., 2013), the red dot in Fig. 1. Component numbers per chip are now constrained by electrical connectivity and thermal management. Membrane technologies, addressed in Secs. III and IV of this paper, offer a route to the size and energy reductions required for higher density integration, and for close integration with electronics, which will solve the interconnect bottleneck. In photonics, we do not foresee integration levels as presently achieved in digital microelectronics: physical dimensions and heat dissipation of photonic circuits are orders of magnitude larger than those of transistors. In this respect, photonics resembles analog and RF-electronics, where
integration scales are also significantly lower than in digital electronics. However, when the present bottlenecks in heat management and efficient integration of photonic and electronic circuits are solved, we expect that the exponential development can be pushed at least 2 decades further.

A. Semiconductor integration technology

The production of wafer-based electronic and photonic technologies have similarities as well as differences. Table I highlights some of the milestones which have been reached in both electronic and photonic integration. The development of photonic and micro-electronic integration follows largely the same path, with a delay of 25 to 30 years for photons, as indicated in Table I. The starting point for microelectronic integration was the invention of the transistor (Bardeen et al., 1948; Shockley, 1948), a compact semiconductor amplifier which replaced the bulky vacuum tubes. The starting point for photonic integration was the invention of the semiconductor laser, which replaced the bulky gas and solid-state lasers (Allerton et al., 1969). In the early years, both the transistor and the laser were used as discrete components. In microelectronics, Kilby succeeded in 1958 to integrate a circuit containing several transistors in a silicon substrate (Kilby, 1958). In the early days, several technologies were explored, but in the 1970s CMOS became the dominant integration technology in microelectronics (Wanlass and Sah, 1963). In photonics, a first integrated circuit consisting of a laser integrated with a modulator was reported in 1987 (Suzuki et al., 1987). The integration of several components in a semiconductor substrate marked the start of a long period of exponential development, which we know as Moore’s law.

B. Generic integration technology

In the early years of both microelectronic and photonic integration, when the circuit complexity was still relatively small, design and technology development were closely connected and the chip designs were technology specific. With the increasing circuit complexity, this close connection between design and technology became increasingly difficult and inefficient. An important step in the development of semiconductor integration technology was, therefore, the introduction of generic integration processes, i.e., process technologies that allow for decoupling of design and technology by offering chip designers a small set of well-defined standardized building blocks with which they can design a broad range of application specific circuits. In microelectronics this approach, which was introduced by Conway and Mead (Mead and Conway, 1979), caused a revolution in IC-design and opened the way to VLSI. An important advantage of designing in a process with standardized building blocks is that it enables combinations of designs from a number of different designers on a so-called Multi-Project Wafer (MPW), which leads to a large reduction of the costs of prototyping. Additionally, the technology is continuously improved independently of the design. In photonics, this approach was pioneered by the COBRA research institute, now known as the Institute for Photonic Integration at the TU Eindhoven (Smit, 2002). It was adopted by a large number of European research groups in the ePIXnet Network of Excellence (ePIXnet, 2007), which brought Europe the world’s first photonic MPW runs in Indium Phosphide (InP) and Silicon Photonics in 2008.

Today InP-based monolithic integration and silicon photonics are the two major integration technologies in photonics. In both technologies, access to MPW runs is offered by industrial and semi-industrial foundries. The advantage of silicon photonics is that, as far as the process is CMOS-compatible, the integration processes can be run in a CMOS foundry, which provides them with a well-controlled and rapidly scalable fabrication environment. As the size of silicon substrates is significantly larger than that for InP substrates, its potential for scaling to high volumes is better. However, silicon photonics lacks light sources and amplifiers which strongly limits its potential for large scale integration. Work on integration of InP-based light sources and amplifiers on silicon substrates is underway, but formidable manufacturing challenges remain. InP-based monolithic integration offers the most comprehensive range of photonic functionality with high-energy-efficiency quantum well lasers and modulators, as well as optical amplifiers, detectors and a range of passive components for creating interferometers, combiners and modulators. An important milestone on the road to mature integration technology is the reduction of killer defect density to a level < 1 cm⁻², for silicon electronics this milestone was reached in 1987 and for InP photonics 23 years later, in 2010 (Kish et al., 2018).

C. Differences between electronic and photonic integration technology

Although microelectronic and photonic integration show a lot of similarities, there are also differences. Photonic building blocks

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**TABLE I. Important milestones in the development of electronic and photonic integration.**

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<thead>
<tr>
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<th>Electronics</th>
<th>Photonics</th>
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<tr>
<td>Invention of key component (transistor/seadector laser)</td>
<td>1947</td>
<td>1969</td>
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<tr>
<td>Semiconductor integration technology</td>
<td>1958</td>
<td>1987</td>
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<tr>
<td>Generic integration technology (MPWs)</td>
<td>1979</td>
<td>2008</td>
</tr>
<tr>
<td>Killer random defect densities reported &lt;1 cm⁻²</td>
<td>1987</td>
<td>2010</td>
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are larger than electronic building blocks, and the active building blocks such as optical amplifiers and modulators operate at much higher power levels than transistors. However, at the component level, the electronic amplifiers currently operate with three to four times more power than the photonic devices they are connected to. The footprint for the active components themselves are comparable if one considers only the waveguide areas and transistor circuits. However, the electronic driver areas are often dominated by passive components such as resistors, capacitors, and the input/output connections and photonic circuits include redundant chip area for cross-talk mitigation, waveguide bends, and electrical connections. Comparisons for high performance active photonic devices may be more appropriately made with RF and analog electronics, particularly when considering the full design flow and the numbers of integrated components. There is also an important difference in terms of operational capacity and technology maturity: the higher wafer throughputs in electronic circuit manufacturing enables a faster manufacturing learning curve when introducing new technology nodes.

Nanophotonic technology offers the prospect of order of magnitude power level reductions as well as footprint reduction. Both become critical as designs become thermally constrained. While it is not envisaged that photonics will scale to the same component densities seen in CMOS electronics, the application of membrane-based technologies creates a roadmap to the level of tens of thousand components per chip, as indicated in Fig. 1. This does however raise new challenges in terms of mechanical, thermal, and electrical design.

D. Outline

In this perspective paper, we will focus on InP-based integration technology. In Sec. II, we will give a short overview of the present status of this technology. We will discuss membrane-based technologies which support integration with electronics in Sec. III and the next nanophotonic node which supports higher integration densities in Sec. IV.

II. GENERIC InP-BASED INTEGRATION TECHNOLOGY

An extensive description of InP-based generic integration technology is given in (Smit et al., 2014). Here, we will give a short overview including some recent progress. Figure 2 shows the relation between generic electronic and photonic integration technology. Electronic circuits are composed of a very small set of basic building blocks: transistors, capacitors and resistors, with a few variations, and electrical interconnection lines. In a generic integration technology which supports integration of these basic building blocks, even the largest processors and memories can be layed out by inserting the basic building blocks and more sophisticated combinations of building blocks (also known as IP blocks) from design libraries. The use of standardized, calibrated, and accurately described building blocks accelerates the design and enables increasingly accurate circuit level performance optimization before the chip design is finalized for production. In photonics, we apply the same approach. Light has an amplitude, a phase and a polarization. These properties can be manipulated with an optical amplifier, a phase modulator and a polarization converter, respectively. With a process in which we can integrate these basic building blocks with waveguides and passive components, we can realize a large variety of circuits, including tunable lasers, transmitters, and receivers, and a variety of sensor readout circuits. Note that in a generic approach, the laser is not a basic building block but a composite building block: in its simplest form, it is composed of an optical amplifier and a resonator. The resonator can be a ring or a waveguide with reflecting gratings, which may be physically separated for a distributed Bragg reflector (DBR) laser or superimposed in the case of a distributed feedback (DFB) laser. Tunable and pulsed lasers contain many more basic building blocks. The most important building block is the optical amplifier: in importance it is comparable to the transistor in electronics.

Around the turn of the century the COBRA research institute of TU Eindhoven started pioneering the development of a generic process for integration of optical amplifiers with waveguide components and phase modulators (Smit, 2002). In 2008 COBRA opened its process to external designers in the framework of the ePIXnet network of excellence, which had adopted a foundry model for photonics (ePIXnet, 2007). The process is very similar to processes that are used by some vertical integrated companies like Oclaro and Infinera, but these were not accessible for external designers. In 2009 and 2010, two large European research projects were started (EuroPIC and PARADIGM) with the aim to transfer the foundry model from the COBRA university environment to an industrial environment. In EuroPIC and PARADIGM, Oclaro (Caswell, UK) and the semi-industrial Heinrich Hertz Institute (Berlin) started preparing a foundry process for open access. COBRA licensed its own foundry process to the startup company SMART Photonics, who started providing commercial access in 2013. In 2014, after the end of the PARADIGM project, the Henrich-Hertz Institut (HHI) also decided to provide commercial access so that presently two European foundries provide commercial access to InP-based generic
photonic integration processes. So far, they are the only open-access generic InP-foundries in the world providing pre-specified building blocks in so-called process design kits (PDK). Figure 3 shows the basic building blocks which are now available on these platforms.

A. Process design kits

Application specific design is greatly accelerated by the availability of prespecified building blocks which have been pretested and can be configured and placed according to the circuit requirements. This requires a heightened level of interoperability between design tools, fabrication methods and PIC prototype test and packaging. Europe’s key players in InP-based photonic integration are cooperating in the JePPIX-platform (JePPIX: Joint European Platform for Photonic Integration of Components and Circuits. www.jeppix.eu) on the development of a foundry eco-system to address these interoperability needs. JePPIX partners include PIC foundries, PIC designers, photonic design software developers, packaging and test partners and technology research partners. Central in the cooperation is the development of the Process Design Kit (PDK). It contains modules for generating the mask-layout of the building blocks and data supporting simulations. Furthermore, it contains templates for packaging and testing for PICs in which the input and output ports are defined to comply with packaging and test equipment. The PDK contains software for checking design rules and flagging up design errors. The PDK is the design interface between the user and the foundry for manufacturing, packaging, and testing of PICs. It determines to a large extent the potential of the foundry platform: the richer its contents (number of building blocks provided, accuracy of the description, achievable performance) the more powerful the platform. The JePPIX partners started cooperation on the development of PDKs in EuroPIC, PARADIGM, and the Dutch MEMPHIS project. Since then, they are continuing in a number of projects on further extension of the PDK content including, OpenPICs which started in 2016 and the InP-Pilot Line project InPulse which started early 2019.

B. Present capabilities

The example shown in Fig. 4 illustrates many of the present capabilities of the InP foundry platforms; it is a widely tunable laser. The laser consists of a ring resonator with an SOA for providing gain and three cascaded Mach-Zehnder filters for providing the wavelength selection. The three Mach-Zehnder filters consists of two MMI-couplers and two electro-optic phase modulators each. The filters have periodic wavelength responses with a ratio 1:2:4, which can be shifted with the phase modulators. By appropriate control of the phase shifters, the laser wavelength can be tuned over more than 70 nm, as shown in the right figure. The laser signal is coupled out of the ring with an MMI power splitter. In total the laser consists of 14 building blocks: one SOA, 6 phase shifters and 7 MMI-couplers. With a circuit size of $1.5 \times 3.5 \text{ mm}^2$, a number of them will fit in a MPW-cell of $4 \times 5 \text{ mm}^2$.

In the past decade, several hundreds of different MPW cell designs have been processed by the JePPIX foundries in more than 30 MPW runs, with PIC designs for telecommunication, data communication, microwave-photonic applications, fiber sensor
readouts, metrology, medical diagnostics, gas sensing, and automotive applications.

A description of the building blocks available in the JePPIX InP foundries in 2018 is provided in the JePPIX roadmap 2018 (JePPIX, 2018). The foundries provide optical amplifiers with 70–90 cm⁻¹ gain and a user defined length, DBR gratings, DFB and DBR lasers, electro-optical phase modulators for 10 Gb/s operation, thermo-optic and current injection modulators, high responsivity photodetectors with low dark currents and >30 GHz bandwidth, high and low confinement waveguides with losses <2 dB/cm, and a variety of passive devices: AWGs, MMI-couplers and reflectors, spot-size converters and polarization converters.

Recent innovations include the introduction of 193 nm scanner lithography for precision waveguide fabrication (Augustin et al., 2018) which has already shown low-excess-loss arrayed waveguide gratings (Bolk et al., 2018) through reduced feature sizes and more specifically, well-resolved inter-waveguide gap dimensions. Excess losses down to 0.15 dB were demonstrated. High accuracy methods to automate in-line measurements for gain (Pustakhod et al., 2018a), loss (Pustakhod et al., 2018b) and intracavity reflections (Zhou 2018) have been devised to enable both process optimizations and statistically representative component models. High speed electroabsorption modulators are now demonstrated, with 55 GHz bandwidth (Trjovkic et al., 2018) and 112 Gbit/s operation with polarization multiplexed electroabsorption modulators (Bauer et al., 2017) through the use of semi-insulating substrates. For the coming years, improvement of the platform capabilities are envisaged through enhanced efficiency, precision, and bandwidth for the building blocks, introducing statistically representative performance data into the PDK and reducing wafer to wafer variations.

III. WAVER-SCALE INTEGRATION OF PHOTONICS AND ELECTRONICS

As InP integrated photonic circuits increase in complexity, component density, and circuit performance, the wiring density between photonic and electronic components and thermal load become design limiting. Semiconductor lasers are typically 200 μm and longer for wide tunable lasers, but these can be reduced to order 100 μm within integrated circuits (Nakahara et al., 2015), and techniques to create shorter lasers are addressed in Sec. IV. Eliminating nonfunctional area is attractive for increasing functionality within the same area but this leads to profound challenges in terms of optical, electronic (Yao et al., 2016) and thermal (Giardi et al., 2015) crosstalk as well as optical, electrical, and thermal connectivity as information density increases and heat transfer must be efficiently managed. A broad range of strategies have been identified for the chip and wafer scale connection and integration of photonic and electronic circuits, ranging from the full embedding of a subset of key photonic functions into electronics, through to 3-D integration, hybrid integration, and heterogeneous integration. Table II provides an overview of the potential and challenges for these approaches.

The conceptually simplest approach from the electrical perspective is to partition the photonics and implement the light source in a separate chip. In this approach, high speed RF connections between modulators, detectors and drivers can be combined within the same chip. It does not however address the challenges associated with photonic connection and impairments introduced with imperfect interfaces in the photonic circuits. There are additional open questions on how scalable such approaches will be with many light sources and amplifiers per chip. 3D integration using through-silicon vias offers two-dimensional grids of bond pads and a route to more than a thousand electrical connections, but the use of large bond pads limits component density, both on the photonic side, and potentially on the electronic side also. Many of the proposed solutions using silicon waveguides use dielectric claddings, which will frustrate heat removal. Hybrid integration is defined here as the assembly of prefabricated chips, leading either to a submicron alignment requirement for chip to substrate assembly, or the use of larger chips incorporating mode-adaptation. Heterogeneous integration offers a highly scalable route to combine photonics and electronics and is implemented at the wafer scale for both electronics and photonics. The photonic circuit is not partitioned. All optical interfaces are implemented within the monolithic circuit and can therefore be optimized within the wafer scale process to remove parasitic reflections. Electrical interfaces can also be implemented with wafer scale processes, without the need for enlarged bond pads, saving surface area. The electrical connections can be reduced to the micron-scale thickness of the InP-based PIC stack.

An overview of recent developments in InP-based photonic integration is given in the special issue of the Journal of Selected Topics in Quantum Electronics of Jan/Feb 2018 (Williams et al., 2018). In heterogeneous integration there are a few different approaches. An overview is given by (Liu et al., 2018), we will give

<table>
<thead>
<tr>
<th>TABLE II. Convergence of electronic-photonic integrated circuit technologies.</th>
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<td><strong>Optical connections</strong></td>
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a brief summary here. In the most frequently applied approach an unprocessed InP die with the layer-stack required for the laser is bonded top-down on top of a processed silicon photonics circuit, after which the InP substrate is removed and a series of processing steps is applied for turning the unprocessed InP-stack into an optical amplifier or laser. Tapers are used to couple the light from the InP-layer to the underlying silicon photonics layer. The InP-dice have either been bonded onto the silicon photonics wafer using molecular bonding (Bowers, 2018; Elfaiki et al., 2018), or adhesive bonding (Dhoore et al., 2016). Transfer printing is proposed as a more cost-effective technology for bonding small InP-dice (coupons). In all approaches, the photonic circuit consists of two layers, a silicon layer and a III-V layer, between which the light is coupled with tapers. This causes coupling losses and it requires additional space for the couplers. Recently a more cost-effective approach was proposed in which the full photonic circuit is realized in a III-V stack epitaxially grown on a silicon wafer, which serves as a mechanical substrate (Liu et al., 2018). This approach comes close to classical InP technology. It combines the performance advantage of InP with the scale advantage of processing on silicon wafers.

So far most heterogeneous integration approaches focus on realizing a cost advantage by manufacturing photonic ICs on large silicon wafers and using the high performance of silicon-based equipment. Heterogeneous integration with electronics is further down the roadmap because it would require integration of three layers: a silicon electronics layer, a silicon photonics layer, and an InP photonics layer, which is considered too complex on the short term. In the aforementioned approach proposed by Liu, only one layer is required for the photonic circuit. However, because it is epitaxially grown, it cannot be integrated on top of a CMOS wafer by backend processing because of the high temperatures that occur during the epitaxy. An alternative would be to integrate it in the front end processing, but this would require a redesign of the full CMOS process.

In this section, we describe an approach in which the full photonic circuit is realized in an InP-based stack which is fabricated in a commercial integration process on an InP substrate. The photonic layer is transferred to a CMOS wafer by adhesive bonding with a BCB (benzocyclobutene, a robust polymer) layer and substrate removal, after which a III-V membrane of a few microns thick is left on top of the CMOS wafer. The electrical connections between the photonic and the electronic layer are realized using wafer scale processing. We call the approach IMOS: InP Membrane on Silicon. In the approach described here the fabrication of the Photonic IC is done on InP substrates, which limits the wafer size to 4 in. or 6 in. In Sec. IV we describe an improved IMOS technology which enables manufacturing on large silicon wafers.

Our approach for integration of photonics and electronics requires accurate co-design of the photonic and the electronic layer. This is anticipated to enable a step change in both efficiency and function. The shorter connections between detectors and amplifiers enable lower parasitic loss (Saeedi, 2016) and energy-efficiencies through the removal of impedance matching networks. The closer placement of electronic and photonic chips already allows for higher numbers of electronic connections and functions such as digital-to-analog conversion to be performed in the optical domain (Vanhoecke et al., 2017; Aimone et al., 2016). So far these techniques have been studied for single elements and devices, enabling connections between co-designed chips which are placed side by side, but larger circuits implementing on-chip multiplexing will require more electrical connections. Sensor and communication chips are increasingly leveraging multiple wavelength channels. While this is straight forward to implement from a photonic perspective, there are considerable challenges from an electronic perspective due to higher levels of control complexity and crosstalk.

Membrane-based photonic integrated circuits offer a powerful means to create a photonic plane over an electronic control plane as the substrate can be removed to reduce parasitics, enabling thermal and electrical vias, and to ensure the most intimate heatsink connections. As the light source and full photonic functionality is maintained within the same plane, the photonic circuits can be created without compromising the electronics. Similarly the electronic fabrication flow is not compromised by the photonics. Figure 5 shows an illustration of a InP-wafer and a BiCMOS wafer, which were co-designed and bonded on top of each other.

The intimate attachment of InP PIC wafers to electronics leads to a number of challenges. We envisage a longer term need to intimately connect components with the shortest distances, and therefore focus on methods to connect drivers and photonic devices with high-density, micron-scale vias. Figure 6 shows a cross section for the methods under development. A BCB layer is used for the purposes of both planarization and adhesion, but also provides optical, thermal and electrical isolation. Creating vias for electrical signal routing and thermal management requires the removal of the substrate. This photonic-electronic integration, also known as photonic integration, uses processed PIC wafers and ASIC wafers. Silicon BiCMOS wafers provide a mechanical support for the InP wafer membrane which is several microns in thickness.
In this approach, the full suite of generic building blocks is available, requiring no re-engineering of the photonics. Similarly, no bespoke processes are required from the electronics, offering a “zero-change” integration approach. The fabrication challenges for this technology node are therefore primarily at the interface, creating fine pitch vias. Design challenges address the re-engineering of co-designed circuits to take full advantage of the circuit level design freedom. With such intimate integration, it becomes impractical to include bias tees or termination resistors, for example, as these are now significantly larger than the other circuit elements. The removal of capacitors, transmission lines, resistive terminations, and uncontrolled inductances from, e.g., bond wires is key to reducing energy which is otherwise lost to heat. The heterogeneously integrated combination of state of the art industry-sourced photonics and electronics is expected to deliver considerable speed and energy improvements over co-packaged systems. And, it offers the possibility to create “smart photonic building blocks,” e.g., lasers and modulators which are integrated with monitor diodes and electronic control circuitry which keeps the building blocks at the right operating point despite of variations in temperature or fabrication process parameters.

The membranes used in the photronics approach use the same micron-scale waveguide features as used in today’s manufactured PIC products. However, removing the substrate creates considerably more design flexibility. As can be seen from Figs. 6 and 7, the photonic waveguides can now be completely clad using low index materials such as BCB, SiO$_x$, SiN$_x$, or even air. This enables far tighter confinement of light, the potential for new forms of mode-adaptation, and the introduction of precision surface grating technologies. Exploiting nanophotonic confinement in active devices does however require higher precision fabrication in terms of dopant profiles, lithography and etching and the optimized positioning of optically lossy, electrically-conductive materials. Section IV highlights recent advances.

IV. SILICON-BASED NANOPHOTONIC IMOS PLATFORM

The nanophotonic IMOS (InP Membrane on Silicon) technology node enables higher density photonics integration. This is achieved by using a thin InP-based membrane, in which both active and passive functions can be realized (van der Tol et al., 2018). The high index contrast obtained with the membrane allows an order of magnitude reduction of device cross section and for many structures such as bends, reflectors, and splitters, this enables significant areal reductions. Furthermore, as in the photronics platform presented in Sec. III, this nanophotonic membrane approach supports heterogeneous integration with micro-electronics. The nano-photonic IMOS platform is illustrated in Fig. 7.
Developing an IMOS-platform presents specific technological challenges and opportunities. The basic procedure involves wafer bonding of InP and Si, using BCB as the adhesive polymer. The BCB material provides a uniform bonding interface, with high bonding strength, high tolerance to topology and low outgassing (Keyvaninia et al., 2013). An etch-stop layer composed of InGaAs is placed between the InP substrate and the functional membrane layers. After bonding, the substrate and the etch-stop layer can be removed using well-chosen selective chemical etchants. Both before and after bonding, active and passive components can be fabricated in the membrane, using optimized lithography and dry etching technologies (Jiao et al., 2014). Where useful, double-sided processing (before and after bonding) is possible, which brings additional flexibility for optimizing devices (Shen et al., 2016a). Using these technologies a series of both passive and active devices have been demonstrated (van der Tol et al., 2018), including polarization converters, demultiplexers, and various laser structures.

High speed operation is facilitated in the membrane approach as considerable parasitic capacitance can be removed in comparison to n+ substrate circuits (Jiao et al., 2015; Zhang et al., 2018; and Zhao et al., 2017). A demonstration for this is the record high bandwidth for a membrane based UTC-photodiode (Shen et al., 2016b). The cross section of this device is shown in Fig. 8(a), with a SEM-picture given in Fig. 8(b). The principle of operation is based on absorption close to the p-side of a p-i-n diode so that only the fast carriers (i.e., electrons) need to travel through the intrinsic region. It should be noted that high speed operation is also feasible with semi-insulating substrates (van Dijk et al., 2014), but realization on a membrane platform enables integration with a suite of nanophotonic devices such as precision surface grating couplers, microrings and miniaturized passive components. Fabrication is performed with double-sided processing (Shen et al., 2016a). Figure 8(c) gives the frequency response up to 67 GHz (equipment limited). Equivalent circuit modeling...
based on these measurements indicates a 3 dB response beyond 110 GHz.

Another example of a realized active IMOS device is a membrane laser (Pogoretskii et al., 2016). It uses a twin guide structure with an S-shaped diode cross section, made possible by double-sided processing. Figure 9(a) depicts the schematic of the optical amplifier section, while Fig. 9(b) shows a realized device and one of the photonic crystal (PhC) reflectors used for building the laser cavity. Figure 9(c) gives the measured output spectra for two different pumping currents. For these first realizations the threshold currents are 20 mA and the output power in the fiber reaches 1 mW.

The first lasers have been designed with lengths of several hundreds of microns. However, the high index contrast of the membrane configuration is expected to enable much shorter cavities and even nanometer scale light sources. This requires very high reflectivity, low-loss cavities. In the platform, we fabricated the first µm-size metal-clad nano-LEDs, coupled to a membrane waveguide (Dolores-Calzadilla et al., 2017). Output powers reached 60 nW. Improvement of technologies to reduce the cavity losses and the surface recombination will open up the way to extremely small lasers in the IMOS-platform.

The IMOS platform still needs a significant effort for further development. From an application perspective it is important to reduce laser linewidth and increase output powers. Methods have been developed to facilitate high bandwidth modulators in the platform (Mejia et al., 2013) and an electro-absorption modulator with high optical bandwidth based on the bandfilling effect has been proposed (van Engelen et al., 2016). Work is now focused on developing these devices into building blocks in a next generation integration platform. Just like in the JePPiX approach, described in Sec. II, this will allow a rapid uptake of the technology through MPW-runs. The first experimental MPW-run for IMOS, involving 10 different photonic circuits from various designers, was recently completed. Figure 10 shows the passive and active device cross sections, and the realized wafer.

The longer-term perspective of this nanophotonic platform involves scaling to larger wafers. So far, research has been performed using 2- and 3-in. InP-wafers, but there is no fundamental restriction to this. When larger wafers become available, IMOS can be transferred to those, and using wafer bonding or transfer printing techniques it can be scaled to large silicon wafers. Apart from mimicking the building blocks from the current generic integration approach (the JePPiX foundries), the high contrast platform provides extra functionalities, including non-linear optical interactions, strong interface interactions and optical isolation. In this respect, IMOS is very similar to other membrane platforms, notably silicon photonics based ones. However, the combination of these possibilities with integration of optical sources and amplifiers makes IMOS a very promising nanophotonic integration platform.

V. OUTLOOK

While photonic integration has a long history, and it lags microelectronics by almost 30 years, there is increasing evidence that the technology is set to follow the same trajectory over the coming years. With the recent establishment of generic foundry technologies and the enabled multiproject wafer services, comparisons with microelectronics are both timely and instructive. The application of generic methodologies to the main platforms has allowed separation of design innovation and technology development which enables a broader uptake of the technology and diversity in circuit innovation. Continued pressure on performance motivates the development of new technology nodes for higher speed, higher precision, and energy efficiency. Circuits produced with wafer-scale technologies will benefit from large-scale manufacturing methods. We highlight promising new technology nodes to introduce electronic integration, to transition to integrated nanophotonics for high density and richer functionality, and a roadmap to waveguide integrated nano-lasers.

ACKNOWLEDGMENTS


ePiXnet, Towards a foundry model for micro- and nanophotonic ICs, a vision for Europe, vision document of the ePiXnet steering committee, March 2007.