A 0.1-nW-1-μ W energy-efficient all-dynamic versatile capacitance-to-digital converter

A 0.1-nW–1-μW Energy-Efficient All-Dynamic Versatile Capacitance-to-Digital Converter

Haoming Xin, *Student Member, IEEE*, Martin Andraud, *Member, IEEE*, Peter Baltus, *Senior Member, IEEE*, Eugenio Cantatore, *Fellow, IEEE*, and Pieter Harpe, *Senior Member, IEEE*

***Abstract*— A versatile, low-power, and energy-efficient capacitance-to-digital converter (CDC) for Internet-of-Things (IoT) is presented, based on an all-dynamic architecture with adaptable speed, resolution, and range. The proposed CDC includes a single-armed capacitive bridge and a differential switched-capacitor 10-b asynchronous successive approximation register (SAR) analog-to-digital-converter (ADC). The bridge output is directly sampled by the ADC through fully passive correlated-double-sampling (CDS) approach, which enables a fully dynamic operation. The design is fabricated in a 65-nm CMOS technology. Thanks to the dynamic nature of the CDC, sampling rates from 1 S/s up to 100 kS/s are supported and capacitances from 1.23 to 24.59 pF can be digitized, while the power scales inherently from 0.1 nW to 1 μW. Optionally, the range can be further extended to >100 pF, and oversampling can be used to enhance resolution. This makes the design versatile to efficiently deal with a variety of sensors having different speed and resolution requirements and different capacitance values. The 0.1 nW lowest absolute power is >20× smaller than the prior art, and the figure of merit (FoM) from 18 to 59 fJ/conv-step is also the lowest among prior designs. To provide application examples, this chip is further verified with a microelectromechanical (MEMS) pressure sensor and a MEMS accelerometer. It can measure environmental pressure consuming only 0.8 nW at a speed of 100 S/s, and measure acceleration using 1.4 nW at a speed of 200 S/s.**

***Index Terms*— Capacitance-to-digital converter (CDC), dynamic, Internet-of-Things (IoT), microelectromechanical (MEMS) sensors, successive approximation register (SAR) analog-to-digital converter (ADC), versatility.**

I. Introduction

RECENT Internet-of-Things (IoT) applications such as implantable biomedical systems [1] and autonomous environmental monitoring sensor nodes [2] require on-demand sensing circuits with a power consumption in the nanowatt range. Scarce energy is available due to their limited size, so ultra-low power consumption is crucial, while a moderate resolution is acceptable in these applications. Capacitive sensors are well suited for low-power sensing as they consume only dynamic power, and they can be used to measure many parameters such as pressure, acceleration, and humidity. In order to save power and reduce physical size, capacitive microelectromechanical (MEMS) sensors tend to have a relatively small capacitance, but the value and range are different for each sensor (e.g., 2–3 pF for an exemplary accelerometer [3], 8–12 pF for a pressure sensor [4], and 5–6 pF for a humidity sensor [5]). On top of this, different sensor types or applications require a different sensing speed. For example, an environmental pressure sensor only needs a relatively low rate, while an accelerometer measuring movements will require a much higher rate. Therefore, a low-power capacitance-to-digital converter (CDC) which can efficiently adapt both speed and range (from 1 to 25 pF) is critical to cover different sensors and applications.

Recent successive approximation register (SAR)-based CDCs can achieve a very good power efficiency down to 33 fJ/conv-step [6]–[8], but their absolute power is in microwatt range. On the other hand, recent low power designs [1], [9] can achieve a low absolute power of 110–160 nW, at the expense of decreased power efficiency. On top of this, many of these designs show a limited speed scalability. In [10], the speed can scale by about 13×, but the power scales only about 2.6×. The quasi-dynamic architecture proposed in [7] and the fully digital architecture in [11] can theoretically scale power and speed over a wide range, but this was not included in their measurement data. The direct SAR CDC architectures [12]–[14] where the sensing capacitance is incorporated in the digital to analog converter (DAC) capacitor array of the SAR analog-to-digital-converter (ADC) can provide a large speed and power scalability as well. However, their power efficiency (290–7937 fJ/conv-step) is not state of the art, as the ADC's DAC capacitance value should be comparable with the large sensing capacitance (picofarad range), making the ADC less power efficient.

To combine a low absolute power with high versatility and state-of-the-art efficiency, a versatile CDC based on an all-dynamic architecture is proposed, which consists of a passive single-armed capacitive bridge and an asynchronous SAR ADC. Thanks to its all-dynamic architecture, the power inherently scales with speed over 4 orders of magnitude. By using an array of on-chip reference capacitors, this design is able to cover an input range of 1.23–24.59 pF optimally, with a possible extension to >100 pF. In addition, it can deal with both single-ended and differential capacitive sensors. The leakage power is optimized to 0.1 nW, such that the

Manuscript received November 16, 2018; revised January 26, 2019; accepted February 18, 2019. Date of publication March 21, 2019; date of current version June 26, 2019. This paper was approved by Guest Editor Ángel Rodríguez Vázquez. This work was supported by the European Union's Horizon 2020 Research and Innovation Programme under Grant 665347. *(Corresponding author: Haoming Xin.)*

H. Xin, P. Baltus, E. Cantatore, and P. Harpe are with the Integrated Circuits Group, Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands (e-mail: h.xin@tue.nl).

M. Andraud is with the Department of Electrical Engineering, ESAT-MICAS, KU Leuven, 3001 Leuven, Belgium.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2902754

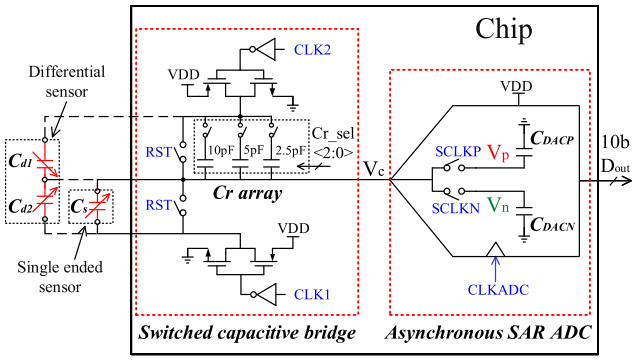

Fig. 1. Architecture of the versatile CDC.

efficiency is maintained even for very low sample rates, which is essential to enable on-demand operation or monitor quasi-static signals. An optional double-sided measurement mode (similar to [15]) is also implemented in this CDC to improve performance.

This paper is an extension of [16], and it is organized as follows: the versatile all-dynamic CDC is introduced and analyzed in Section II; measurement results of the proposed CDC are presented in Section III, and the conclusion is drawn in Section IV.

II. Proposed All-Dynamic Versatile CDC

A. Architecture

The architecture of the versatile CDC is shown in Fig. 1. It includes a single-armed capacitive bridge, which is essentially a capacitive voltage divider, and a differential switched-capacitor 10-b asynchronous SAR ADC, similar to [17]. For simplicity, only the sampling switches and aggregated DAC capacitance (C_{DACP} and C_{DACN}) of the ADC are shown. The bridge and ADC will be shown in more detail in Figs. 2 and 9 later on. In [9], a single-armed capacitive bridge was also used but with an integrating amplifier for charge transfer, while in this design the bridge output is directly sampled by the ADC's DAC through passive charge sharing. The total DAC capacitance of the ADC is sufficiently smaller than that of the target sensing capacitance. Thus, the signal attenuation caused by charge sharing between the capacitive bridge and the ADC's DAC is limited. Both blocks of the proposed architecture only use dynamic circuits, hence, consuming only dynamic power. Therefore, the power consumption of the CDC scales inherently with the measurement speed and sensing capacitance, making it an ideal architecture for a versatile interface. On top of this, the simple architecture also enables excellent power efficiency and low absolute power: the passive bridge unavoidably consumes energy dependent on the sensing capacitance, but the SAR ADC is the only active block, and has been shown to be very energy efficient [17], [18].

A single-ended sensor C_s can be connected externally. To deal with different nominal C_s values, the on-chip reference C_r can be programed by Cr_sel⟨2:0⟩ in a range from 2.5 to 17.5 pF with a step of 2.5 pF. Complementary switches are used to connect both sides of the bridge to VDD or GND with the help of CLK1 and CLK2, producing a regular or reversed

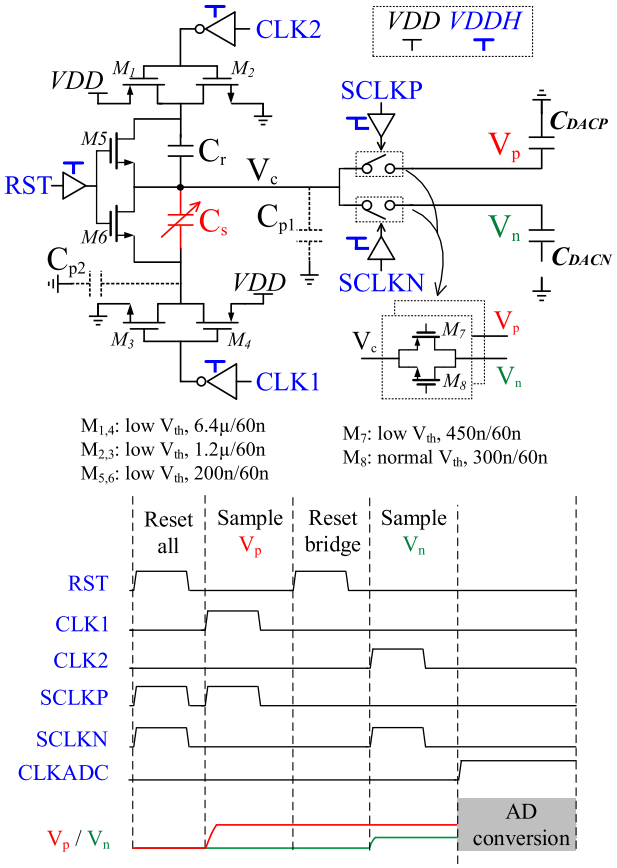

Fig. 2. Core of bridge and ADC (top) and operation waveforms (bottom).

output V_c. The reset switches in the capacitive bridge are controlled by the clock signal RST, and they are used to reset C_r and C_s when required. As indicated in Fig. 1, the capacitive bridge is also able to deal with differential sensors (C_{d1} and C_{d2}), for instance, for a capacitive accelerometer. In this case, C_r is disabled, the top and bottom sides of the differential sensor are directly connected to the bridge switches, and the middle point of the differential sensor is directly connected to the ADC. The SAR ADC samples V_c with the clock SCLKP and the reversed V_c with the clock SCLKN on C_{DACP} and C_{DACN} separately and performs the digitization at the rising edge of CLKADC. Both the capacitive bridge and the SAR ADC use a 0.6-V supply to save power and to achieve a ratiometric measurement. The schematic in Fig. 2 shows the detailed information about the switches used in the proposed CDC. To provide enough switch linearity, all the switches shown in Fig. 2 use clock drivers with a 0.8-V supply (VDDH). The size of M_1–M_4 is large to provide a fast *RC* settling time, so the leakage power of these complementary switches can be significant. Thanks to the 0.8-V clock drivers, PMOS transistors M_1 and M_4 can be completely switched OFF during the sleep period when both CLK1 and CLK2 are low, which significantly reduces the leakage power.

B. Circuit Operation

Since the proposed architecture uses a single-armed bridge, a passive correlated double sampling (CDS) method is used to provide a differential voltage to the ADC. The operation of the

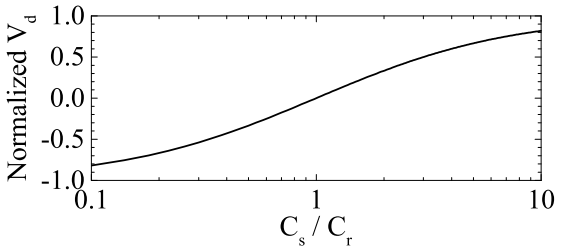

Fig. 3. Normalized differential bridge output for a fixed C_r at different C_s values.

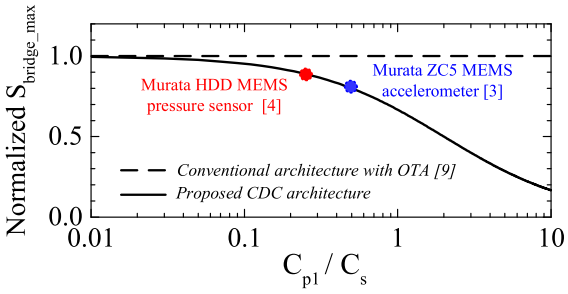

Fig. 4. Architecture comparison showing the impact of parasitic capacitance on the bridge sensitivity.

sensor interface is very similar when dealing with single-ended and differential sensors. Thus, the operation will be explained only for a single-ended sensor, as shown in the schematic of Fig. 2. The waveforms in Fig. 2 explain the operation over time: these waveforms are provided from outside the chip for the best flexibility. The reset phase comes first: CLK1 and CLK2 are low, so both the top and bottom sides of the bridge are connected to ground. RST, SCLKP, and SCLKN are high, thus resetting nodes V_c, V_p, and V_n to ground. Then, the first sampling phase starts. At this period CLK1 is high, while CLK2 remains low, thus connecting the top/bottom side of the bridge to GND/VDD, respectively. SCLKP is also high to connect the bridge output to the positive side V_p of the ADC's DAC (C_{DACP}). The voltage V_p can be calculated as

$$V_p = \frac{C_s}{C_s + C_r + C_{\mathrm{DACP}} + C_{\mathrm{p1}}} \cdot \mathrm{VDD} \tag{1}$$

where C_{p1} is the parasitic capacitance of C_s at the middle point of the bridge, which is relatively small compared to C_s. After V_p is sampled, CLK1 goes low, and RST goes high again to reset the bridge for the preparation of the second sampling phase. In the second sampling phase, CLK2 goes high, while CLK1 remains low, and SCLKN is high to sample the reversed bridge output on C_{DACN}. The voltage V_n can be calculated as

$$V_n = \frac{C_r}{C_s + C_r + C_{\mathrm{DACN}} + C_{\mathrm{p1}}} \cdot \mathrm{VDD}. \tag{2}$$

In this way, a full-bridge measurement is obtained with only a single arm, as the differential voltage V_d is given as

$$V_d = V_{\mathrm{p}} - V_n = \frac{C_s - C_r}{C_s + C_r + C_{\mathrm{DAC}} + C_{\mathrm{p1}}} \cdot \mathrm{VDD} \tag{3}$$

where $C_{\mathrm{DAC}} = C_{\mathrm{DACP}} = C_{\mathrm{DACN}}$. The mismatch between C_{DACP} and C_{DACN} is negligible for the 65-nm technology employed in this design, as C_{DACP} and C_{DACN} are fabricated very close to each other on the same wafer. When CLKADC goes high, the ADC digitizes this differential signal asynchronously [17], [19] without any additional external clock signals. The output code is produced after the conversion delay, and then, all the circuits' power down automatically thanks to their dynamic nature. While (3) is dependent on VDD, the ADC uses the same VDD as its reference, such that the digital output code will become independent of VDD. Fig. 3 shows the differential bridge output V_d (normalized to VDD) at different C_s/C_r ratios, assuming that C_{p1} and C_{DAC} are much smaller than C_s and C_r. As shown, the sampled differential voltage V_d is non-linear with the sensed value C_s. However, this bridge non-linearity is entirely predictable by (3) and, therefore, can be compensated afterward. Details of this compensation will be explained in Section II-F.

For a differential capacitive sensor, V_d can be rewritten as

$$V_d = \frac{C_{d2} - C_{d1}}{C_{d1} + C_{d2} + C_{\mathrm{DAC}} + C_{\mathrm{p1}}} \cdot \mathrm{VDD} \tag{4}$$

where $C_{d1} = C_0 - \Delta C$, $C_{d2} = C_0 + \Delta C$, C_0 is the nominal capacitance for both sensors and $2\Delta C$ is the differential signal provided by the sensor. Then, (4) can be rearranged as

$$V_d = \frac{2\Delta C}{2C_0 + C_{\mathrm{DAC}} + C_{\mathrm{p1}}} \cdot \mathrm{VDD}. \tag{5}$$

Thus, the bridge output voltage is linear with the capacitance change ΔC when a differential sensor is used. Therefore, no bridge non-linearity needs to be compensated in this case.

C. Capacitive Bridge Analysis

To obtain a sufficiently large sensitivity of the bridge, a single-ended sensor should have a suitable reference capacitance C_r. According to (3), the bridge capacitance to voltage sensitivity S_{bridge} can be calculated as

$$S_{\mathrm{bridge}} = \frac{\partial V_d}{\partial C_s} = \frac{2C_r + C_{\mathrm{DAC}} + C_{\mathrm{p1}}}{(C_s + C_r + C_{\mathrm{DAC}} + C_{\mathrm{p1}})^2} \cdot \mathrm{VDD}. \tag{6}$$

The maximum sensitivity can be found when $C_r = C_s$, indicating that C_r should be selected close to C_s for the best sensitivity. Rearranging (6) using $C_r = C_s$, the maximum bridge sensitivity is given as

$$S_{\mathrm{bridge\_max}} = \frac{\mathrm{VDD}}{2C_s + C_{\mathrm{DAC}} + C_{\mathrm{p1}}} \tag{7}$$

which shows that $S_{\mathrm{bridge\_max}}$ decreases with larger C_s, C_{DAC}, and C_{p1}. Thus, minimizing C_{DAC} and C_{p1} is beneficial to improve sensitivity, especially when C_s is small.

The calculation in (7) shows that the proposed CDC sensitivity depends on the parasitic capacitance C_{p1}, while this is not the case for the traditional switched-capacitor architectures (see [9]), which use an operational transconductance amplifier (OTA) to perform the charge transfer. As shown in Fig. 4, indeed, the bridge sensitivity of the proposed CDC reduces when C_{p1} is large compared to C_s(here, it is assumed that $C_{\mathrm{DAC}} = 0$ for simplicity), while the sensitivity of conventional architectures does not depend on the parasitic capacitance.

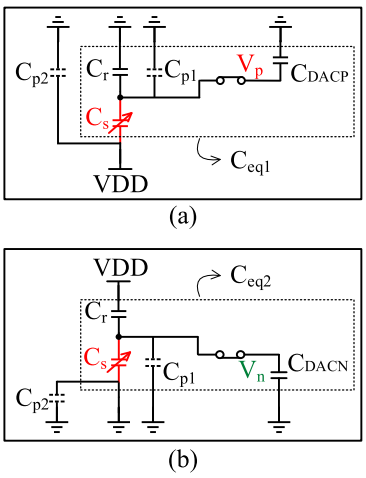

Fig. 5. Two sampling phases that consume energy in the bridge. (a) Sample V_p. (b) Sample V_n.

However, the parasitic capacitance of recent MEMS capacitive sensors is usually smaller than their sensing capacitance [3], [4], as indicated in Fig. 4. This makes the sensitivity loss of our CDC very little, when it is used together with this kind of sensors. Most importantly, as the proposed CDC avoids the power-hungry OTA, it achieves a very low absolute power and high efficiency, together with an inherent speed and power scalability.

The capacitive bridge only consumes energy during the two sampling phases, as shown in Fig. 5. The reset phases do not cost energy, as the capacitors are reset to the ground. The total energy consumption for one complete cycle can be calculated as

$$\begin{aligned} E_{\text{bridge}} &= (C_{\text{eq1}} + C_{\text{p2}}) \cdot \text{VDD}^2 + C_{\text{eq2}} \cdot \text{VDD}^2 \\ &= (C_{\text{eq1}} + C_{\text{p2}} + C_{\text{eq2}}) \cdot \text{VDD}^2 \end{aligned} \tag{8}$$

where

$$C_{\text{eq1}} = \frac{C_s \cdot (C_r + C_{\text{DAC}} + C_{\text{p1}})}{C_s + C_r + C_{\text{DAC}} + C_{\text{p1}}} \text{ and}$$
$$C_{\text{eq2}} = \frac{C_r \cdot (C_s + C_{\text{DAC}} + C_{\text{p1}})}{C_s + C_r + C_{\text{DAC}} + C_{\text{p1}}}$$

are the equivalent capacitances to ground at each phase, as shown in Fig. 5. C_{p2} is the parasitic capacitance of C_s at the bottom side of the bridge: it impacts E_{bridge}, as it needs to be charged to VDD during phase (a).

Assuming that C_{p1}, C_{p2}, and C_{DAC} are much smaller than C_s and C_r, (6) and (8) can be rewritten as

$$S_{\text{bridge}} \approx \frac{2C_r}{(C_s + C_r)^2} \cdot \text{VDD} \tag{9}$$

$$E_{\text{bridge}} \approx \left(\frac{2C_s \cdot C_r}{C_s + C_r}\right) \cdot \text{VDD}^2. \tag{10}$$

Fig. 6 shows the bridge sensitivity and energy for a given C_s value at a different C_r. S_{bridge} and E_{bridge} are normalized to the case when $C_r = C_s$. For best use, C_r should be selected close to the nominal value of C_s for a high bridge sensitivity. Since for most sensors, C_s only varies within a small range around its nominal value, and the sensitivity can be maintained. An array

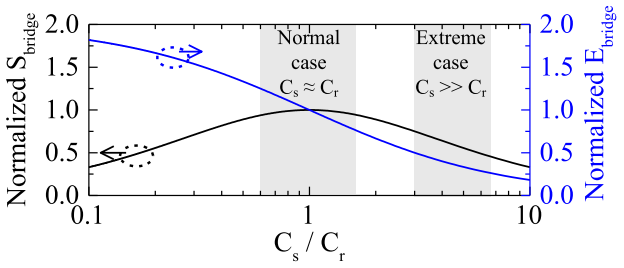

Fig. 6. Normalized bridge sensitivity and energy for a given C_s at different C_r values.

of reference capacitors from 2.5 to 17.5 pF implemented in this design can be easily programed to cope with sensors within the target capacitance range of 1–25 pF.

Even though the implemented capacitance range can already cover many different sensors, there are still outliers that could fall out of this range. For those cases, where the sensor capacitance is much larger than 17.5 pF, for instance, when C_s is around 100 pF, implementing a comparable value of C_r on-chip is not practical, as it will occupy a large chip area. Despite the sensitivity reduction, using a smaller C_r in such a case can be a reasonable choice, as it not only occupies less chip area but also consumes less energy in the bridge, as shown in Fig. 6. Note that, in this case, the differential bridge output V_d is large as indicated in Fig. 3, which means that the ADC should have a large input range to cope with this voltage. For another extreme case, when C_s is much smaller than 2.5 pF, it is suggested to implement a comparable C_r on-chip both for better sensitivity and less energy consumption, as the area overhead would be negligible. However, the sensitivity reduction caused by C_{DAC} and C_{p1} becomes more relevant in this case, according to (7), and this will lead to performance degradation.

D. Double-Sided Measurement

Because V_p is sampled before V_n, V_p may have more signal droop due to sampling switch leakage. Even though the entire sampling is finished within 3 μs, this can still lead to a slight inaccuracy. To solve this problem and to cancel ADC offset and $1/f$ noise, an optional "double-sided" measurement (similar to [15]) can be implemented, as shown in the waveforms of Fig. 7. First, a normal measurement as described in Fig. 2 is done which produces a digital output D_{out1}. Immediately in the next measurement, CLK2 goes high first when sampling on C_{DACP}, while CLK1 goes high afterward when sampling on C_{DACN}. By doing this, a reversed version of the differential voltage is sampled by the ADC, which produces a reversed digital output D_{out2}. By subtracting D_{out2} from D_{out1}, the double-sided measurement D_{ds} is obtained, which is able to compensate the aforementioned errors and to improve SNR by 3 dB [15]. After this, all circuits are powered down to sleep mode until the next measurement, as shown in Fig. 7.

The benefit of the double-sided measurement is valid assuming that the input signal is quasi-static during the two single-sided measurements (D_{out1} and D_{out2}). If the input

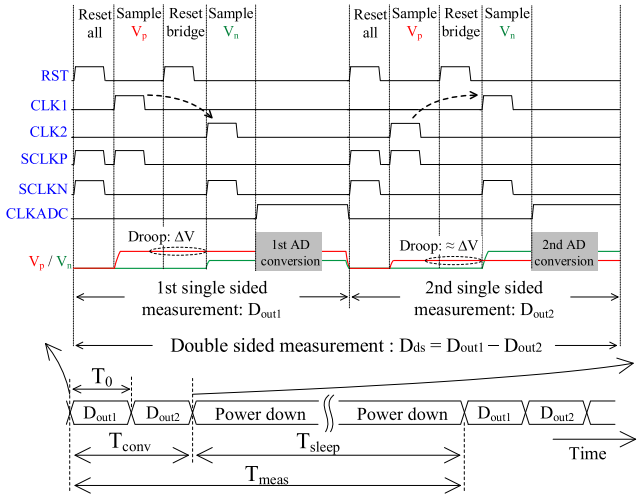

Fig. 7. Waveforms of the "double-sided measurement."

signal changes fast, the effectiveness of the double-sided measurement may reduce. Assuming that the sensor produces a signal V_{in} with a frequency f_{in} and voltage amplitude A at the ADC input, V_{in} in the time domain can be written as

$$V_{\text{in}}(t) = A \cdot \sin(2\pi f_{\text{in}} \cdot t). \tag{11}$$

The ADC is considered to be ideal for simplicity. Then, the two single-sided measurements are calculated as

$$D_{\text{out1}}(t) = G_{\text{ADC}} \cdot V_{\text{in}}(t) \tag{12}$$

$$D_{\text{out2}}(t) = -G_{\text{ADC}} \cdot V_{\text{in}}(t + T_0) \tag{13}$$

where G_{ADC} is the ADC voltage-to-digital code gain, and T_0 is the conversion delay of the first single-sided measurement. G_{ADC} can be calculated as

$$G_{\text{ADC}} = \frac{2^N}{V_{\text{FS}}} \tag{14}$$

where N is the number of bits of the ADC, and V_{FS} ($\propto$VDD) is the full-scale input range of the ADC. The phase shift in D_{out2} is given as

$$\varphi_0 = 2\pi f_{\text{in}}/f_0 \tag{15}$$

where $f_0 = 1/T_0$. Using (11)–(13) and (15), the double-sided measurement D_{ds} can be calculated as

$$D_{\text{ds}}(t) = D_{\text{out1}}(t) - D_{\text{out2}}(t) = C \cdot [2D_{\text{out1}}(t + T_{\text{shift}})] \tag{16}$$

where

$$C = \sqrt{\frac{1}{2}[1 + \cos(\varphi_0)]}$$

$$T_{\text{shift}} = \tan^{-1}\left(\frac{\sin(\varphi_0)}{1 + \cos\varphi_0}\right)/2\pi f_{\text{in}}.$$

According to (16), D_{ds} has an amplitude reduction by a factor of C and a time shift of T_{shift} compared to $2 \cdot D_{\text{out1}}$ (t), which is the ideal output of a double-sided measurement. The value of C at different f_{in}/f_0 ratios is shown in Fig. 8. When $f_{\text{in}} < 0.04 \cdot f_0$, C is larger than 99%, which means that the amplitude reduction is almost negligible, and the input signal

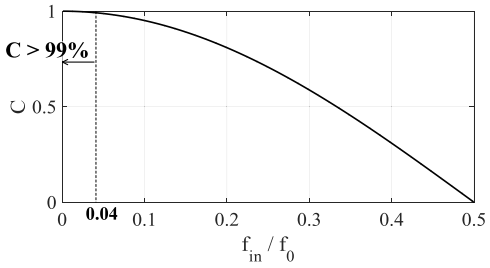

Fig. 8. Attenuation factor C at different f_{in}/f_0 ratios.

can be considered as "quasi-static." The nominal conversion delay of this CDC for a single-sided measurement is 10 μs, thus, the double-sided mode can ideally cover a 4-kHz signal bandwidth which is sufficient for many capacitive sensors. Regarding the time shift T_{shift}, it can be re-written as (17), using (15)

$$T_{\text{shift}} = \frac{T_0}{2}. \tag{17}$$

Hence, T_{shift} is a constant time shift which is independent of the input signal. Thus, it can be easily corrected in the digital domain.

E. Asynchronous SAR ADC

An asynchronous 10-b SAR ADC [17] is used such that a single clock edge enables the entire ADC operation. Asynchronous dynamic logic as in [20] is used to minimize the number of logic gates, which helps to reduce the leakage power. Moreover, high-V_{th} transistors with increased length (L = 100 nm) are used for the ADC logic to further minimize the leakage power, which dominates the power at low speed. The sampling switches are implemented with CMOS transmission gates rather than using dynamic clock boosting to enable operation at very low speed. As in [17], the ADC uses a segmented DAC with three unary and seven binary bits to improve linearity and save power. The DAC capacitance is only 300 fF with 250-aF unit capacitors to save power while achieving sufficiently low kT/C noise and sufficient linearity. A conventional differential switching scheme is used. C_{DAC} is sufficiently small compared to C_s and C_r, so that passive charge sharing between bridge and ADC is possible without causing strong signal attenuation.

The nominal ADC differential input range is about 1 V with 0.6-V VDD. As mentioned previously, C_s typically varies within a small range around the nominal value, so only a small part of the ADC signal range is useful. Therefore, two optional attenuation capacitors (300/600 fF) are added to the DAC [Fig. 9(a)] to reduce the DAC swing which effectively reduces the ADC input range, increasing the ADC sensitivity by a factor

$$S_{\text{rel\_ADC}} = (C_{\text{ATT}} + C_{\text{core}})/C_{\text{core}} = C_{\text{DAC}}/C_{\text{core}} \tag{18}$$

where $S_{\text{rel,ADC}}$ is the relative increase of ADC sensitivity, C_{core} is the capacitance of the core DAC, C_{ATT} is the added attenuation capacitance which is implemented with metal–insulator–metal capacitors, and C_{DAC} is the final total DAC capacitance.

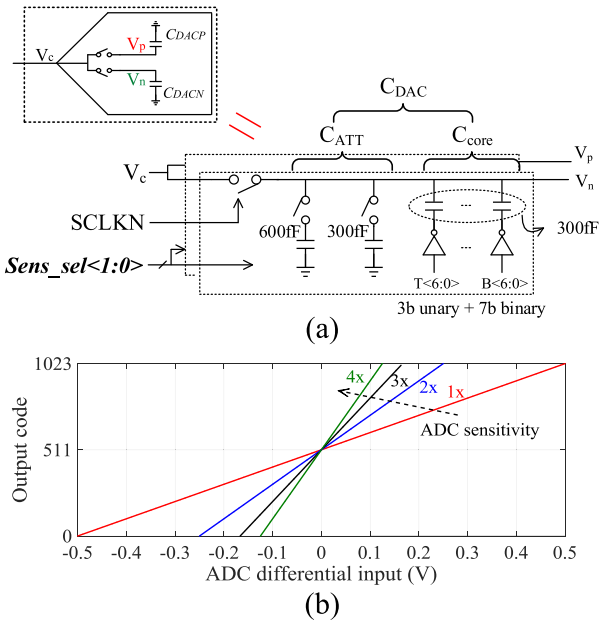

Fig. 9. Configurability of the ADC sensitivity. (a) Circuit implementation. (b) Calculated ADC range.

C_{DACP} and C_{DACN} in Figs. 1, 2, and 5 are in fact implemented by C_{DAC}, as shown in Fig. 9(a). Using Sens_sel⟨1:0⟩, the ADC sensitivity can be set from 1× up to 4×, as shown in Fig. 9(b). Note that with the increase of ADC sensitivity, the bridge sensitivity will be reduced according to (7), as the value of C_{DAC} becomes larger. However, this sensitivity reduction is not significant as long as C_{DAC} is still much smaller than the sum of C_s, C_r, and C_{p1}. In addition, as C_{ATT} reduces the DAC swing, and it also reduces the impact of DAC mismatch on the CDC accuracy. This results in a better CDC accuracy, as the gain factor from capacitance to code is changed. The low ADC sensitivity setting (which results in a large input range) can be used for cases where C_s is much larger than C_r, as discussed in Section II-C.

The total input-referred noise of the CDC in voltage can be estimated as a combination of the sampling noise on C_{DAC} $V_{n,\mathrm{samp}}$, the ADC quantization noise $V_{n,\mathrm{qn}}$, and the comparator noise $V_{n,\mathrm{cmp}}$, which are uncorrelated

$$V_{\mathrm{n,tot}}^2 \approx V_{\mathrm{n,samp}}^2 + V_{\mathrm{n,qn}}^2 + V_{\mathrm{n,cmp}}^2. \tag{19}$$

The noise contribution from the capacitive bridge is negligible, as C_s and C_r are relatively large compared to C_{DAC}. Fig. 10 shows the noise value of each contribution at different ADC sensitivities, based on simulations and calculations. The sampling noise is the thermal noise sampled on C_{DAC} which results in a $2\text{-}kT/C_{\mathrm{DAC}}$ contribution, so it has less noise contribution at higher ADC sensitivity. The quantization noise is also reduced with the ADC sensitivity, as the ADC input range is reduced. Then, the total noise is ultimately limited by the comparator noise, which does not scale with the ADC sensitivity.

The ADC uses a dynamic two-stage comparator [21], which includes a pre-amplifier and a latch stage. The dynamic

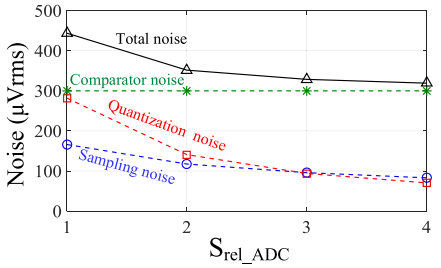

Fig. 10. Input-referred noise voltage of the CDC at different ADC sensitivities based on calculations and simulations.

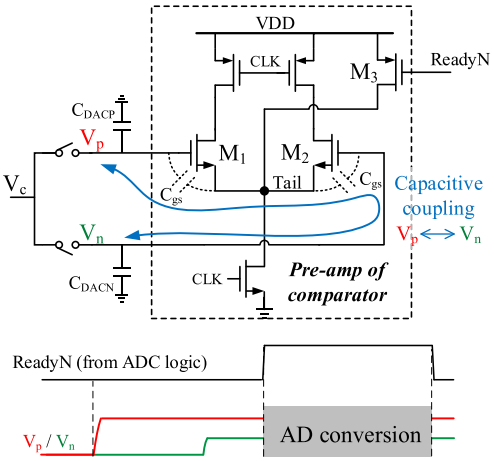

Fig. 11. Tail node control of the comparator pre-amplifier.

pre-amplifier shown in Fig. 11 is reset when CLK is low and enabled when CLK is high. Since there is only a parasitic capacitive load, only dynamic power is consumed. The sampled voltages V_p and V_n directly drive the input NMOS transistors (M_1 and M_2) of the pre-amplifier, as shown in Fig. 11. Normally in a differential ADC when V_p and V_n are sampled at the same time, the "Tail" node of the pre-amplifier shown in the schematic is kept floating during the sampling phase [17], [21]. However, this can be a problem when employing the CDS sampling scheme of this CDC, as the series parasitic capacitances C_{gs} of M_1 and M_2 would lead to disturbance due to capacitive coupling between V_p and V_n during the sampling phase. To avoid this, the "Tail" node is shorted to VDD by M_3 during the sampling period. M_3 is controlled by the ReadyN signal from the ADC logic, which is active during the conversion time of the ADC, as illustrated in Fig. 11.

F. Bridge Non-Linearity Compensation

As discussed previously, the output code is inherently non-linear with C_s but entirely predictable by the transfer function (3). After the sampled differential voltage V_d is converted by the ADC, using (3), the digital output D_{out} can be calculated as

$$D_{\mathrm{out}} = \frac{C_s - C_r}{C_s + C_r + C_{\mathrm{DAC}} + C_{\mathrm{p1}}} \cdot D_f. \tag{20}$$

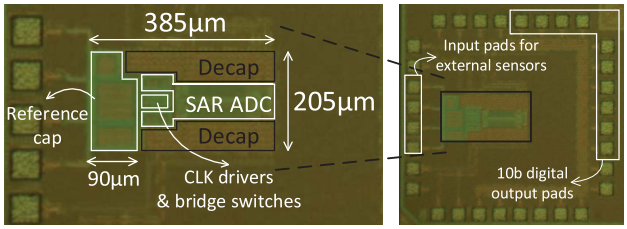

Fig. 12. Die photograph in 65-nm CMOS.

$D_f = \text{VDD} \cdot G_{\text{ADC}}$ is independent of VDD, being G_{ADC} inversely proportional to VDD according to (14). Thus, there are three unknown parameters in C_s-to-D_{out} transfer function (20): C_r, $C_{\text{DAC}} + C_{\text{p1}}$, and D_f. A three-point calibration is, therefore, required to reconstruct this transfer function. This is a disadvantage compared to many other prior designs, where the output code depends linearly on the sensing capacitance. However, many single-ended capacitive sensors, for instance, the pressure sensor in [4] and the humidity sensor in [5], show an intrinsic non-linearity, as well as variability of their nominal value and sensitivity, which needs to be calibrated, regardless of the sensor interface. Thus, sensor calibration can be done simultaneously with systematic non-linearity compensation. On the other hand, the proposed CDC can actually benefit from the bridge non-linearity, as it can measure a C_s value which is much larger than C_r. Situations where $C_s \gg C_r$ have a reduced sensitivity, but the smaller value of C_r enables a smaller chip area and less energy consumption, as discussed in Section II-C.

III. Measurement Results

This design was fabricated in a 65-nm CMOS technology and occupies an area of 0.08 mm^2, including the reference and decoupling capacitors but excluding I/O pads, as shown in Fig. 12. The measurement results of the CDC, measurement results with MEMS sensors, and the comparison to the prior art are discussed in this section.

A. CDC Measurement Results

To characterize the chip, a trimming capacitor with a range of 1–30 pF is used as the sensing capacitor. The total parasitic capacitance ($C_{\text{p1}} \approx C_{\text{p2}}$) due to the interconnection between this trimming capacitor and the chip is estimated to be about 2.5 pF. The CDC measurements reported in this section are all based on this parasitic capacitance value. First, the trimming capacitor is trimmed manually and measured with a GW INSTEK LCR-6100 meter for reference, and then, it is connected to the chip to obtain a digital code. This process is repeated for different values of C_s, yielding the code versus C_s, as shown in Fig. 13 ($C_r = 5$ pF). As expected, higher ADC sensitivity increases the output code range, while lower ADC sensitivity supports a wider sensing range.

Fig. 14 shows the measured output code with different C_r settings in double-sided measurement and 4 × ADC sensitivity mode. Fig. 15 shows the measured inaccuracy after a three-point calibration of each segment. The highlighted points

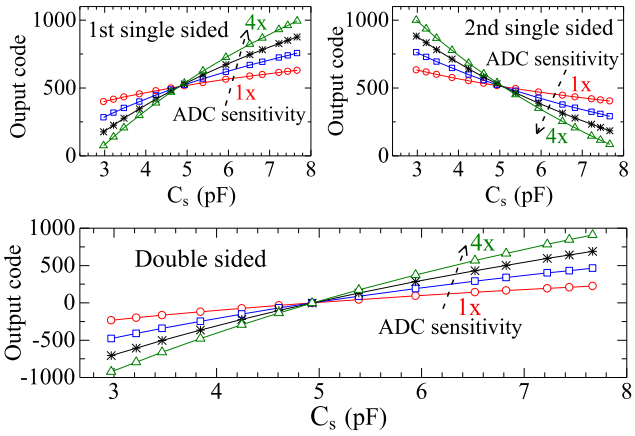

Fig. 13. Measured output code versus C_s for various settings of ADC sensitivity when $C_r = 5$ pF.

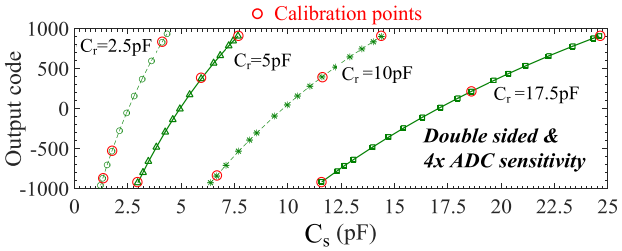

Fig. 14. Measured output code versus C_s for various values of C_r.

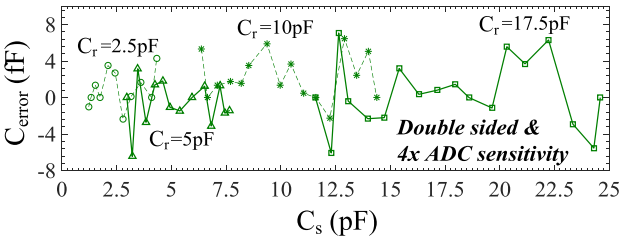

Fig. 15. Measured inaccuracy after three-point calibration for various values of C_r.

shown in Fig. 14 are used for calibration to compensate the bridge non-linearity. After calibration, the measured errors are within ±8 fF with a C_s range of 1.23–24.59 pF. It should be noted that these reported errors include inaccuracy of the LCR-6100 reference meter as well as potential errors due to the measurement procedure (e.g., disturbance in the environment and parasitic capacitance change due to manually tuning and placing the capacitor). Thus, the ADC non-linearity, which is the dominant inaccuracy source, is also measured separately to provide more reliable inaccuracy results. Fig. 16 shows the measured ADC INL and DNL errors at 4× ADC sensitivity over eight IC samples from the same batch. The minimum and maximum errors are −0.90 and 0.68 LSB, respectively, and this corresponds to a capacitance error of −11.4–8.6 fF for a capacitance range of 11.58–24.59 pF when $C_r = 17.5$ pF, which is similar to the inaccuracy shown in Fig. 15.

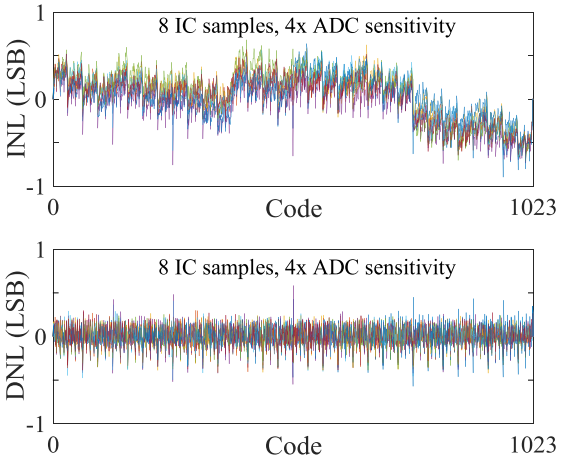

Fig. 16. Measured ADC INL and DNL over eight-IC samples.

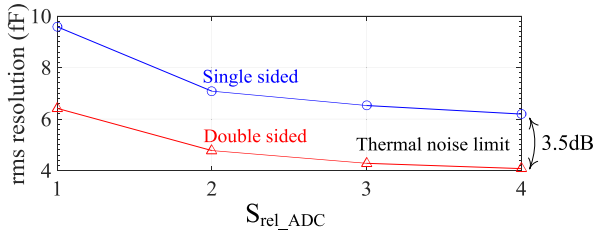

Fig. 17. Measured rms resolution versus ADC sensitivity when $C_r = 5$ pF.

To determine the noise performance of the CDC, the standard deviation of the digital output over 2^{14} measurements at the same C_s value is calculated. This process is repeated at more than ten other C_s values. Then, these standard deviations are averaged in the power domain, and referred back to the input capacitance, obtaining the rms resolution of the CDC. When $C_r = 5$ pF, the rms resolution for single- and double-sided measurements at different ADC sensitivity settings is shown in Fig. 17. A higher ADC sensitivity has better resolution as discussed previously, and the resolution is eventually limited by the thermal noise of the ADC comparator. As the double-sided measurement mode can also cancel the $1/f$ noise, it has about 3.5 dB better resolution compared to the single-sided mode. This is further verified observing the noise power spectral density shown in Fig. 18. Thanks to the all-dynamic circuitry, the power scales proportionally to the speed, as shown in Fig. 19(a). The leakage power is only 0.1 nW; hence, the figure-of-merit (FoM) of this design can be maintained even at a very low speed, as shown in Fig. 19(b). The power supply sensitivity is measured by checking the digital code variation when changing VDD from 0.55 to 0.65 V. Thanks to the ratiometric architecture of the CDC, the error due to the power supply change is within only 1.3 LSB ($C_r = 5$ pF and $C_s = 7.67$ pF), which corresponds to a capacitance error of 3.3 fF at the double-sided mode, as shown in Fig. 20. Thanks to the large ADC input range at $1\times$ ADC sensitivity mode, this CDC can support a much larger C_s (up to 100 pF) when $C_r = 17.5$ pF, as shown in Fig. 21.

The measured performance for different C_r settings at $4\times$ ADC sensitivity mode is summarized in Table I.

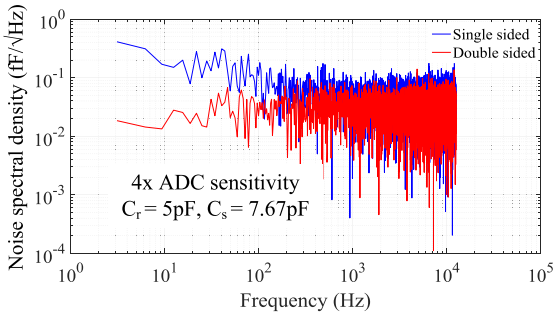

Fig. 18. Measured noise spectral density for single- and double-sided modes at a speed of 25 kS/s.

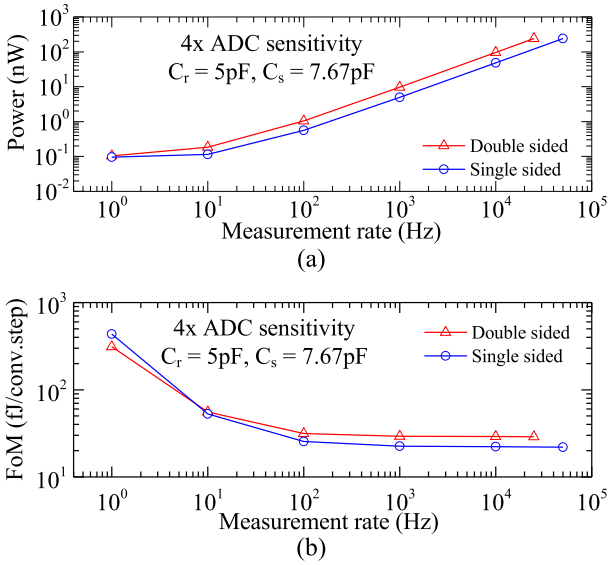

Fig. 19. (a) Measured power versus measurement rate. (b) FoM versus measurement rate for $C_r = 5$ pF and $4\times$ ADC sensitivity.

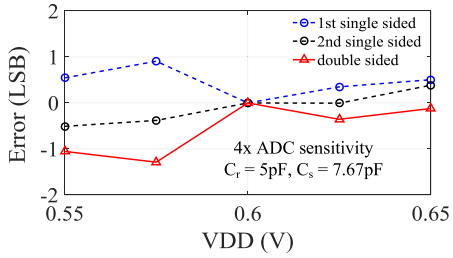

Fig. 20. Power supply sensitivity measurement.

Similar SNR is obtained for different C_r settings. When C_r is small, the signal attenuation caused by C_{p1} and C_{DAC} becomes more relevant, hence reducing the common mode voltage of the sampled input signal. The ADC comparator with an NMOS input pair thus becomes slower, which leads to a lower maximum speed. This can be easily fixed by using a comparator with a PMOS input pair, which works much faster at a low common-mode voltage. Note that unlike the single-sided-mode, the double-sided mode cannot support the Nyquist bandwidth (maximum speed/2) as discussed in

TABLE I
MEASURED PERFORMANCE SUMMARY (4× ADC SENSITIVITY, $C_{p1} \approx C_{p2} = 2.5$ pF)

C_r (pF)	2.5		5		10		17.5		Combined	
Input range (pF)	1.23~4.33		2.97~7.67		6.38~14.38		11.58~24.59		1.23~24.59	
Single/double sided	single	double	single	double	single	double	single	double	single	double
Resolution (fF)	4.38	2.90	6.19	4.07	10.54	7.06	16.86	11.10	16.86	11.10
SNR [a] (dB)	47.97	51.55	48.58	52.22	48.57	52.05	48.72	52.35	53.80	57.43
Max. speed (kS/s)	20	10	50	25	100	50	100	50	100	50
Power [b] (nW)	73.8	74.7	240	242	695	694	1006	1004	1006	1004
E/conv. (pJ)	3.69	7.47	4.80	9.68	6.95	13.88	10.06	20.08	10.06	20.08
FoM [c] (fJ/ conv-step)	18	24	22	29	32	42	45	59	25	33

[a] SNR = 20 log {Cap. range / (2√2 · Cap. resolution)} [c] FoM = (E/conv.)/$2^{(SNR-1.76)/6.02}$
[b] Power at max. speed, measured with largest C_s for each segment

TABLE II
COMPARISON WITH THE PRIOR ART

	[1]	[6]	[8]	[9]	[10]	[11]	[13]	This work [a]	
Method	Dual Slope	SAR	SAR + VCO	SAR	SAR + ΔΣ	Delay Chain	SAR	SAR	
Technology (nm)	180	180	40	180	180	40	180	65	
Cap. range (pF)	5.3~30.7	0~12.66	0~5	2.5~75.3	0~24	0.7~10000	6.8~10.8 [d]	2.97~7.67	
Resolution (fF)	8.7 [b]	1.2	1.1	6	0.16	12.3 [e]	3.79 [d]	Single	Double
								6.19	4.07
SNR (dB)	44.2 [b]	71.43	64.2	72.65	94.7	49.7 [e]	51.43 [d]	48.58	52.22
Speed (S/s)	156.25	62.5k	1M	250	4348	52.6k [e]	30~100000	1~50000	1~25000
Power (nW)	110	6440	75000	160	33700	1840 [e]	2.8~8820	0.1~240	0.1~242
Conversion time (μs)	6400	16	1	4000	230	19 [e]	10	20	40
E/conv. (pJ)	704	103	75	640	7750	35.1 [e]	88 [c]	4.80 [c]	9.68 [c]
FoM (fJ/conv-step)	5300 [b]	33	55	183	175	141 [e]	290 [c]	22 [c]	29 [c]

[a] Measured results with C_r = 5pF, 4x ADC sensitivity, $C_{p1} \approx C_{p2}$ = 2.5pF [b] Calculated with one subrange [c] @ max. speed
[d] Estimated from provided data [e] Measured with 11.3pF

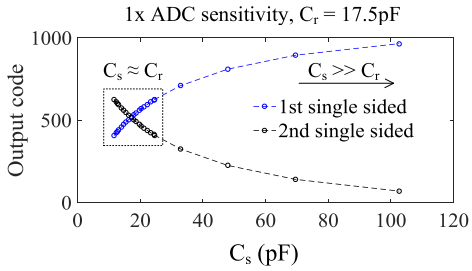

Fig. 21. Measurement results for extreme case when $C_s \gg C_r$.

Section II-D. The power is measured with the largest C_s for each segment, which is the worst case. The ADC and the 0.8-V clock drivers consume about 1 and 0.1 pJ per conversion, respectively, according to the post-layout simulations, and the rest is consumed by the capacitive bridge including the parasitic capacitance. A smaller C_r leads to lower energy per conversion, as the bridge consumption scales with the capacitance value. Therefore, better FoM is obtained for smaller C_r; yet, all settings achieve a very competitive FoM from 18 to 59 fJ/conv-step.

B. Measurements With MEMS Capacitive Sensors

To verify this design with real capacitive sensors, two types of MEMS capacitive sensors are tested. First, a Murata HDD MEMS pressure sensor is bonded to the chip and characterized in a pressure chamber. C_r is set to 10 pF, and 4× ADC sensitivity is used. The bridge non-linearity of this chip and the MEMS sensor's inherent non-linearity are calibrated together in the digital domain. An NXP MPXH6400A pressure sensor is placed close to the chip as a reference. Fig. 22(a) shows that the measured results of this chip can very well follow the results from the commercial reference. Only 0.8-nW power is consumed at the single-sided mode with a speed of 100 S/s and a resolution of 0.18 kPa.

For the second example, a Murata ZC5 MEMS accelerometer which is a differential capacitive sensor is bonded to the chip. C_r is disabled, 4× ADC sensitivity is used, and only the gain and offset errors are calibrated in this case, as no bridge non-linearity needs to be compensated. Fig. 22(b) shows that the measured results of this chip also match the commercial reference (Analog Devices ADXL335), while only 1.4-nW power is consumed at the double-sided mode with a speed of 200 S/s and a resolution of 12 mg.

C. Comparison With Prior Art

Table II shows the comparison of the performance of this paper ($C_r = 5$ pF, 4× ADC sensitivity mode) with the prior art. An SNR of 48.58/52.22 dB is obtained at single-/double-sided mode with a maximum speed of 50/25 kS/s. A lowest reported absolute power of 0.1 nW is achieved at 1 S/s, which is >20× smaller than the prior art. A reported lowest FoM

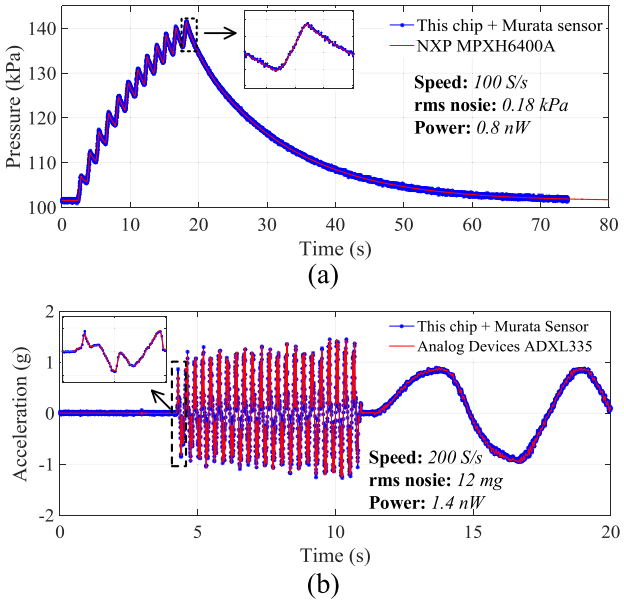

Fig. 22. (a) Pressure and (b) acceleration measurements of this chip with MEMS capacitive sensors.

TABLE III
SPEED AND POWER SCALABILITY COMPARISON

	[7] [a]	[10] [b]	[13]	This work [c]	
				Single	Double
Speed range (S/s)	up to 62.5k	0.5k~6.3k	30~100000	1~100000	1~50000
Scaling factor [d]	>> 4	12.6	3333	100k	50k
Power range (W)	up to 7.25µ	16µ~42µ	2.8n~8820n	0.1n~1006n	0.1n~1004n
Scaling factor [d]	>> 4	2.625	3150	10k	10k

[a] Estimated from measurements; actual range probably much larger
[b] Estimated from measurements
[c] Measured results with C_r = 17.5pF & 4x ADC sensitivity
[d] Scaling factor = max. value / min. value

of 22/29 fJ/conv-step is also achieved (at maximum speed) with single- and double-sided modes, respectively. Note that with smaller C_r, the FoM further improves down to 18 fJ/conv-step. The resolution of this paper could be further improved by means of oversampling or by spending more power in the comparator, which is dominating the overall noise level. Table III summarizes the speed and power scalability of this design ($C_r = 17.5$ pF, 4× ADC sensitivity mode). The speed of this design can scale over 5 orders of magnitude and 4 orders of magnitude scalability are achieved in power, making it able to deal with different sensors and applications easily and efficiently.

IV. CONCLUSION

This paper presented a versatile, energy efficient, and low-power CDC with only dynamic circuits, including a single-armed capacitive bridge and a 10-b asynchronous SAR ADC. It combines the state-of-the-art power efficiency (down to 18 fJ/conv-step) with the lowest reported power (down to 0.1 nW) and highest versatility, such that a wide variety of sensor types and IoT applications can be supported optimally. Measurements with a MEMS pressure sensor and a MEMS accelerometer are further demonstrated for verification, showing that this design can measure environmental pressure and acceleration with only 0.8 and 1.4 nW, respectively, while providing adequate precision and speed.

ACKNOWLEDGMENT

The authors would like to thank Murata Electronics, Hoofddorp, The Netherlands, for providing the sensor samples and Europractice, Leuven, Belgium, for IC fabrication.

REFERENCES

[1] S. Oh *et al.*, "A dual-slope capacitance-to-digital converter integrated in an implantable pressure-sensing system," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1581–1591, Jul. 2015.
[2] M. Andraud *et al.*, "Exploring the unknown through successive generations of low power and low resource versatile agents," in *Proc. Conf. Design, Automat. Test Eur. (DATE)*, Mar. 2017, pp. 290–293.
[3] Murata Electronics. *SCG10Z-G001CB Datasheet*. Accessed: Oct. 22, 2018. [Online]. Available: https://www.mouser.com/pdfdocs/scg10z_ver3.PDF
[4] Murata Electronics. *SCB10H Datasheet*. Accessed: Oct. 22, 2018. [Online]. Available: https://www.murata.com/en-us/products/sensor/accel/pressure
[5] L. Gu, Q.-A. Huang, and M. Qin, "A novel capacitive-type humidity sensor using CMOS fabrication technology," *Sens. Actuators B, Chem.*, vol. 99, nos. 2–3, pp. 491–498, May 2004.
[6] H. Omran, A. Alhoshany, H. Alahmadi, and K. N. Salama, "A 33fJ/step SAR capacitance-to-digital converter using a chain of inverter-based amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 310–321, Feb. 2017.
[7] H. Omran, A. Alhoshany, H. Alahmadi, and K. N. Salama, "A 35fJ/Step differential successive approximation capacitive sensor readout circuit with quasi-dynamic operation," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.
[8] A. Sanyal and N. Sun, "An energy-efficient hybrid SAR-VCO ΔΣ capacitance-to-digital converter in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1966–1976, Jul. 2017.
[9] H. Ha, D. Sylvester, D. Blaauw, and J.-Y. Sim, "A 160 nW 63.9 fJ/conversion-step capacitance-to-digital converter for ultra-low-power wireless sensor nodes," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 220–221.
[10] S. Oh, W. Jung, K. Yang, D. Blaauw, and D. Sylvester, "15.4b incremental sigma-delta capacitance-to-digital converter with zoom-in 9b asynchronous SAR," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[11] W. Jung, S. Jeong, S. Oh, D. Sylvester, and D. Blaauw, "A 0.7pF-to-10nF fully digital capacitance-to-digital converter using iterative delay-chain discharge," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[12] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, and A. Matsuzawa, "A 0.026 mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, Nov. 2007, pp. 244–247.
[13] T. M. Vo, Y. Kuramochi, M. Miyahara, T. Kurashina, and A. Matsuzawa, "A 10-bit, 290 fJ/conv. steps, 0.13 mm^2, zero-static power, self-timed capacitance to digital converter," in *Proc. Int. Conf. Solid State Devices Mater.*, Oct. 2009, pp. 1–19.
[14] M. M. Ghanbari, J. M. Tsai, A. Nirmalathas, R. Muller, and S. Gambini, "An energy-efficient miniaturized intracranial pressure monitoring system," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 720–734, Mar. 2017.
[15] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 174 pW–488.3 nW 1 S/s–100 kS/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 70–73, Mar. 2018.
[16] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 0.1 nW–1 μW all-dynamic capacitance-to-digital converter with power/speed/capacitance scalability," in *Proc. ESSCIRC*, Sep. 2018, pp. 18–21.
[17] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. H. M. van Roermund, "A 0.20 mm^2 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 240–248, Jan. 2016.

[18] H.-Y. Tai, Y.-S. Hu, H.-W. Chen, and H.-S. Chen, "A 0.85fJ/conversion-step 10b 200 kS/s subranging SAR ADC in 40 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 196–197.
[19] S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.
[20] P. J. A. Harpe *et al.*, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.
[21] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

Haoming Xin (S'18) received the B.Sc. degree from Xi'an Jiaotong University, Xi'an, China, in 2013, and the M.Sc. degree from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2015, where he is currently pursuing the Ph.D. degree with the Integrated Circuits Group.

His research focus is the design of low-power versatile sensor interface.

Martin Andraud (S'14–M'17) was born in Clermont-Ferrand, France, in 1988. He received the Diploma degree in engineering, with a focus on microelectronics, from Telecom Physics Strasbourg, Illkirch-Graffenstaden, France, in 2012, the M.S. degree in micro- and nano-electronics from Strasbourg University, Strasbourg, France, in 2012, and the Ph.D. degree in micro- and nano-electronics from the TIMA Laboratory, University of Grenoble Alpes, Grenoble, France, in 2016.

Since 2016, he has been a Post-Doctoral Researcher with TU Eindhoven, Eindhoven, The Netherlands. He is currently a Post-Doctoral Researcher with KU Leuven, Leuven, Belgium. His current research interests are the design of ultralow-power circuits and the development of machine-learning-based adaptive hardware techniques for analog and mixed-signal circuits.

Peter Baltus (M'08–SM'11) was born in Sittard, The Netherlands, in 1960. He received the master's degree in electrical engineering and the Ph.D. degree from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 1985 and 2004, respectively.

He was a Research Scientist, the Program Manager, an Architect, the Domain Manager, the Group Leader, and a fellow at Philips, for 20 years, and later NXP, Eindhoven, The Netherlands; Nijmegen, The Netherlands; Tokyo, Japan; and Sunnyvale, CA, USA, where he focused on data converters, microcontroller architecture, digital design, software, and RF circuits and systems. In 2007, he joined the Eindhoven University of Technology, as a Professor of high-frequency electronics. From 2007 to 2016, he was the Director of the Centre for Wireless Technology, Eindhoven University of Technology. Since 2017, he has been the Chair of the Integrated Circuits Group, Eindhoven University of Technology. He has co-authored over 200 papers. He holds 16 U.S. patents.

Eugenio Cantatore (F'16) received the master's and Ph.D. degrees in electrical engineering from the Politecnico di Bari, Bari, Italy, in 1993 and 1997, respectively.

From 1997 to 1999, he was a fellow with the European Laboratory for Particle Physics (CERN), Geneva, Switzerland. In 1999, he joined Philips Research, Eindhoven, The Netherlands, as a Senior Scientist. In 2007, he joined the Eindhoven University of Technology, Eindhoven, where he has been a Full Professor since 2016. He authored or co-authored over 200 papers in journals and conference proceedings. He holds 13 patents. His research interests include the design and characterization of electronic circuits exploiting emerging technologies and the design of ultra-low-power micro-systems.

Dr. Cantatore was a recipient of the Beatrice Winner Award from ISSCC for Editorial Excellence in 2006, the Philips Research Invention Award in 2007, the Best Paper Award from ESSDERC 2012, the Distinguished Technical Paper Award from ISSCC 2015, and nominated in the Scientific American top 50 list. He has been twice a Guest Editor of the *Journal of Solid-State Circuits*. He is active in the Technical Program Committees of IWASI, ESSCIRC, and ISSCC. From 2013 to 2016, he was the Chair of the Technology Directions Subcommittee. He is currently the Program Chair of ISSCC.

Pieter Harpe (SM'15) received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2004 and 2010, respectively.

In 2008, he joined the Holst Center/imec, Eindhoven, as a Researcher. Since, he has been working on ultralow-power wireless transceivers, with a main focus on ADC research and design. In 2011, he joined the Eindhoven University of Technology, where he is currently an Associate Professor of low-power mixed-signal circuits.

Dr. Harpe was a recipient of the ISSCC 2015 Distinguished Technical Paper Award. He is a Co-Organizer of the yearly workshop on Advances in Analog Circuit Design (AACD) and an Analog Subcommittee Chair of the ESSCIRC Conference. He also served as a Member of the ISSCC ITPC and a Distinguished Lecturer of the IEEE SSCS.