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A CMOS Peak Detect Sample and Hold Circuit

M. W. Kruiskamp and D. M. W. Leenaerts

Abstract—In pulse electronics systems, like particle calorimeters, circuits that can hold the peak value of a signal are important links. The desire of integrating complete particle detection systems on a single IC requires compact and low power peak detect sample and hold circuits (PDSH). In this paper, a PDSH architecture is presented which is especially designed for CMOS integration.

I. INTRODUCTION

In elementary particle physics, the energy of particles is often measured by means of semiconductor detectors [1]. The sensors produce a current pulse with a total amount of charge proportional to the absorbed energy. This charge is then integrated in a charge sensitive amplifier (CSA), resulting in a voltage step. To increase the signal-to-noise ratio, the step signal is usually filtered by a pulse shaping amplifier (PSA) [1], [2]. The resulting output signal is a voltage pulse with a peaking time (τ_p) typically on the order of 1 to several μ s. Such a system is realized as a CMOS integrated circuit with impressive results by Sansen and Chang [3].

The peak value of the output signal of the PSA contains the information about the energy of the particle. To digitize the peak value, for processing reasons, the peak value should be sampled and held by a peak detect sample and hold circuit (PDSH). The entire detector readout system is depicted in Fig. 1.

At this moment, the only possible analog structure to realize a high performance PDSH without the need of adjusting component values after fabrication is an amplifier charging a capacitor through a nonlinear device. The basic architecture is depicted in Fig. 2. When the input voltage is higher than the output voltage, the hold capacitor is charged by the OTA through the conducting diode. However, when the input voltage is lower than the output voltage, C_s cannot be discharged since the diode is in that situation reverse biased.

This principle is used with success in several discrete realizations [4], [5]. Systems with many detectors however,

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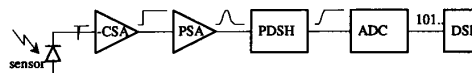


Fig. 1. Analog chain.

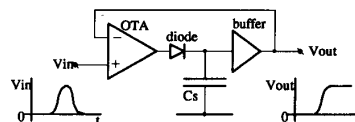


Fig. 2. Basic PDSH architecture.

require low power and compact integrated processing systems [6]. Although the architecture of Fig. 2 could be realized as a CMOS integrated circuit, the parasitic components parallel to the diode will give rise to some problems. When the pulse has reached its peak value, the output voltage of the OTA will become equal to its negative saturation voltage. In combination with the parasitic capacitance of the diode, this voltage step will result in a charge injection in the hold capacitor. To limit the voltage drop of the output, without increasing the hold capacitance, either the voltage step or the parasitic capacitance has to be limited. In this paper, a modified architecture is proposed which limits both.

II. MODIFIED PDSH ARCHITECTURE

Since a current mirror uses a diode to generate a voltage out of the input current, it has a rectifying behavior. The output current of an nMOST mirror, as depicted in Fig. 3, can not become negative, i.e., the current must flow into the mirror. Assuming that M2 is operating in saturation, the parasitic capacitance between the input and the output is only composed out of the gate drain overlap capacitance of M2. Furthermore, the input voltage swing, when switching off the mirror, will at most be equal to the threshold voltage of M1. These features of the current mirror make it very suitable to be used in the PDSH circuit.

The modified PDSH architecture is depicted in Fig. 4. The input signal is assumed to be a negative pulse. When the input voltage is lower than the output voltage, a current will flow into the mirror. This results in a current Iload, charging the capacitor, C_s . During this mode, the

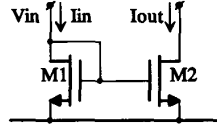


Fig. 3. nMost current mirror.

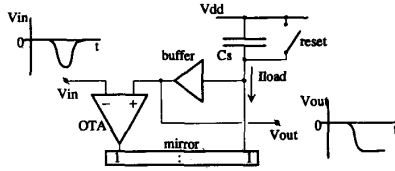


Fig. 4. Modified PDSH architecture.

output voltage of the OTA will be equal to the negative power supply voltage plus the gate-source voltage of the input MOST of the mirror.

When the input voltage of the PDSH becomes higher than the output voltage, the negative output current switches off the mirror. The output voltage of the OTA will at least be equal to the negative power supply voltage, only resulting in a small charge injection in C_s through the parasitic capacitance of the mirror. After the output signal has been processed by an analog to digital converter, as depicted in Fig. 1, the reset switch is closed. This will discharge C_s . After the switch is opened again, the circuit is ready to sample the next pulse.

A CMOS realization of this architecture is depicted in Fig. 5. The bulk of the nMOSTs are connected to V_{ss} and the bulk of the pMOSTs are connected to V_{dd} . The OTA is a differential pair (M1A, M1B) loaded with a mirror (M2A, M2B). The buffer is made by a source follower (M4, M6B). The rectifying mirror is composed out of M3A and M3B and the reset switch is realized by M7. The mirrors (M5A, M5B) and (M6A, M6B) mirror the bias currents I_{bias1} and I_{bias2} , respectively. The capacitor C_{load} models the input capacitance of an analog to digital converter, or a buffer.

III. PERFORMANCE

The output signal of the CMOS realization of the PDSH will not be exactly equal to the peak value of the input pulse, due to all kinds of non-idealities. The effects of the most important nonidealities will be discussed in this section.

A. Quiescent Current

The hold capacitor C_s is connected to the output MOST of the mirror (M3B) and the switch (M7) is connected parallel to C_s . Even when there is no input pulse and V_{reset} is equal to V_{dd} , both M3B and M7 will produce a

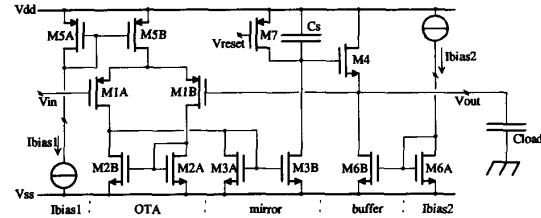


Fig. 5. CMOS realization of the PDSH.

very small quiescent current. When the resulting current flows into C_s , the output voltage slowly increases. This produces an output current which flows out of the OTA and compensates, after it is mirrored by M3A/M3B, for the quiescent current. The result is a neglectable offset voltage at the output, equal to the quiescent current divided by the transconductance of the OTA. When the PDSH is in the hold mode, the output voltage increases with a slope equal to the quiescent current, divided by the hold capacitor.

Much worse is the situation when the quiescent current flows out of C_s . The output voltage then slowly decreases, resulting in a decrease of the output voltage of the OTA, until M2B runs out of saturation. Unfortunately, this does not stop the charging of the hold capacitor and the output voltage will become approximately equal to the negative power supply voltage. Therefore, this situation must be avoided by not opening switch M7 completely.

B. Charge Injection

The only charge injection is due to the gate to drain capacitance of M3B, which is very small. The gate to source voltage of M4 is constant and therefore the gate to source capacitance of M4 is not contributing to the charge injection. All other parasitic capacitances are situated parallel to the hold capacitor C_s and are for that reason not doing any harm.

C. Limited Bandwidth of the Overall System

When the rectifying mirror (M3A, M3B) is conducting and all transconductances are assumed to be constant, the transfer function can be approximated by expression (1).

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{(1 + s\frac{1}{2}\tau_2)}{s\tau_1(1 + s\tau_2)(1 + s\tau_3)(1 + s\tau_4) + (1 + s\frac{1}{2}\tau_2)} \quad (1)$$

$$\tau_1 = \frac{C_s}{gm_{M1}} \quad \tau_2 = \frac{2C_{gs,M2}}{gm_{M2}} \quad \tau_4 = \frac{C_{load}}{gm_{M4}} \quad \tau_3 = 2C_{gs,M3}R$$

$$R \text{ is equal to } \frac{1}{gm_{M3}} \text{ parallel to } r_{ds,M2}$$

$$\text{and parallel to } r_{ds,M1}.$$

TABLE I
USED COMPONENT VALUES

Component	Value/size (3 Volt)	Value/size (5 Volt)
V_{dd}	1.5 V	2.5 V
V_{ss}	-1.5 V	-2.5 V
I_{bias1}, I_{bias2}	5 μ A	10 μ A
$V_{in\ dc}$	0 V	0 V
V_{reset}	open: 1 V; closed: -1 V	open: 2 V; closed: -2
M1A, 1B, 5A, 5B	$W = 9.6\ \mu\text{m}, L = 2.4\ \mu\text{m}$	
M2A, 2B, 4, 6A, 6B	$W = 4.8\ \mu\text{m}, L = 2.4\ \mu\text{m}$	
M3A, 3B, 7	$W = 2.4\ \mu\text{m}, L = 2.4\ \mu\text{m}$	
C_s	1 pF	
Load	0.1 pF	

Since the transconductance of M2 is in the same order of magnitude as the transconductance of M1, and C_s is much larger than the gate source capacitances, τ_2 can be neglected compared with τ_1 . However, τ_3 is dependent on the output current of the OTA and might become as large as τ_1 for low output currents. In the situation that τ_3 is larger than τ_1 , the system is under damped. In that situation, overshoot can be expected. To prevent overshoot, τ_3 must be made as small as possible and τ_1 should be made larger than τ_3 . This lower limit of τ_1 will define the minimal peaking time of the pulses that can be handled. The transconductance of the buffer and the load capacitance define τ_4 . As long as τ_4 is significantly larger than τ_1 , its influence will be small.

D. Mismatch

In fabricated chips, transistor mismatch is inevitable. Transistor mismatch in the OTA (M1A/M1B and M2A/M2B) results in a constant offset voltage between the input and the output of the PDSH. Typical values for this offset voltage are on the order of several mV to several tens of mV. Fortunately, this offset will be independent of the signal amplitude. It is therefore possible to compensate for this effect afterwards.

IV. SIMULATION RESULTS

In order to evaluate the behavior of the PDSH circuit, PSPICE simulations were performed. The transistor parameters that were used are based on the 2.4 μm MI-ETEC nwell CMOS process. The component values are listed in Table I. The circuit is simulated for two bias conditions: one with a power supply voltage of 5 Volt and one with a very low power supply voltage of 3 Volt.

In Fig. 6, the simulated response of the PDSH, with a 5 Volt power supply voltage and a pulse train at the input is depicted. All pulses are fourth order semi Gaussian pulses with a peaking time of 1 μs . The amplitudes are equal to -20 mV, -200 mV and -2 V. A reset pulse, with a duration of 1 μs , is presented to the circuit 5 μs after each peak. The response of the PDSH on the first pulse (-20 mV), is depicted in detail in Fig. 7. The final offset, mainly due to the non-ideal frequency behavior of the circuit, is less than 2 mV. In Fig. 8, the response on a -1

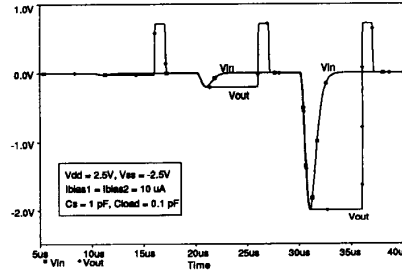


Fig. 6. Response to a pulse train.

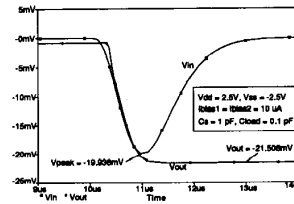


Fig. 7. Response to a -20 mV pulse.

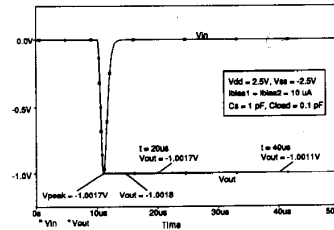


Fig. 8. Response to a -1 V pulse.

V pulse is depicted. The output is a good reproduction of the peak value of the input signal with less than 1 mV offset. The droop rate of the output signal, defined by expression 2, is small enough to perform an analog to digital conversion, since the conversion time of present A/D converters is around several μs . All specifications, obtained with PSPICE simulations, are listed in Table II.

$$\text{droop rate} = \frac{\partial v_{out}}{\partial t},$$

while the PDSH is operating in the hold mode. (2)

V. CONCLUSIONS

The proposed PDSH circuit combines a low power consumption, very low power supply voltages and a compact circuit. The circuit does not depend on absolute

TABLE II
SIMULATED SPECIFICATIONS

Specification	$V_{dd} - V_{ss} = 3 \text{ V}$	$V_{dd} - V_{ss} = 5 \text{ V}$
power dissipation:	60 μW	200 μW
minimal input voltage:	1.45 V	-2.4 V
minimal peaking time (τ_p)	0.5 μs	0.5 μs
error - 20 mV pulse, $\tau_p = 1 \mu\text{s}$	-2.0 mV (= 10%)	-1.6 mV (= 8%)
- 200 mV pulse, $\tau_p = 1 \mu\text{s}$	-0.9 mV (= 0.5%)	-2.0 mV (= 1%)
- 1 V pulse, $\tau_p = 1 \mu\text{s}$	+4 mV (= -0.4%)	+0.2 mV (= -0.02%)
- 2 V pulse, $\tau_p = 1 \mu\text{s}$	not possible	+2.3 mV (= -0.1%)
delay time	$\leq 300 \text{ ns}$	$\leq 300 \text{ ns}$
α - droop rate	28 $\mu\text{V}/\mu\text{s}$	29 $\mu\text{V}/\mu\text{s}$

component values, and is therefore very suitable for CMOS integration.

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