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Midpoint Voltage Stabilization of Split DC Bus in Three-Phase Four-Wire Shunt Active Power Filters

Prototyping of a Midpoint Voltage Balancer for the ECSEL JU Funded Project CONNECT

Xinwei Xu
Midpoint Voltage Stabilization of Split DC Bus in Three-Phase Four-Wire Shunt Active Power Filters
Prototyping of a Midpoint Voltage Balancer for the ECSEL JU Funded Project CONNECT

Dissertation submitted in partial fulfillment of the requirements for the degree of Professional Doctorate in Engineering

Eindhoven University of Technology
Department of Electrical Engineering
Electromechanics and Power Electronics Group

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August 29th, 2019
This thesis is approved by the scientific supervisor and the PDEng thesis evaluation committee. The composition of the PDEng thesis committee is shown in the following:

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The design described in this thesis has been carried out in accordance with the TU/e Code of Scientific Conduct.
Midpoint Voltage Stabilization of Split DC Bus in Three-Phase Four-Wire Shunt Active Power Filters

Prototyping of a Midpoint Voltage Balancer for the ECSEL JU Funded Project CONNECT

Xinwei Xu
The work described in this PDEng thesis is a part of the CONNECT project, which aims to research, design, develop, and showcase novel solutions for efficient devices and components of the future smart grid; to reduce the peak power demand by at least a factor of two. The CONNECT project is funded by the Electronic Components and Systems for European Leadership Joint Undertaking (ECSEL JU) under grant agreement No. 737434. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation program and from individual countries: Germany, Slovakia, the Netherlands, Spain, and Italy.

Second edition, August 2018
Midpoint Voltage Stabilization of Split DC Bus in Three-Phase Four-Wire Shunt Active Power Filters:

Prototyping of a Midpoint Voltage Balancer for the ECSEL JU Funded Project CONNECT

The increasing adoption of small-scale photovoltaic systems and electrical vehicles, which are commonly distributed unequally across three-phase feeders, aggravates voltage imbalance in electrical power distribution networks (EPDNs). Voltage imbalance in an EPDN poses a great threat to the normal operation of connected electric devices, causing overloading and overheating of distribution transformers, power loss in neutral wires, efficiency degradation of induction motors, and more.

Three-phase four-wire (3P4W) shunt active power filters (APFs) can be employed to deal with issues associated with voltage imbalance by injecting or sinking current to or from the point of common coupling (PCC) of an EPDN. In order to fully compensate the voltage imbalance in a PCC, a dc bus midpoint, to which the neutral current flows, must be provided.

In this thesis, a midpoint voltage balancer (MVB), which consists of a dual-switching-leg, two split capacitors, and two neutral inductors, is proposed. The MVB is designed to deliver a voltage-stable midpoint for a 20 kVA 3P4W shunt APF, which is used to enhance the voltage quality of the PCC by providing voltage imbalance compensation, voltage harmonic mitigation, and power factor correction.

Due to the utilization of a dual-switching-leg, the neutral current handling capacity of the MVB is doubled compared to some of existing neutral point configurations. An interleaved control is implemented in the dual-switching-leg, which minimizes the propagation of high-frequency current into the midpoint. In addition, the neutral inductors are designed in a way to enable ZVS operation across all IGBT switches of the MVB, when the neutral current is smaller than 29 A_{rms}. 
The operation of the MVB is governed by a dual-loop control, that includes an inner current loop and an outer voltage loop. The current loop facilitates the tracking of the total inductor current to the neutral current, preventing current injection into the midpoint. In addition, an active damping scheme is embedded in the current loop to damp the resonance introduced by the LC network. The voltage loop safeguards the midpoint against excessive voltage variations by addressing voltage imbalance between the two split capacitors. Furthermore, the voltage loop compensates any regulation error from the current loop by adjusting the current reference of the neutral inductors accordingly.

MATLAB simulation is carried out, which verifies the effectiveness of the proposed MVB. Moreover, a 20 kVA prototype has been built, and the experimental results show that the voltage ripple of the midpoint is maintained within around 1.3% of the total dc bus voltage under a neutral current transient of 58 A_{rms} at 50 Hz.

Therefore, the prototyping of the proposed MVB is a promising step towards the success of the ECSEL JU funded project CONNECT. The MVB provides a voltage-stable midpoint to the 20 kVA 3P4W shunt APF, which will be a final deliverable from TU/e to the CONNECT project. In addition, the proposed MVB also has a great potential in bipolar dc micro grid applications.
Acknowledgement

Time is tricky. I had two years lay ahead of me when I entered the TU/e, thinking that would take “forever”, of course in a good way. Now I am at the very end of my PDEng program, summarizing the project, concluding the thesis, worrying about the final project evaluation, and thinking about the journey that I have been gone through.

If it wasn’t for all the help, support, guidance, courage, and inspiration that I have received during the two years of this PDEng program, the completion of the project would not be possible, and I would not be able to fulfill the criteria to be a technological designer. Hence, I would like to express my gratitude to those who have empowered me throughout the program.

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Xinwei Xu 徐新蔚
Eindhoven, August 2019
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The motivations for an ECSEL JU funded project CONNECT, and its affiliated two-year PDEng project is presented in this chapter. The definition, implications, causes of and solutions to voltage imbalance in electric power distribution networks (EPDNs) are discussed. A 20 kVA three-phase four-wire shunt active power filter that is able to compensate the voltage imbalance in EPDNs, is under development by TU/e as a contribution to the CONNECT project. Next, the scope and facts of the PDEng project, midpoint voltage stabilization and its hardware implementation, are presented. An overview of the thesis is given at the end of this chapter.

1. INTRODUCTION

Voltage imbalance in EPDNs
CONNECT project
PDEng project within the CONNECT
Thesis overview
1.1 Voltage imbalance in EPDNs

1.1.1 Definition

Voltage imbalance in an EPDN is a condition in which the rms values of the phase voltages or the phase angle between consecutive phases are not equal [1]. Ideally speaking, the generated three-phase voltage in a power system are purely sinusoidal and equal in magnitude, with a 120-degree phase shift to each other [2]. However, the three-phase voltage at the PCC (point of common coupling) or the distribution end is always unbalanced to some extent due to some practical reasons, which will be covered in section 1.1.3. Figure 1-1 shows a phasor diagram example of a balanced and an unbalanced three-phase voltage.

Figure 1-1. Phasor diagram of a balanced and an unbalanced three-phase voltage.

According to IEEE standard 1159-2009 [3], the voltage imbalance factor (VUF) in a three-phase system is defined as the ratio of the magnitude of the negative sequence component to the magnitude of the positive sequence component, expressed as a percentage.

\[
VUF = \frac{|V_{neg}|}{|V_{pos}|} \times 100\%.
\]  

(1-1)

The positive sequence component creates flux variation in the direction that an electric motor is intended to rotate, while the negative sequence component rotates reversely, creating flux variation in the opposite direction, which produces additional heat in the motor.

It is recommends that the maximum VUF of an EPDN should be less than 2% in IEEE Std. 1159-2009 [3]. This 2% VUF limit also applies to EN standard 50610:2010 and IEC standards 62000-2-2 [4].
1.1.2 Implications

Voltage imbalance poses adverse effects on EPDNs and the connected electrical equipment. It leads to derating of distribution transformers [5, 6], increased power loss in neutral wires [7], thus reducing the capacity of the EPDN [8].

Moreover, voltage imbalance causes derating, reduced efficiency, and decreased lifetime of induction motors that are directly coupled to the grid [2]. In addition, voltage imbalance results in undesirable low-frequency harmonic components on the dc bus voltage of motor drives, which raises the temperature of the dc bus capacitors, thus degrading their predicted lifetimes [9, 10]. Furthermore, voltage imbalance may give rise to possible malfunctions of grid-connected inverters.

1.1.3 Causes

Voltage imbalance at the PCC can generally be attributed to a mismatch of power loads, distributed power generations (DPGs), and impedances across the three phases in the EPDN. The following lists the common causes of voltage imbalance in EPDNs [2, 11, 12]:

1. Load asymmetry (unequal distribution of single-phase loads);
2. Generation asymmetry (unequal distribution of signal-phase DPGs, such as roof-top photovoltaics);
3. Transformer winding asymmetry and distribution feeder impedance asymmetry.

1.1.4 Solutions

Several approaches have been proposed to compensate voltage imbalance in EPDNs [8, 13-17]. One of the approaches is to apply strict regulations on loads and DPGs connected to EPDNs. Only permissible loads/generators can be connected to an EPDN based on their input/output power characteristics. However, hard restrictions on connected electrical equipment lead to a high cost for commercial applications and residential households.

Another approach is manual/dynamical load switching among the three phases based on static transfer switch [13]. Single-phase loads and signal-phase generators are distributed as equally as possible from the beginning of construction. However, user activity varies continually, which creates load asymmetry. In addition, the energy generated from rooftop photovoltaics connected to one phase may vary from their counterparts in different phases, due to the shadow effect in solar panels. Therefore, load switching can cause excessive transients in EPDNs.
An alternative approach is to deploy inverter-based DPGs to compensate voltage imbalance in EPDNs [8, 14-17]. In addition to active power injection, these DPGs are envisaged to compensate negative and zero sequence voltages at a PCC by providing negative and zero sequence currents to an EPDN, so that the current draw from the PCC is balanced. This means that a balanced three-phase voltage is maintained at the PCC, and the power throughput of the EPDN is optimized.

1.2 CONNECT project

1.2.1 Background

Power demand in electric power systems varies from time to time, of which peak level can be significantly higher than average supply level. This means that the capacity of an EPDN needs to be higher than the nominal to deal with the highest possible peak power demand, otherwise electricity blackout may happen. Generally, it is the distribution system operators’ (DSOs) duty to maintain a good power quality in the EPDN under varying power demands.

Over the past years, the number of EVs on the road has increased rapidly due to government subsidies, technical advancements (increased range, lower battery cost), and environmental sensitivity. However, the increasing adoption of EVs is aggravating the peak power demand in EPDNs. This means that more investments need to be made to build more robust EPDNs by DSOs.

For residential users, electricity bill is based on the energy consumed during a certain period. While for residential and industrial users, beside the energy consumption, the electricity bill includes power demand charge, as well as possible penalties for low power quality. These penalties might include low power factor charge and current harmonic charge depends on the region.

In some cases, the power demand charge for industrial users can be as much as half of the total energy bill. Therefore, it is beneficial not just for DSOs but also for energy users to shave off peak power demand of their facilities.

1.2.2 Facts

An ECSEL JU funded project, CONNECT was proposed to deal with peak power demand in an EPDN. CONNECT aims to research, design, develop, and showcase novel solutions
for efficient devices and components of the future smart grid, with the key objective of reducing the peak power demand by at least a factor of two.

The CONNECT project started in April 2017 and has a duration of 36 months. This project is coordinated by Infineon Technologies AG, involving 19 participating organization in 5 European countries (detailed participants list can be found in Appendix A). The CONNECT project receives total funding of 19.9 million euros from ECSEL JU research and innovation action program, as well as from participating countries. Table 1-1 lists a few facts of CONNECT project [18, 19].

<table>
<thead>
<tr>
<th>Project coordinator</th>
<th>Infineon Technologies AG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Website</td>
<td><a href="http://www.connect-ecsel.eu/">http://www.connect-ecsel.eu/</a></td>
</tr>
<tr>
<td>Start date</td>
<td>April 2017</td>
</tr>
<tr>
<td>Duration</td>
<td>36 Months</td>
</tr>
<tr>
<td>Total investment</td>
<td>€ 19.9 M</td>
</tr>
<tr>
<td>Number of participating organizations</td>
<td>19</td>
</tr>
<tr>
<td>Number of countries involved</td>
<td>5</td>
</tr>
</tbody>
</table>

1.2.3 Objectives

The key objective of the CONNECT project is the reduction of the peak power demand by at least a factor of two [18, 19]. Realization of this key objective includes the reduction of power fluctuations inside the EPDN and the reduction of power consumptions and losses. This key objective can be achieved through the development of innovative solutions for three research challenges of the EPDN: power conversion, smart energy management, and communication infrastructure.

In the CONNECT project, specific sub-objectives have been introduced based on these three challenges, and on the implementation of developed solutions, as well as on their dissemination activities. All nine sub-objectives of the CONNECT project are listed as follows:

1. To design power converters with improved efficiency;
2. To develop converters that optimize the power throughput of the EPDN by improved power quality;
3. To reduce the power demand of the EPDN by providing power consumption and generation data to energy users;
4. To reduce the peak demand through load scheduling, cooperation, and micro-grids;
5. To increase the performance of current measurement in future smart grids;
6. To increase the performance of communications in future smart grids;
7. To introduce advanced security measures to the communications in the future smart grids;
8. Implementation and proof-of-concept of CONNECT solutions in practical scenarios;
9. Scientific dissemination and contribution to standardization bodies and fora.

1.2.4 TU/e contribution

EPDNs are normally designed, constructed and rated based on fundamental frequency, balanced and sinusoidal load currents. However, voltage imbalance and voltage harmonic, which are generally caused by non-linear and asymmetrical loads/distributed power generators, lead to higher losses and derating of the power lines and power transformers in EPDNs [6, 20-22].

As one of the participants in the CONNECT project, TU/e is contributing to the objective 2 (to develop power converters that optimize the power throughput of EPDNs by improved power quality) by the design and implementation of a 20 kVA bidirectional 3P4W grid-interfacing dc-ac power converter demonstrator, which is designated as a 20 kVA shunt APF. Table 1-2 lists a few facts of the research project assigned to TU/e. In addition, the detail requirements of the 20 kVA shunt APF are given in Appendix B.

<table>
<thead>
<tr>
<th>Project owner</th>
<th>dr. Jorge Duarte</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start date</td>
<td>April 2017</td>
</tr>
<tr>
<td>Duration</td>
<td>36 months</td>
</tr>
<tr>
<td>Funding from the EU</td>
<td>214 k€ [23]</td>
</tr>
</tbody>
</table>

Table 1-2. Facts of the project: design and implementation of a 20 kVA 3P4W shunt APF.

This 20 kVA 3P4W shunt APF is developed to optimize the power throughput of an EPDN by improving voltage quality of the local power grid. It provides voltage imbalance compensation, harmonic mitigation, and power factor correction\(^1\) to a PCC of the local grid.

Different from conventional shunt APFs in the market, the developed shunt APF does not need load current measurements to perform the control strategy of voltage quality enhancement, which puts it beyond the state-of-the-art.

1.3 PDEng project within the CONNECT

1.3.1 Background

In EPDNs, 3P4W is the most common configuration for residential and industrial users [13]. The fourth wire is connected to the neutral of delta-to-wye transformers and is

\(^1\) The power factor correction depends on the existence of a central energy management system that sends the reactive power command to the 20 kVA 3P4W shunt APF.
grounded periodically [24]. It acts as a return conductor for the mixed single-phase and three-phase loads in the EPDNs, providing a path for the zero-sequence current, so that the phase voltage in the 3P4W EPDNs can be theoretically balanced.

Therefore, the power converter developed for the CONNECT project to improve the power quality of the 3P4W EPDNs must provide a neutral point for the fourth wire. Hence, the research project “design and implementation of a 20 kVA bidirectional 3P4W grid-interfacing dc-ac power converter” is divided into three parts:

1. Midpoint voltage stabilization and its hardware implementation for a 20 kVA 3P4W shunt APF;
2. Advance control strategy of voltage quality enhancement with local current and voltage measurements only based on a 2 kVA 3P4W shunt APF;
3. Implementation of voltage enhancement strategy in a 20 kVA prototype.

Part 1 is designated as a two-year PDEng project, and part 2 is distributed to a PhD candidate, while the remaining work is planned to be carried out by a researcher in the EPE group.

1.3.2 Scope

This two-year PDEng project includes the design, implementation, and verification of a midpoint voltage balancer for the 20 kVA 3P4W shunt APF. The scope of this PDEng project are:

1. Design choice selection of neutral point creation and its possible improvement;
2. Simulation and experimental verification of the proposed midpoint voltage balancer;
3. Passive components design and dimensioning;
4. PCB design and prototyping;
5. Current and voltage signal acquisition;
6. Digital control based on dSPACE MicroLabBox;
7. Participation in project meetings and project dissemination activities (scientific conferences).

1.3.3 Facts

Table 1-3 lists some general facts of the PDEng project. This PDEng project is supervised by dr. Jorge Duarte and started in August 2017 with a duration of 24 months. More detailed information on the PDEng project regarding the problem definition, deliverables, delimitations, planning, stakeholder analysis, risk management and more can be found in the Appendix D: project based management.
Table 1-3. Facts of the PDEng project: midpoint voltage stabilization and its hardware implementation for a 20 kVA 3P4W shunt APF.

<table>
<thead>
<tr>
<th>Project supervisor</th>
<th>dr. Jorge Duarte</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDEng program coordinator</td>
<td>dr. ir. Peter Smulders</td>
</tr>
<tr>
<td>Start date</td>
<td>August 2017</td>
</tr>
<tr>
<td>Duration</td>
<td>24 months</td>
</tr>
<tr>
<td>Budget</td>
<td>unknow</td>
</tr>
<tr>
<td>Number of stakeholders</td>
<td>9</td>
</tr>
</tbody>
</table>

1.4 Thesis overview

While parts of the PDEng project were already published in [25], this thesis extensively covers the work that has been performed during the two-year traineeship. This thesis is organized as follows:

Chapter 2 discusses neutral point configurations of 3P4W shunt APFs in EPDNs. General introductions, advantages, and disadvantages of different configurations are given. A design choice is made based on the scoring of different configurations. At the end of the chapter, a proposed MVB is selected for further implementation.

Chapter 3 presents the design, dimensioning, and selection of neutral inductors and split capacitors for the proposed MVB. The neutral inductors are designed to allow ZVS operation of the MVB in a wide range. While the split capacitors are designed based on a desired range of \( LC \) resonant frequency.

Chapter 4 carries out the analytical modeling of the MVB, in which a discrete-time small-signal model is selected for the control design. An active damping strategy is implemented, by creating a virtual series resistance to the neutral inductors. A dual-loop structure, which consists of an inner current loop and an outer voltage loop, is implemented to regulate the voltage of the neutral point to half of that of the dc bus.

Chapter 5 demonstrates the simulation and experimental verification processes of the MVB under various neutral current settings. The performance of the ASCB configuration is compared to that of the MVB. It is concluded that the MVB stabilizes the midpoint with a voltage ripple being less than 20 V under various asymmetric load conditions.

Chapter 6 gives main conclusions of the thesis as well as recommendations for future work.
Chapter 2

This chapter discusses neutral point configurations of 3P4W shunt APFs in EPDNs. General introduction, advantages, and disadvantages of four three-phase-based neutral point configurations, i.e., the 2-C configuration, the 4-Leg configuration, the ACSB configuration, and the proposed MVB are given. Afterwards, a design choice is made based on the scoring of different neutral point configurations. In the end, the proposed MVB is selected for further implementation of the midpoint voltage stabilization in a 3P4W shunt APF.

2. NEUTRAL POINT CONFIGURATIONS OF 3P4W SHUNT APFS

- Introduction
- 2-C configuration
- 4-Leg configuration
- ACSB configuration
- Proposed MVB
- Design choice selection
- Conclusion
2.1 Introduction

Shunt APFs have been widely employed to deal with voltage imbalance in EPDNs by actively injecting currents to or sinking currents from the PCC [2, 5, 26, 27]. In EPDNs, the compensation of the zero-sequence voltage imbalance requires a neutral wire to inject or sink zero-sequence current component. Therefore, shunt APFs used for voltage imbalance compensation in EPDNs must be constructed in a 3P4W fashion.

Various configurations of 3P4W shunt APFs have been reported, which are categorized into two groups: independent single-phase-based and three-phase-based. For the independent single-phase-based 3P4W shunt APFs, there are 3 single-phase H-bridges [28-30] and 4 single-phase H-bridges [31] configurations. While for the three-phase-based 3P4W shunt APFs, there are conventional split capacitors (2-C) [26, 32-34], four-leg converter (4-Leg) [32, 35-37], and actively controlled split dc bus (ACSB) [38-43] configurations. Figure 2-1 gives an overview of the classification of the configurations in 3P4W shunt APFs.

Independent single-phase based shunt APFs are good candidates for medium-to-high-power applications [44]. This configuration decreases minimum dc link voltage by a factor of 2 and $\sqrt{3}$ compared to that of the 2-C and 4-Leg configuration respectively, which cuts the cost of semiconductor switches used in the shunt APFs. However, the presence of line-frequency transformers and high number of semiconductor switches are considered drawbacks [45]. Even though the independent single-phase based shunt APF can be constructed using isolated dc links [28, 46], so that the line-frequency transformers are not required, the demanded independent dc links significantly increases the control complexity and the system cost.

In the following sections, only three-phase based shunt APF configurations are considered. The shunt APF based on three-phase converter must provide a dc bus midpoint where a neutral wire connects to, so that the zero-sequence current component can be injected to
or sunk from the PCC. In this thesis, the dc bus midpoint is also designated as the neutral point.

### 2.2 2-C configuration

For the 3P4W shunt APF with 2-C configuration, as shown in Figure 2-2, the neutral point is construed by the midpoint of split capacitors. In this configuration, two bulky capacitors \( C_{N1} \) and \( C_{N2} \), normally electrolytic, are employed to form a neutral point, which the fourth wire is connected to. The neutral current keeps charging one of the split capacitors while discharging the other for a certain period.

![Figure 2-2. Neutral point configuration of a 2-C 3P4W shunt APF.](image)

On the one hand, this solution is easy to implement, on the other hand, it associates problem of voltage mismatching across the two split capacitors. Several practical factors, including unequal capacitance, asymmetrical charging of the capacitors, and asymmetrical circuit configuration could cause voltage mismatching between two split capacitors [38]. In addition, if the neutral current contains a dc component, a major voltage mismatching would happen, triggering over-voltage protection or resulting in system failure. Since the midpoint voltage in conventional split dc bus is not actively controlled, high voltage variation of the midpoint is highly probable under severe load asymmetry. As a result, the high midpoint voltage variation adversely affects the current tracking precision of shunt APFs, thus degrading their voltage imbalance compensation performance.

### 2.3 4-Leg configuration

For the 3P4W shunt APF with 4-Leg configuration (see Figure 2-3), the neutral point is construed by the midpoint of an extra switching leg. This configuration was proposed in
[32], adopting an extra switching leg on the top of the three-phase converter. Bulky electrolytic capacitors have been eliminated in the 4-Leg configuration, which contributes to components cost reduction and power density improvement. However, the control of the extra switching leg and the control of the three-phase converter are not decoupled, which increases the development effort.

In the fourth leg of the 3P4W shunt APF with 4-Leg configuration, the voltage potential of the midpoint varies from half the $V_{bus}$ to zero in high frequency. In most low-voltage EPDNs, the neutral wire is connected to the protective earth. Therefore, high-frequency voltage ripples are present over parasitic capacitors (between positive/negative dc bus and ground) [47]. This high frequency voltage ripple causes common-mode currents, being a source of EMC problems. Therefore, adding a large inductor in the neutral wire to reduce the common-mode current in the 4-Leg configuration becomes a common practice [34].

**Figure 2-3. Neutral point configuration of a 4-Leg 3P4W shunt APF.**

### 2.4 ACSB configuration

An alternative configuration, the ACSB, is the combination of the 2-C configuration and the 4-Leg configuration [42], as shown in Figure 2-4. The neutral point is constructed by the midpoint of split capacitors, which is connected to a neural inductor whose current is actively controlled by the fourth switching leg. The control of the fourth switching leg in ACSB is decoupled from the three-phase inverter. Therefore, the 3P4W shunt APF adopting this approach is equivalent to three independent half bridge converters.

Comparison between the 3P4W shunt APF with the 2-C configuration and the ACSB configuration is given in [41], where the ACSB approach can handle 137% more asymmetric current within the defined safe operating limits. However, experimental verification of the ACSB has not been shown.
Note that, the maximum neutral current is twice of the nominal phase current under the worst scenario of asymmetric loads [25]. Therefore, a single-switching-leg design in the ACSB configuration is not adequate. Furthermore, the high frequency (HF) current circulation in the split capacitors could cause overheating to the split capacitors, thus degrading the lifespan of these capacitors.

Figure 2-4. Neutral point configuration of an ACSB (actively controlled split bus) 3P4W shunt APF.

### 2.5 Proposed MVB

A new neutral point configuration based on the ACSB is proposed in the PDEng project. It addresses the problems of bulky electrolytic capacitors, incompetent of dc current component handling, high control effort, EMC problem, and low neutral current handling capacity and so on that are present in the 2-C, 4-Leg and ACSB neutral point configurations.

The circuit diagram of the 3P4W shunt APF with the proposed MVB is shown in Figure 2-5. A dual-switching-leg consisting of IGBT switches $S_7$, $S_8$, $S_9$, and $S_{10}$, have been added to the MVB. Together with two neutral inductors $L_{N1}$ and $L_{N2}$, the MVB actively balances the voltage between two split capacitors, $C_{N1}$ and $C_{N2}$, by moving extra energy stored in one of the capacitors to the other.

Due to the dual-switching-leg configuration and interleaved control in the proposed MVB, current rating of the neutral wire is increased to more than twice of that in the ACSB [25]. In addition, the interleaved control helps to prevent HF current circulation in the split capacitors and facilitate an accurate neutral current tracking. Furthermore, the neutral inductances can be designed in a small value to allow zero crossing of the inductor current so that soft switching of the MVB is ensured under wide operation range without affect the neutral current tracking.
Figure 2-5. Neutral point configuration of a 3P4W shunt APF with a proposed MVB (split dc bus with interleaved control).

2.6 Design choice selection

In order to justify why the proposed MVB is a good candidate for the implementation of midpoint voltage stabilization in 3P4W shunt APFs, a comparison between the 2-C configuration, the 4-Leg configuration, and the ACSB configuration are made in the following. Two groups of criteria, as shown in Table 2-1, are considered during the design choice selection process.

Table 2-1. Measurement criteria for design choice selection.

<table>
<thead>
<tr>
<th>Technical criteria</th>
<th>Non-technical criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus voltage utilization</td>
<td>Power density</td>
</tr>
<tr>
<td>Neutral current dc component handling</td>
<td>Cost of solution</td>
</tr>
<tr>
<td>EMC immunity</td>
<td>Lifespan</td>
</tr>
<tr>
<td>Ease of current rating upgrade</td>
<td>Ease of development</td>
</tr>
<tr>
<td>Midpoint voltage stabilization</td>
<td></td>
</tr>
<tr>
<td>Neutral current handling capacity</td>
<td></td>
</tr>
</tbody>
</table>

Supposing the grid phase-to-neutral rms voltage is $V_g$, then the minimum required dc bus voltage of the 2-C configuration is $2\sqrt{2}V_g$, and the minimum required dc bus voltage of the 4-Leg configuration is $\sqrt{6}V_g$. While for the ASCB configuration and the proposed MVB, the minimum required dc bus voltage is $2\sqrt{2}V_g$. Therefore, the dc bus voltage utilization of the 4-Leg configuration is 15% higher than the other configurations [39]. Since the 3P4W shunt APF with 2-C configuration is not able to process dc component current, the scoring of 2-C configuration in terms of neutral current dc component handling is quite low.

Due to the complexity of quantitively scoring neutral point configurations in terms of all the measurement criteria listed in Table 2-1, scoring is qualitatively given. Figure 2-6 shows a spider graph of the scoring of neutral point configurations in terms of technical
and non-technical measurement criteria. It is possible to conclude that the proposed MVB is a promising design choice from a comprehensive perspective.

![Figure 2-6. Scoring of neutral point configurations in terms of measurement criteria.](image)

### 2.7 Conclusion

The neutral point configurations of 3P4W shunt APFs in the EPDN have been discussed in this chapter. These configurations are classified into two categories: independent single-phase based and three-phase based. The requirement of either line frequency transformers or isolated dc links makes the independent single-phase based configuration less cost-effective. Therefore, only three-phase based neutral point configurations are considered in this chapter.

General introduction and advantages and disadvantages of four three-phase based neutral point configurations, i.e., the 2-C configuration, the 4-Leg configuration, the ACSB configuration, and the proposed MVB are given. Afterwards, the design choice is made based on the scoring of different configurations in terms of several non-technical and technical measurement criteria. In the end, the proposed MVB is selected for further implementation of the midpoint voltage stabilization in a 3P4W shunt APF.
The design, dimensioning, and selection of neutral inductors and split capacitors for the proposed MVB are presented in this chapter. First, the related requirements of the shunt APF are introduced, which sets design constraints for the passive components. Then, due to the topology similarity, the ASCB configuration is chosen for the calculation of the inductance and the capacitance for the ease of analysis. Finally, the design method and the general specifications of the passive components in the proposed MVB are described.

3. PASSIVE COMPONENTS DESIGN

Introduction
Design and dimensioning of neutral inductors
Design and selection of split capacitors
Conclusion
3.1 Introduction

Passive components, such as resistors, inductors, capacitors and transformers, account a large percentage in electronic devices cost-wise, dimension-wise and quantity-wise. A good design of passive components guarantees the optimal operation of electronic circuits.

In power electronics converters, the design, dimensioning, and selection of passive components, especially for the inductors and the capacitors in the main circuits, on the one hand, not just affects the performance, but also the efficiency and the stability of the converter system. On the other hand, the desired performance, efficiency, stability margin, dimension of the power electronics converters constraint the design, dimensioning, and selection of passive components.

3.1.1 Design requirements

This chapter is dedicated to the design, dimensioning, selection of the neutral inductors and split capacitors for the proposed MVB. The design of these passive components is based on the requirements provided in Table 3-1, and the objective of achieving a higher efficiency, as well as a robust control loop.

Table 3-1. Requirements (partial) of the 20 kVA 3P4W shunt APF.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Symbol</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal power</td>
<td>$P_{\text{nom}}$</td>
<td>/</td>
<td>20</td>
<td>/</td>
<td>kVA</td>
</tr>
<tr>
<td>DC bus voltage</td>
<td>$V_{\text{bus}}$</td>
<td>720</td>
<td>760</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>Voltage of split capacitors</td>
<td>$V_{CN1}, V_{CN2}$</td>
<td>360</td>
<td>380</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>AC main frequency</td>
<td>$f_g$</td>
<td>49.5</td>
<td>50</td>
<td>50.5</td>
<td>Hz</td>
</tr>
<tr>
<td>Phase-to-neutral voltage</td>
<td>$V_g$</td>
<td>210</td>
<td>230</td>
<td>250</td>
<td>V$_{\text{rms}}$</td>
</tr>
<tr>
<td>Line current</td>
<td>$I_g$</td>
<td>/</td>
<td>29</td>
<td>33</td>
<td>A$_{\text{rms}}$</td>
</tr>
<tr>
<td>Neutral wire current</td>
<td>$I_N$</td>
<td>/</td>
<td>0</td>
<td>58</td>
<td>A$_{\text{rms}}$</td>
</tr>
<tr>
<td>DC bus midpoint voltage ripple</td>
<td>$\Delta V_{CN2}$</td>
<td>/</td>
<td>20*</td>
<td>80</td>
<td>V</td>
</tr>
</tbody>
</table>

* 20 V is the desired upper limit of the midpoint voltage ripple.

3.1.2 Revisit of the proposed MVB

The circuit diagram of a 3P4W shunt APF with the proposed MVB introduced in Section 2.5 is reproduced in Figure 3-1 for convenience. The 3P4W shunt APF contains two parts, the proposed MVB and the three-phase converter. The former is for neutral point creation and its voltage stabilization. While the latter one is meant for grid interfacing, providing voltage imbalance compensation and dealing with other voltage quality issues of the PCC point [48-50]. As it shown in Figure 3-1, the proposed MVB has two neutral inductors $L_{N1}$, $L_{N2}$, two split capacitors $C_{N1}$, $C_{N2}$, and four IGBT switches $S_7$, $S_8$, $S_9$, $S_{10}$.
In the proposed MVB, two switching legs and two neutral inductors are employed to facilitate interleaved control. Therefore, the neutral current is shared equally in two neutral inductors, decreasing the rms and peak value of current flow in the inductors by a factor of 2.

Figure 3-1. Neutral point configuration of a 3P4W shunt APF with the proposed MVB. Due to the topology resemblance between the MVB and the ACSB, the proposed MVB consisting of dual switching legs with interleaved control can be simplified to an ASCB configuration, for the ease of subsequent analysis. Figure 3-2 provides the circuit diagram of the proposed MVB and its simplified topology. In Figure 3-2 (b), IGBT switch $S_9$, $S_{10}$ and neutral inductor $L_{N1}$ are omitted.

Figure 3-2. Circuit diagram of the proposed MVB. (a) Original topology. (b) Simplified topology for the ease of analysis, which is the same topology as that in the ACSB configuration.

### 3.2 Design and dimensioning of neutral inductors

#### 3.2.1 Design

The purpose of the extra switching leg, as shown in Figure 3-2 (b), is to actively stabilize the voltage of the midpoint to half of the total dc bus voltage by switching on and switching
off \( S_7 \) and \( S_8 \) in a certain pattern. Therefore, during steady state operation, the duty cycle of the \( S_7 \) and \( S_8 \) is 50\%. Since the switching frequency is 20 kHz, the duration of on-state \( T_{on} \) and off-state \( T_{off} \) of \( S_7 \) and \( S_8 \) are

\[
T_{on} = T_{off} = 25 \mu s. \tag{3-1}
\]

The peak-to-peak current ripple on the neutral inductor is given by

\[
\Delta i_{LN2} = \frac{V_{bus}}{2L_{N2}} T_{on}, \tag{3-2}
\]

where \( V_{bus} \) is the voltage of the dc bus.

The total inductor current \( i_L \) in the MVB, as shown in Figure 3-2 (b), tries to track the neutral current \( i_N \), as in

\[
i_L = i_N, \tag{3-3}
\]

so that no charging or discharging current \( i_C \) flows into the split-capacitor branch, thus keeping the voltage of two split capacitors balanced.

If the half of the peak-to-peak current ripple of the inductor is larger than the neutral current \( i_N \), indicated as follows

\[
\frac{\Delta i_{LN2}}{2} \geq i_N, \tag{3-4}
\]

the switches can operate under zero voltage switching (ZVS) condition, which eliminates the turn-on loss of IGBT switches and reverse recovery loss of the anti-paralleled diode.

However, a higher neutral inductor ripple results to higher turn off switching loss and higher conduction loss of the extra switching leg. According to the requirements of in Table 3-1, the maximum neutral current is 58 A_{rms}. If the neutral inductor is designed accordingly to maintain full ZVS operation of the extra switching leg under all neutral current conditions, the inductor ripple current is too high for the MVB to stay power efficient. Instead, the nominal phase current \( I_{g, nom} \) is considered as the neutral current of interest.

Note that the neutral inductor current \( i_{LN1} \) and \( i_{LN2} \) in the proposed MVB equal half of the total inductor current \( i_L \). Thus (3-4) becomes

\[
\frac{\Delta i_{LN2}}{2} \geq \frac{I_{g, nom}}{2}. \tag{3-5}
\]

Substitution of (3-5) into (3-2) yields
Substitution of the corresponding parameters from the requirement Table 3-1 into (3-6) leads to

\[ L_{N2} < 232 \text{ µH.} \tag{3-7} \]

Therefore, the inductance of the neutral inductor \( L_{N2} \) needs to be less than 232 µH to keep ZVS operation of the extra leg under a wide operation range.

Due to the interleaving operation of neutral inductor currents in the proposed MVB, the two inductors should be identical. The inductance is thus chosen with some margin,

\[ L_{N1} = L_{N2} = 220 \text{ µH.} \tag{3-8} \]

### 3.2.2 Dimensioning

The requirements of the neutral inductors are listed in Table 3-2 based on the requirements of the shunt APF and the analysis in section 3.2.1. Due to the high current and high frequency ripple, it is rather improbable to find suitable inductors from off-the-shelf components. Therefore, the neutral inductors used in the proposed MVB have been dimensioned and assembled for the proposed MVB in this PDEng project.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>( L_{N} )</td>
<td>220</td>
<td>µH</td>
</tr>
<tr>
<td>Maximum inductor current</td>
<td>( I_{LN,rms} )</td>
<td>29</td>
<td>A_{rms}</td>
</tr>
<tr>
<td>Ripple of inductor current</td>
<td>( i_{LN,rip} )</td>
<td>41</td>
<td>A_{pp}</td>
</tr>
<tr>
<td>Ripple frequency</td>
<td>( f_{rip} )</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Peak inductor current</td>
<td>( I_{LN,p} )</td>
<td>62</td>
<td>A</td>
</tr>
</tbody>
</table>

Using the product of area approach to dimension the neutral inductor, the area product of the neutral inductors is found to be

\[ A_w A_E = \frac{L_{N} I_{LN,p} I_{LN,rms}}{k_w S_{rms} B_S}, \tag{3-9} \]

where

1. \( A_w \) is the winding area of \( E \) core;
2. \( A_E \) is the effective magnetic cross section;
3. \( k_w \) is the winding factor, normally varies from 0.25 to 0.65 [51];
4. \( S_{rms} \) is maximum allowed current density of cooper wire in \( A_{rms}/\text{mm}^2 \);
5. \( B_S \) is maximum allowed flux density of the selected core material;
Chapter 3 PASSIVE COMPONENTS DESIGN

Considering the commercial availability, the magnetic core E80 B66375G0000X187 from TDK. Figure 3-3 shows the magnetic characteristics and the dimension of this E core. The following values are chosen for further calculation.

\[ k_w = 0.3, \]  
\[ S_{rms} = 5 \text{ A rms/mm}^2, \]  
\[ B_S = 380 \text{ mT}. \]  

Solution of (3-9) yields

\[ A_w A_{E} = 0.694 \times 10^6 \text{ mm}^4. \]  

Figure 3-3. Magnetic characteristics and the dimension of a TDK E80 core.

Based on the magnetic characteristics and the core dimensions given in Figure 3-3, from the effective magnetic cross section \( A_E = 390 \text{ mm}^2 \) and winding window \( A_w = 800 \text{ mm}^2 \), the area product of one pair of E80 core is found to be

\[ A_w A_{E,E80} = 0.312 \times 10^6 \text{ mm}^4. \]  

The minimum pairs \( K_p \) needed for designing neutral inductors is derived as

\[ K_p = \text{ceil} \left( \frac{A_w A_E}{A_w A_{E,E80}} \right) = 3. \]  

The number of turns of the inductors is calculated through

\[ N_T = \text{ceil} \left( \frac{L_{N1}N_p}{B_S K_p A_{E,E80}} \right). \]  

Substitution of (3-16) and values provide in Table 3-2 into (3-17) yields

\[ N_T = 31. \]  

Air gap of the inductor is then derived according to
\[
\sigma = \frac{N_T^2 \mu_0 K_p A_{E,80}}{L_N},
\]  
(3-18)

where \(\mu_0\) is the permeability of free space, \(\mu_0 = 1.257 \times 10^{-6} \text{ H/m}\). Substitution of (3-16), (3-18) and values provides in Table 3-2 into (3-19) yields

\[
\sigma = 7.7 \text{ mm}.
\]  
(3-19)

The results of the dimensioning of the neutral inductors are summarized in Table 3-3.

Figure 3-4 shows the photo of the neutral inductors made for the proposed MVB.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>(L_{N1}, L_{N2})</td>
<td>220</td>
<td>(\mu)H</td>
</tr>
<tr>
<td>Quantity</td>
<td>/</td>
<td>2</td>
<td>/</td>
</tr>
<tr>
<td>Number of E80 core set</td>
<td>/</td>
<td>3</td>
<td>/</td>
</tr>
<tr>
<td>Number of turns</td>
<td>(N_T)</td>
<td>31</td>
<td>/</td>
</tr>
<tr>
<td>Air gap</td>
<td>(\sigma)</td>
<td>7.7</td>
<td>mm</td>
</tr>
<tr>
<td>Low-frequency resistance @50Hz</td>
<td>/</td>
<td>36</td>
<td>m(\Omega)</td>
</tr>
<tr>
<td>High-frequency resistance @20kHz</td>
<td>/</td>
<td>76</td>
<td>m(\Omega)</td>
</tr>
<tr>
<td>Weight</td>
<td>/</td>
<td>1580</td>
<td>g</td>
</tr>
</tbody>
</table>

Figure 3-4. Photo of the neutral inductors made for the proposed MVB.

### 3.3 Design and selection of split capacitors

#### 3.3.1 2-C configuration

When the dual switching legs in the MVB are disabled, in this case, the total neutral inductor current \(i_L\) is regarded as 0. Therefore, the proposed MVB is equivalent to a 2-C configuration. Provided with the peak neural current \(I_{N,\text{peak}}\) and the maximum allowable midpoint voltage ripple \(\Delta V_{CN2,\text{max}}\), the capacitance \(C_{N1}\) and \(C_{N2}\) in the 2-C configuration is derived through [25]
\[ C_{N1} = C_{N2} = \frac{I_{N,\text{peak}}}{2\pi f_g \Delta V_{CN2,\text{max}}} \int_0^{\frac{1}{f_g}} \sin(2\pi f t) dt. \] (3-20)

Solution of (3-21) yields

\[ C_{N1} = C_{N2} = \frac{I_{N,\text{peak}}}{2\pi f_g \Delta V_{CN2,\text{max}}}, \] (3-21)

where \( f_g \) is the grid frequency (\( f_g = 50 \) Hz).

Substitution of the peak values of neutral current and the maximum allowable voltage ripple provided in Table 3-1 into (3-22) leads to

\[ C_{N1} = C_{N2} = 3300 \, \mu F. \] (3-22)

However, substitution of the peak neutral current and the desired voltage ripple (20 V) provided in Table 3-1 into (3-22) leads to

\[ C_{N1} = C_{N2} = 13000 \, \mu F. \] (3-23)

Therefore, it is concluded that 2-C configuration suffers from the fact that it needs bulky electrolytic capacitors, which limits the power density and the life expectancy of the midpoint voltage balancer. Table 3-4 lists parameters of 2-C configuration in various papers for comparison, where the capacitance of the split capacitors ranges from 1500 µF to 4000 µF.

<table>
<thead>
<tr>
<th>Article</th>
<th>( P_{\text{nom}} ) (kW)</th>
<th>( V_{\text{bus}} ) (V)</th>
<th>( f_{\text{sw}} ) (kHz)</th>
<th>( C_{N1}, C_{N2} ) (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kumar, and Sreenivas (2016) [54]</td>
<td>N.A.</td>
<td>900</td>
<td>12</td>
<td>1500</td>
</tr>
<tr>
<td>Lin, Z., et al. (2018) [55]</td>
<td>9</td>
<td>700</td>
<td>10</td>
<td>4000*</td>
</tr>
</tbody>
</table>

1. N.A. means such information is not provided in the paper.
2. * The value of dc link capacitance from Lin, Z., et al. (2018) [55] in this table is an estimation, since it is not directly provided in the paper.

### 3.3.2 Proposed MVB

In the ACSB configuration and the proposed MVB, the neutral current is conditioned by the extra switching legs. These extra switching legs keep the neutral inductor current tracking the neutral current, thus in principle, no charging or discharging current flows
into the dc bus midpoint, which guarantees the voltage balance between the two split capacitors. Therefore, the capacitance of the split capacitors in the ACSB configuration and the proposed MVB can be much smaller.

Before investigating the split capacitors in the proposed MVB, parameters of split capacitors and neutral inductors in various paper regarding ACSB configuration are listed in Table 3-5 for comparison. According to the Table 3-5, the capacitance of the split capacitors in ASCB configuration varies from 25 µF up to 6600 µF.

Supposing the dc bus voltage $V_{\text{bus}}$ is constant, the ACSB is equivalent to a buck converter [42]. The output inductor is the same as the neutral inductor in the ASCB, while the capacitance $C_N$ of the output capacitor equals to

$$C_N = C_{N1} + C_{N2}. \quad (3-24)$$

Table 3-5. Parameters of ACSB configuration in papers regarding split capacitors and neutral inductors.

<table>
<thead>
<tr>
<th>Article</th>
<th>$P_N$ (kW)</th>
<th>$V_{\text{bus}}$ (V)</th>
<th>$f_{\text{sw}}$ (kHz)</th>
<th>$C_{N1}, C_{N2}$ (µF)</th>
<th>$C_{\text{bus}}$ (µF)</th>
<th>$L_N$ (mH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zhong, Q.-C., et al. (2005)</td>
<td>N.A.</td>
<td>900</td>
<td>10</td>
<td>4000</td>
<td>/</td>
<td>10</td>
</tr>
<tr>
<td>Zhong, Q.-C., et al. (2006)</td>
<td>30</td>
<td>800</td>
<td>10</td>
<td>6600</td>
<td>/</td>
<td>2.5</td>
</tr>
<tr>
<td>Srikanthan (2010) [58]</td>
<td>N.A.</td>
<td>320</td>
<td>0.625</td>
<td>2200</td>
<td>/</td>
<td>50</td>
</tr>
<tr>
<td>Hornik and Zhong (2013) [59]</td>
<td>N.A.</td>
<td>N.A.</td>
<td>5</td>
<td>1000</td>
<td>N.A.</td>
<td>2.85</td>
</tr>
<tr>
<td>Dharmadhikari, et al. (2014)</td>
<td>N.A.</td>
<td>750</td>
<td>500</td>
<td>500</td>
<td>/</td>
<td>0.2</td>
</tr>
<tr>
<td>Bozalakov, D., et al. (2017)</td>
<td>N.A.</td>
<td>400</td>
<td>20</td>
<td>2000</td>
<td>/</td>
<td>0.666</td>
</tr>
<tr>
<td>Zhao, W., et al. (2017) [42]</td>
<td>10</td>
<td>800</td>
<td>10</td>
<td>250</td>
<td>4000*</td>
<td>2.8</td>
</tr>
</tbody>
</table>

1. The power converters proposed in [58] and [40] are three-level converters.
2. * The value of dc-link capacitance from Zhao, W., et al. (2017) [42] in this table is an estimation, since it is not directly provided in the paper.

Therefore, the resonant frequency of the $LC$ branch in the ACSB, and in the proposed MVB is found to be

$$f_{\text{res,LC}} = \frac{1}{2\pi\sqrt{L_N\left(C_{N1} + C_{N2}\right)}}, \quad (3-25)$$

where $L_N$ is the neutral inductor in the ACSB configuration, or one of the neutral inductors in the proposed MVB.

Table 3-6 lists out the resonant frequency of the $LC$ branch in the ACSB configuration in various papers. According to the Table 3-6, the resonant frequency is roughly 100 times smaller than the switching frequency. In addition, the resonant frequency deviates from
the grid fundamental frequency and its low-order harmonic frequencies. However, the resonant frequencies in [39], [60], and [61], corresponding to 450 Hz, 356 Hz, and 98 Hz respectively, are too close to the 9th, 7th and 2nd harmonic frequencies, which might cause instability of the system.

Since the proposed MVB is designed for the 20 kVA 3P4W shunt APF, which provides voltage imbalance compensation and harmonic mitigation to the PCC in the EPDN. It is expected that the neutral wire conducts current of fundamental frequency and its harmonic frequencies. Since maximum harmonic order under mitigation of the 20 kVA 3P4W shunt APF is 11th (Table C-1 in Appendix B), the neutral wire will conduct harmonics current up to 11th order.

### Table 3-6. Resonant frequency of the LC branch in ACSB configuration.

<table>
<thead>
<tr>
<th>Article</th>
<th>$C_{N1}$, $C_{N2}$ (μF)</th>
<th>$L_N$ (mH)</th>
<th>$f_{sw}$ (kHz)</th>
<th>$f_{res,LC}$ (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mishra, M. K., et al. (2003) [38]</td>
<td>2200</td>
<td>200</td>
<td>1.8</td>
<td>0.005</td>
</tr>
<tr>
<td>Zhong, Q.-C., et al. (2005) [56]</td>
<td>4000</td>
<td>10</td>
<td>10</td>
<td>0.018</td>
</tr>
<tr>
<td>Zhong, Q.-C., et al. (2006) [57]</td>
<td>6600</td>
<td>2.5</td>
<td>10</td>
<td>0.028</td>
</tr>
<tr>
<td>Liang, J., et al. (2009) [39]</td>
<td>25</td>
<td>2.5</td>
<td>10</td>
<td>0.450</td>
</tr>
<tr>
<td>Srikanthan and Mishra (2010) [58]</td>
<td>2200</td>
<td>50</td>
<td>0.625</td>
<td>0.011</td>
</tr>
<tr>
<td>Hornik and Zhong (2013) [59]</td>
<td>1000</td>
<td>2.85</td>
<td>5</td>
<td>0.067</td>
</tr>
<tr>
<td>harmadhikari, et al. (2014) [60]</td>
<td>500</td>
<td>0.2</td>
<td>500</td>
<td>0.356</td>
</tr>
<tr>
<td>Bozalakov, D., et al. (2017) [61]</td>
<td>2000</td>
<td>0.666</td>
<td>20</td>
<td>0.098</td>
</tr>
<tr>
<td>Zhao, W., et al. (2017) [42]</td>
<td>250</td>
<td>2.8</td>
<td>10</td>
<td>0.135</td>
</tr>
<tr>
<td>Fu, Y., et al. (2018) [62]</td>
<td>220</td>
<td>0.12</td>
<td>50</td>
<td>0.693</td>
</tr>
</tbody>
</table>

Therefore, the resonant frequency of the LC branch in the proposed MVB needs to be higher than 550 Hz and significantly smaller than the switching frequency of 20 kHz. The range of the resonant frequency is chosen as

$$550 \text{ Hz} \leq f_{res,LC,MVB} \leq 1000 \text{ Hz}. \quad (3-26)$$

In the most cases, two split capacitors are identical. Solution of (3-26) yields

$$C_{N1} = C_{N2} = \frac{1}{2L_N \left(2\pi f_{res,LC,MVB}\right)^2}. \quad (3-27)$$

Substitution of (3-27) into (3-28) yields

$$57.6 \text{ μF} \leq C_{N1} = C_{N2} \leq 190.3 \text{ μF}. \quad (3-28)$$

Based on the result from (3-29), the capacitance of the split capacitors in the proposed MVB is chosen as

$$C_{N1} = C_{N2} = 100 \text{ μF}. \quad (3-29)$$
According to (3-26), the $LC$ resonant frequency is now

$$f_{\text{res},LC} = 759 \text{ Hz.} \quad (3-30)$$

Compared to that of the 2-C configuration, the capacitance in the proposed MVB is about 30 times smaller.

Considering the high ESR and relatively low lifetime of electrolytic capacitors, two film capacitors, part number FFVE6K0107K from AVX, are selected. Figure 3-5 shows the photo of the split capacitors used in the proposed MVB.

![Figure 3-5. Photo of the split capacitors used in the proposed MVB.](image)

### 3.4 Conclusion

The design, dimensioning, and selection of neutral inductors and split capacitors for the proposed MVB have been presented in this chapter. To start with, several requirements of the shunt APF are specified, which sets design constraints for the passive components. Due to the topology similarity, the ACSB configuration is chosen for calculation of the required inductance and the capacitance for the ease of analysis.

Afterwards, the neutral inductors are designed to allow ZVS operation of the IGBT switches, when the neutral current is less than the nominal phase current. In the end, the split capacitors are designed based on the desired range of $LC$ resonant frequency. The general specifications of the passive components in the proposed MVB are summarized in Table 3-7.

#### Table 3-7. Specifications of the neutral inductors and split capacitors in the proposed MVB.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neutral inductor</td>
<td>$L_{N1, N2}$</td>
<td>220</td>
<td>µH</td>
</tr>
<tr>
<td>Inductor series resistor</td>
<td>$R_{LN1, LN2}$</td>
<td>76</td>
<td>mΩ</td>
</tr>
<tr>
<td>Inductor current rating</td>
<td>$I_{L,\text{nom}}$</td>
<td>29</td>
<td>A$_{\text{rms}}$</td>
</tr>
<tr>
<td>Split capacitor</td>
<td>$C_{N1, N2}$</td>
<td>100</td>
<td>µF</td>
</tr>
<tr>
<td>Specification</td>
<td>Symbol</td>
<td>Value</td>
<td>Unit</td>
</tr>
<tr>
<td>-------------------------------------------</td>
<td>--------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>Capacitor equivalent series resistor (ESR)</td>
<td>$R_{Cn1}, R_{Cn2}$</td>
<td>1.35</td>
<td>mΩ</td>
</tr>
<tr>
<td>Capacitor voltage rating</td>
<td>$V_{C_{nom}}$</td>
<td>600</td>
<td>V</td>
</tr>
</tbody>
</table>
The analytical modeling and the control design of the MVB are carried out in this chapter. A discrete-time small-signal modeling is applied for loop controller design. An active damping strategy is implemented to deal with the $LC$ resonance by creating a virtual series resistance to the neutral inductors. Finally, a dual-loop control, which consists of an inner current loop and an outer voltage loop, is employed to regulate the voltage of the midpoint.

4. MODELING AND CONTROL OF THE MVB

- Introduction
- Modeling of the MVB
- Damping strategy of $LC$ resonance
- Dual loop control
- Conclusion
4.1 Introduction

Control of power converters means that firing pulse width modulation (PWM) signals to the semiconductor switches in a certain manner, usually based on the current and voltage measurements, so that the converters operate in a desired fashion. A simple, yet accurate mathematic model, which represents the behavior of a power converter, is the cornerstone of the control design. As with many other modern power converters, the proposed MVB is regulated by digital control, in which the signal acquisition happens in a finite sampling rate, and the firing of PWM signals lag from the sampling instant.

In this chapter, the analytical modeling of the proposed MVB and its control design is presented. An active damping is proposed to deal with the resonance in the LC network. In addition, a dual-loop control, which consists of an inner current loop and an outer voltage loop, is employed to regulate the voltage of the midpoint. A system overview of the

Figure 4-1. System overview of the 20 kVA 3P4W shunt APF with the proposed MVB.

In this chapter, the analytical modeling of the proposed MVB and its control design is presented. An active damping is proposed to deal with the resonance in the LC network.
20 VA 3P4W shunt APF with the MVB is shown in Figure 4-1, in which the shunt APF is broken down into 3 layers: main circuit, interface, and control algorithm.

In the main circuit layer, the 3P4W shunt APF contains two parts: the proposed MVB and a three-phase converter. The former is designed for neutral point creation and its voltage stabilization, while the latter one provides voltage imbalance compensation, harmonic mitigation, and power factor correction to the PCC. Since the grid interfacing strategy and the voltage quality enhancement control are not the scope of this thesis, a grey box is used for a demonstration purpose only.

The interface layer deals with the digital signal acquisition of currents and voltages at various nodes, as well as the gate signal generation for the IGBT switches in the shunt APF.

In the control algorithm layer, the total inductor current reference $i_{L,ref}[k]$ is generated through the voltage controller $G_{c,v}(z)$ based on the voltage measurements of the split capacitors and the current measurement of the neutral wire. This reference is then divided equally into two parts, regulating each neutral inductor current through the current controllers, $G_{c,ILN1}(z)$ and $G_{c,ILN2}(z)$, in a way that the total inductor current tracks the neural current without introducing high-frequency ripple to the midpoint. Therefore, the midpoint voltage of the 3P4W shunt APF is actively controlled to a certain level, which is half of the total dc bus voltage.

### 4.2 Modeling of the MVB

According to Table 3-7, the series resistance of the neutral inductors is 76 mΩ, and the ESR of the split capacitors is 1.35 mΩ. Therefore, the simplified circuit topology of the MVB is reproduced in Figure 4-2, where the series resistors of the neutral inductors are included, while the ESRs of split capacitors are neglected.

Applying KCL at the neutral point $N$, one gets

$$i_{LN2} + C_{N1} \frac{d(V_{bus} - v_{CN2})}{dt} = i_N + C_{N2} \frac{dv_{CN2}}{dt}. \quad (4-1)$$

Supposing the dc bus voltage $V_{bus}$ is constant, (4-1) is rewritten as

$$i_{LN2} - i_N = (C_{N1} + C_{N2}) \frac{dv_{CN2}}{dt}. \quad (4-2)$$

Therefore,
where \( i_L = i_{LN2} \), \( C_N = C_{N1} + C_{N2} \).
where the neutral inductor current $i_L$ and the neutral voltage $v_{CN}$ are selected both as the state vector $x(t)$ and the output vector $y(t)$, while the dc bus voltage $V_{bus}$ and the neutral current $i_N$ are considered as the input vector $v(t)$.

![Equivalent Circuit Diagram](image)

Figure 4-4. Two topological states of the equivalent circuit of the MVB. (a) When $S_7$ is on. (b) When $S_8$ is on.

The state-space description of the two topological states are shown as

**State 1: $S_7$ is on and $S_8$ is off**

\[
\begin{align*}
L_N \frac{di_L}{dt} &= -R_{LN}i_L - v_{CN} + V_{bus}, \\
C_N \frac{dv_{CN}}{dt} &= i_L - i_N
\end{align*}
\]

(4-5)

\[
\begin{align*}
\frac{d}{dt}
\begin{bmatrix}
i_L \\
v_{CN}
\end{bmatrix}
&= \begin{bmatrix}
-R_{LN}/L_N & -1/L_N \\
1/C_N & 0
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_{CN}
\end{bmatrix}
+ \begin{bmatrix}
1/L_N \\
0
\end{bmatrix}V_{bus} - \begin{bmatrix}
0 \\
-1/C_N
\end{bmatrix}i_N.
\end{align*}
\]

(4-6)

**State 2: $S_7$ is off and $S_8$ is on**

\[
\begin{align*}
L_N \frac{di_L}{dt} &= -R_{LN}i_L - v_{CN2}, \\
C_N \frac{dv_{CN}}{dt} &= i_L - i_N
\end{align*}
\]

(4-7)

\[
\begin{align*}
\frac{d}{dt}
\begin{bmatrix}
i_L \\
v_{CN}
\end{bmatrix}
&= \begin{bmatrix}
-R_{LN}/L_N & -1/L_N \\
1/C_N & 0
\end{bmatrix}
\begin{bmatrix}
i_L \\
v_{CN}
\end{bmatrix}
+ \begin{bmatrix}
0 \\
0
\end{bmatrix}V_{bus} - \begin{bmatrix}
0 \\
-1/C_N
\end{bmatrix}i_N.
\end{align*}
\]

(4-8)
The averaged state-space model is then obtained by averaging (4-6) and (4-8) over one switching period, as shown as

\[
\frac{d}{dt} \begin{bmatrix} i_{LN} \\ V_{CN} \end{bmatrix} = \begin{bmatrix} \frac{R_{LN}}{L_N} & -\frac{1}{L_N} \\ \frac{1}{C_N} & 0 \end{bmatrix} \begin{bmatrix} i_{LN} \\ V_{CN} \end{bmatrix} + \begin{bmatrix} \frac{u}{L_N N_c} \\ 0 \end{bmatrix} \begin{bmatrix} V_{bus} \\ i_N \end{bmatrix} \],
\]

(4-9)

where \( u \) is the control command, from which the duty cycle of \( S_7 \) is derived, and \( N_c \) is the amplitude of a digital carrier signal.

Afterwards, the input vector and the state vector are perturbed considering their stationary value with a superimposed variation, as shown in (4-10) and (4-12),

\[
\begin{align*}
\dot{v}_{bus} &= V_{bus} + \dot{v}_{bus} \\
\dot{i}_N &= I_N + \dot{i}_N \\
u &= U + \dot{u}
\end{align*}
\]

(4-10)

\[
\begin{align*}
\dot{i}_L &= I_L + \dot{i}_L \\
\dot{V}_{CN} &= V_{CN} + \dot{V}_{CN}
\end{align*}
\]

(4-11)

Neglecting the contribution of the second order perturbation, the averaged small-signal state-space representation of the equivalent circuit of the MVB is shown as

\[
\frac{d}{dt} \begin{bmatrix} \dot{i}_L \\ \dot{v}_{CN} \end{bmatrix} = \begin{bmatrix} \frac{R_{LN}}{L_N} & -\frac{1}{L_N} \\ \frac{1}{C_N} & 0 \end{bmatrix} \begin{bmatrix} \dot{i}_L \\ \dot{v}_{CN} \end{bmatrix} + \begin{bmatrix} \frac{U}{L_N N_c} \\ 0 \end{bmatrix} \begin{bmatrix} \dot{V}_{bus} \\ \dot{i}_N \end{bmatrix},
\]

\[
\begin{bmatrix} \dot{i}_L \\ \dot{v}_{CN} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \dot{i}_L \\ \dot{V}_{CN} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \dot{V}_{bus} \\ \dot{i}_N \end{bmatrix}.
\]

(4-12)

\[4.2.2 \text{ Discrete-time small-signal modeling}\]

The discrete-time small-signal modeling presented in this section is based on the practice in [63], which was derived from the perturbation and linearization of the sampled converter state vector in the vicinity of the converter operating point. The yielded small-signal state-space description is shown as
\[
\hat{x}[k+1] = \Phi \hat{x}[k] + \gamma \hat{u}[k],
\]
\[
\hat{y}[k] = \delta \hat{x}[k],
\]
where
\[
\hat{x}[k] = x[k] - X,
\]
\[
\hat{u}[k] = u[k] - U,
\]
\[
\hat{y}[k] = y[k] - Y,
\]
are the small-signal components of the sampled state vector, control command, and output vector, in relation to their dc components \(X\), \(U\), and \(Y\) respectively. Matrices \(\Phi\) and \(\gamma\) are the small-signal state matrix and the small-signal control-to-state matrix. In addition, matrix \(\delta\) represents the output matrix [63].

According to [63], the small-signal state matrix \(\Phi\), the small-signal control-to-state matrix \(\gamma\), and the small-signal output matrix \(\delta\) under symmetrical modulation are derived by

\[
\Phi = e^{A_0 \frac{T}{2} (1-D)} e^{A_1 DT} e^{A_0 \frac{T}{2} (1-D)},
\]
\[
\gamma = \frac{T}{2N_e} e^{A_0 \frac{T}{2} (1-D)} (F_1 + e^{A_1 DT} F_t),
\]
\[
\delta = C_0,
\]
where
\[
F_1 = (A_1 - A_0) X_t + (B_1 - B_0) V,
\]
\[
F_t = (A_1 - A_0) X_t + (B_1 - B_0) V,
\]
and
\[
X_t = \left( I - e^{A_1 DT} e^{A_0 (1-D)T_e} \right)^{-1} \left[ -e^{A_0 DT} A_0^{-1} \left( I - e^{A_1 DT} T_e \right) B_0 - A_1^{-1} \left( I - e^{A_1 DT} T_e \right) B_1 \right] V,
\]
\[
X_t = e^{A_0 (1-D)T_e} X_t - A_0^{-1} \left( I - e^{A_0 (1-D)T_e} \right) B_0 V.
\]

In (4-15) to (4-17), \(A_1\) and \(A_0\), \(B_1\) and \(B_0\), \(C_1\) and \(C_0\) are the state matrices, the input matrices, and the output matrices of the two topological states of the equivalent circuit depicted in Figure 4-4, respectively. These matrices are given in the following:

\[
A_1 = A_0 = \begin{bmatrix}
-\frac{R_N}{L_N} & -\frac{1}{L_N} \\
\frac{1}{C_N} & 0
\end{bmatrix},
\]
Therefore, a discrete-time small-signal model of the equivalent circuit of the MVB can be obtained based on (4-13), from which the control-to-output transfer functions, such as control to neutral inductor current and control to neutral point voltage can be derived.

4.2.3 Comparison

Based on the analysis of section 4.2, the specifications of passive components (see Table 3-7) and digital control of the MVB (see Table 4-1), the control to neutral point voltage transfer function $G_{u,v}$ and the control to neutral inductor current transfer function $G_{u,i}$ are derived as

$$G_{u,v}(s) = \frac{6.91e06}{s^2 + 331.8s + 2.27e07},$$
$$G_{u,i}(s) = \frac{1382s}{s^2 + 331.8s + 2.27e07},$$
$$G_{u,v}(z) = \frac{0.0086 (z+0.99)}{(z^2 - 1.93z + 0.98)},$$
$$G_{u,i}(z) = \frac{0.068 (z-1)}{(z^2 - 1.93z + 0.98)},$$

where $G_{u,i}(s)$ and $G_{u,v}(s)$ represent the transfer functions in $s$ domain, while $G_{u,i}(z)$ and $G_{u,v}(z)$ represent the transfer functions in $z$ domain.

The bode plots of the control to neutral point voltage transfer functions are shown in Figure 4-5, where both the averaged and the discrete-time model are depicted. In general, the discrete model and the averaged model shows a good match in terms of the control to neutral point voltage transfer function. However, the discrete model predicts extra phase lag at high frequencies, due to the modulation delay. Note that a resonant occurs at 759 Hz in the magnitude plot, causing a 180-degree phase shift in the phase plot.
Table 4-1. Specifications of digital control of the MVB.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>( f_{sw} )</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>( f_{samp} )</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Sampling cycle</td>
<td>( T_s )</td>
<td>50</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>Amplitude of digital carrier signal</td>
<td>( N_c )</td>
<td>2500</td>
<td>/</td>
</tr>
<tr>
<td>Control command at steady state</td>
<td>( U )</td>
<td>1250</td>
<td>/</td>
</tr>
<tr>
<td>Modulation delay</td>
<td>( T_{d,m} )</td>
<td>25</td>
<td>( \mu s )</td>
</tr>
</tbody>
</table>

Figure 4-5. Bode plots of control to neutral point voltage transfer function of the equivalent circuit of the MVB: a comparison between the averaged model \( G_{u,v}(s) \) and the discrete-time model \( G_{u,v}(z) \).

Figure 4-6 shows the bode plots of the control to neutral inductor current transfer functions derived in s domain and z domain. Same as in Figure 4-5, a resonant occurs at 759 Hz, causing a 180-degree phase shift in the phase plot. Beside the extra phase lag at high frequencies, the discrete model also differs from the averaged model at low frequencies. The continuous-time average model predicts a zero at the origin, while a finite, non-zero value is predicted by the discrete-time model [63].

The extra phase lag of the discrete-time model at high frequencies can be represented by adding a loop delay to the averaged model. Therefore, the design of the digital voltage controller for the proposed MVB can depend on the control to neutral voltage transfer function derived from the averaged model. Due to the violation of small-aliasing approximation in the averaged model, substantial differences exist in the control to neutral...
inductor current transfer functions between the discrete-time model and the average model. However, no simple correction is available to improve the prediction of the averaged model at low frequencies [63]. Therefore, in the MVB, the design of the digital current controller, which relies on the digital sampling of current signals, is based on the discrete-time model that properly considers the aliasing effects.

![Bode plots of control to neutral inductor current transfer function of the equivalent circuit of the MVB: a comparison between the averaged model $G_{u,i}(s)$ and the discrete-time model $G_{u,i}(z)$.](image)

Figure 4-6. Bode plots of control to neutral inductor current transfer function of the equivalent circuit of the MVB: a comparison between the averaged model $G_{u,i}(s)$ and the discrete-time model $G_{u,i}(z)$.

### 4.3 Damping strategy of LC resonance

Due to the existence of $LC$ network in the proposed MVB, a resonance peak occurs at the frequency, which is defined in (3-26). As shown in the Figure 4-5 and Figure 4-6, the bode plots predicts a resonance and a 180-degree phase shift at 759 Hz. This resonance may lead to system instability, causing oscillations of the neutral inductor current and the neutral point voltage. Therefore, the resonance in the MVB must be damped to ensure a robust current and voltage control.

#### 4.3.1 Passive damping

Passive damping in $LC$ network is a straightforward strategy to suppress resonance. It is implemented by adding a resistor to the inductor branch or the capacitor branch. This
means that the passive damping has four configurations: a resistor in series with the neutral inductor, a resistor in parallel to the neutral inductor, a resistor in series with the split capacitor, and a resistor in parallel to the split capacitor.

Figure 4-7. Bode plots of the open-loop control to neutral inductor current transfer function of the equivalent circuit under different damping resistance, which is in series with the neutral inductor.

Figure 4-7 shows the bode plots of the open loop control to neutral inductor current transfer function of the equivalent circuit of the MVB under various damping resistance. The extra damping resistance is achieved by adding a resistor $R_p$ in series to the neutral inductor, which is rather simple to implement. According to the bode plots, the resonant peak is damped by the extra resistance (from 0 Ω to 20 Ω) added to the neutral inductor, and the current loop remains stable and robust.

However, due to the direct adoption of physical resistor in the inductor branch or the capacitor branch, passive damping may introduce unacceptable power loss to power converters, especially for those in high-power applications [64, 65].

4.3.2 Active damping

An alternative strategy is active damping, which adopts an extra feedback loop though the measurement of inductor current or capacitor current to mimic the mechanism of passive damping. As with passive damping, active damping also has four configurations: a
virtual resistor in series with the neutral inductor, a virtual resistor in parallel to the neutral inductor, a virtual resistor in series with the split capacitor, and a virtual resistor in parallel to the split capacitor.

All four configurations of active damping can suppress the \( LC \) resonant, while damping performance varies. Compared to other three configurations, adding a virtual resistor in series with the neutral inductor has a higher gain at low-frequency and a higher attenuation at high-frequency [66]. In addition, the interleaved control is employed in the proposed MVB, which means that the measurement of inductor currents is a must. Therefore, the active damping configuration by adding a virtual resistor in series with the neutral inductor is more beneficial.

Figure 4-8 shows the control block diagram of a neutral inductor current loop of one switching leg of the proposed MVB, where \( G_{c,i}(z) \) is the current controller, \( G_{u,i}(z) \) is the plant, and \( H_{ILN}(z) \) is the gain of the neutral current measurement.

![Figure 4-8. Control block diagram of the neutral inductor current loop.](image)

The active damping is implemented by feeding back the neutral inductor current to the control command \( u[k] \) with a damping coefficient \( H_{i,damp}(z) \),

\[
H_{i,damp}(z) = \frac{R_a}{K_{PWM}}, \tag{4-23}
\]

where \( R_a \) is the neutral inductor equivalent series resistance of the active damping, and \( K_{PWM} \) is the converter gain from the control command \( u[k] \) to the midpoint voltage of one switching leg. Based on (4-23), it is concluded that the damping coefficient is a proportional gain, thus \( H_{i,damp}(z) = H_{i,damp} \).

In this thesis, \( K_{PWM} \) is defined as the ratio of the dc bus voltage \( V_{bus} \) and the amplitude of the digital counter \( N_c \), which is used to generate a symmetrical carrier waveform of 20 kHz,

\[
K_{PWM} = \frac{V_{bus}}{N_c}, \tag{4-24}
\]
The neutral inductor current loop depicted in Figure 4-8 is simplified by solving the active damping loop, as shown in Figure 4-9. Generally, the gain of the current measurement \( H_{IL}(z) \) is normalized to 1. Therefore, the open-loop gain of the neutral inductor current loop without compensation is

\[
T_{i,o}(z) = \frac{G_{u,i}(z)}{1 + G_{u,i}(z)H_{i,damp}}.
\]

Figure 4-9. Simplified control diagram of the neutral inductor current loop.

Figure 4-10 shows the bode plots of the open-loop gain \( T_{i,o}(z) \) under various virtual resistance, ranging from 0 Ω to 8 Ω. According to (4-23) and (4-24), the damping coefficient \( H_{i,damp} \) varies from 0 to 26.3. Note that, when the virtual resistance is higher than 9 Ω, the closed neutral inductor current loop without compensation becomes unstable. As shown in the bode plots, with the increment of the virtual resistance \( R_o \), the resonance peak decreases, and the sudden phase shift is mitigated.
4.3.3 Design choice selection

A suitable damping coefficient contributes to a reduced resonant peak and a mitigated sudden phase shift. However, an inappropriate design of the damping coefficient leads to instability of the current loop. In this section, the design choice selection for the damping coefficient in active damping is presented.

In order to select an optimum damping coefficient for the current loop, the closed loop transfer function \( T_{i,c}(z) \) without compensation is derived as

\[
T_{i,c}(z) = \frac{T_{i,c}(z)}{1 + T_{i,c}(z)} = \frac{G_{u,i}(z)}{1 + (1 + H_{i,damp})G_{u,i}(z)}.
\] (4-26)

Since the effect of the damping coefficient variation to the close loop stability is the interest of this section, it is convenient to rewrite the closed loop transfer function \( T_{i,c}(z) \) as

\[
T_{i,c}(z) = \frac{G_{u,i}(z)}{1 + k_{damp}G_{u,i}(z)},
\] (4-27)

where \( k_{damp} = 1 + H_{i,damp} \).

In root locus design method, effect of feedback gain variation to closed loop stability can be illustrated. Therefore, a range of suitable damping coefficient \( H_{i,damp} \) can be determined by analyzing the root locus plot of \( G_{u,i}(z) \) as function of \( k_{damp} \) with the help from MATLAB.

Figure 4-11 shows the root locus plot of \( G_{u,i}(z) \), in which \( k_{damp} \) corresponds to the feedback gain. As shown in the figure, all poles of \( T_{i,c}(z) \) fall inside the unity plane if \( k_{damp} \) is less than 28.8. This means that the range of \( H_{i,damp} \), in which the stability of the closed neutral inductor current loop without compensation can be maintained, is

\[-1 \leq H_{i,damp} \leq 27.8. \] (4-28)

With the objective to achieve damping higher than 0.707, the range of \( H_{i,damp} \) becomes

\[3.3 \leq H_{i,damp} \leq 14.1. \] (4-29)

Substitution of (4-29) into (4-23), yields a suitable range of the virtual resistance,

\[1.0 \ \Omega \leq R_2 \leq 4.3 \ \Omega. \] (4-30)
Figure 4-11. Root locus plot of $G_{u,i}(z)$ as function of $k_{\text{damp}}$, which ranges from 0 to 28.8.

In order to damp the resonance as fast as possible, the closed loop poles of $T_{i,c}(z)$ in the unity plane is expected to deviate away from the 1+0i point as much as possible. Even though the pole in the green line can travel far away, the point P (see Figure 4-11) indicates the furthest point that the pole in the blue line can deviate.

Considering the damping and speed requirements, the P point is an optimum pole positioning of the closed loop $T_{i,c}(z)$. This means that the P point represents the optimum damping coefficient selection for the active damping of the LC resonance. At the P point, $k_{\text{damp}}$ equals 5.9, which means

$$H_{i,\text{damp}} = 4.9 \ \Omega.$$  \hspace{1cm} (4-31)

Substitution of (4-31) into (4-23), yields

$$R_u = 1.5 \ \Omega.$$  \hspace{1cm} (4-32)

Therefore, a damping coefficient of 4.9 is chosen, which corresponds to a virtual resistance of 1.5 Ω. This damping coefficient is embedded in the neutral inductor current loop to secure a stable and robust MVB.
4.4 Dual loop control

The ultimate objective of the control design of the MVB is to guarantee the stability of the converter system with a certain margin while performing voltage regulation of the midpoint. Control of midpoint voltage balancers can be implemented by a single voltage loop [39, 42, 43], or dual loops [25, 38, 41, 47], which consists of an inner current loop and an outer voltage loop.

Since the MVB is proposed for the 20 kVA 3P4W shunt APF, which provides voltage imbalance compensation and voltage harmonic mitigation at PCC, the current on the fourth wire is expected to fluctuate. It is essential for the MVB to have a fast respond.

Interleaving of dual switching legs of the MVB does not necessarily requires the measurement of the inductor currents. However, without the current feedback control in the dual switching legs, significant low-frequency current circulation might occur due to circuit and control asymmetry in the switching legs.

![Digital dual-loop control of the equivalent circuit of the MVB.](image)

Therefore, the control of the MVB is implemented in a dual-loop fashion. The current loop directly steers the neutral inductor current, guaranteeing a balanced current sharing in the two neutral inductors. It also ensures a fast transient respond and provides a current...
limit protection of the converter system. The voltage loop regulates the voltage of the midpoint to half of that of the dc bus. It sets the current reference for the current loop. In addition, the voltage loop delivers compensation to the current loop when additional voltage variation on the midpoint is introduced.

The digital dual-loop control of the equivalent circuit of the MVB is shown in Figure 4-12, in which the circuit topology, signal acquisitions, and the loop configuration are illustrated. As shown in the figure, the inner current loop receives its current reference \( i_{L,\text{ref}}[k] \) from the voltage loop controller \( G_{c,v}(z) \) and the neutral current signal acquisition \( i_{N,\text{samp}}[k] \).

Since the current loop responds much faster than the voltage loop, these two control loops can be considered as two decoupled loops. Therefore, the controller design of the current loop and the voltage loop are carried out separately in the following sections.

### 4.4.1 Current loop

The control block diagram of the digital dual-loop control of the equivalent circuit of the MVB is shown in Figure 4-13, from which the open-loop gain of the current loop \( T_{i,o}(z) \) is derived as

\[
T_{i,o}(z) = G_{c,i}(z) H_{iL}(z) \frac{G_{u,i}(z)}{1 + G_{u,i}(z) H_{i,damp}}.
\]  

(4-33)

where \( G_{c,i}(z) \) is the current loop controller to be designed, \( H_{i,damp} \) is the LC resonance damping coefficient, and \( H_{iL}(z) \) is the neutral inductor current sampling gain, which is generally normalized to 1.
The control to neutral inductor current transfer function \( G_{u,i}(z) \) was derived through the discrete-time model presented in Section 4.2.2, and was shown in (4-22). Rewrite \( G_{u,i}(z) \) as

\[
G_{u,i}(z) = \frac{0.068(z - 1)}{(z^2 - 1.93z + 0.98)}.
\] (4-34)

The uncompensated current loop gain is derived through (4-33), shown as

\[
T_{i,o,\text{uncom}}(z) = \frac{G_{u,i}(z)}{1 + G_{u,i}(z)H_{i,damp}}.
\] (4-35)

\[
T_{i,o,\text{uncom}}(z) = \frac{0.068(z - 1)}{z^2 - 1.60z - 0.65}.
\] (4-36)

Figure 4-14 shows the bode plots of \( T_{i,o,\text{uncom}} \), whose gain is negative throughout the frequency range from dc to 10 kHz, and whose phase decays from 180 degrees to -180 degrees.

Figure 4-14. Bode plots of the uncompensated and the compensated current loop gain, as well as the current compensator (PI controller).

Considering the sampling frequency of the MVB, a crossover frequency \( \omega_{c,i} \) of 2 kHz is desired to achieve a fast loop response. In addition, a phase margin of 50 degrees is anticipated to reach a robust loop.
In this thesis, a digital PI controller $G_{i,pi}(z)$ is selected for the current loop compensation, and it is implemented by the forward Euler discretization, shown as

$$G_{c,i}(z) = G_{i,pi}(z) = K_{i,pi,p} + K_{i,pi,i} \frac{1}{z - 1}. \quad (4-37)$$

With the aid of MATLAB Control System Designer, the parameters of proportional gain $K_{i,pi,p}$ and the integral gain $K_{i,pi,i}$ are calculated as

$$K_{i,pi,p} = 6.0, \quad K_{i,pi,i} = 4.4. \quad (4-38)$$

Substitution of (4-38) into (4-37), yields

$$G_{c,i}(z) = \frac{6z - 1.6}{z - 1}. \quad (4-39)$$

The bole plots of the current controller and the compensated current loop gain are also presented in Figure 4-14. Due to the magnitude boost introduced by the PI controller, the compensated current loop gain exhibits a phase margin of 50 degrees at 2 kHz and a positive gain margin of 15.8 dB at the Nyquist frequency.

A finite gain of the compensated current loop gain in low frequency is due to the cancellation of the pole of the PI controller (see (4-39)) and the zero of the control to current transfer function $G_{u,i}(z)$ (see (4-22)). The finite loop gain can be addressed by adding an extra integrator to the current loop. However, the introduction of another integrator part in the current loop requires extra computation effort.

Fortunately, in the dual-loop control system considered here, any regulation error in the inner current loop is compensated by the outer voltage loop, which adjusts the current reference accordingly. Therefore, the finite loop gain in the PI compensated current loop is acceptable in the digital dual-loop control of the MVB.

### 4.4.2 Voltage loop

Generally, in dual-loop control, the inner loop responds much faster than the outer loop, so that the two loops are decoupled. Therefore, the control design of the voltage loop can be separated from the current loop by considering a unit gain of the closed current loop. This method is beneficial when no computer-added tools are available, and still gives relatively good results. With the help of MATLAB, however, the close loop gain of the current loop is fully considered during the control design of the voltage loop.
The equivalent transformation of the control block diagram of the digital dual-loop control, which is shown in Figure 4-13, is presented in Figure 4-15. The current loop with an active damping implemented lies inside the voltage loop.

![Control Block Diagram](image)

Figure 4-15. Equivalent transformation of the control block diagram of the digital dual-loop control.

The open-loop gain of the active damping $T_{ad,o}(z)$ is

$$T_{ad,o}(z) = H_i \text{damp} G_{u,i}(z),$$  (4-40)

and the closed loop transfer function of the active damping $G_{ad,c}(z)$ is
\[ G_{ad,c}(z) = \frac{1}{1 + T_{ad,o}(z)} = \frac{1}{1 + H_{damp}G_{u,i}(z)}. \]  

(4-41)

Therefore, the open-loop gain of the current loop \( T_{i,o}(z) \) is

\[ T_{i,o} = G_{c,i}(z)G_{ad,c}(z)G_{u,i}(z)H_{il}(z), \]

(4-42)

and the closed loop transfer function of the current loop \( G_{i,c}(z) \) is

\[ G_{i,c}(z) = \frac{G_{u,i}(z)G_{ad,c}(z)}{1 + G_{c,i}(z)G_{ad,c}(z)G_{u,i}(z)H_{il}(z)}. \]

(4-43)

According to Figure 4-15 (d), the open-loop gain of the voltage loop \( T_{v,o}(z) \) is derived as

\[ T_{v,o}(z) = G_{c,v}(z)G_{i,c}(z)G_{u,v}(z)H_{CN2}(z). \]

(4-44)

Generally, the gain of voltage measurement \( H_{CN2}(z) \) is normalized to 1. This means that the uncompensated open-loop gain of the voltage loop \( T_{v,o,\text{uncom}}(z) \) can be simplified into

\[ T_{v,o,\text{uncom}}(z) = G_{i,c}(z)G_{u,v}(z), \]

(4-45)

and in view of (4-22),

\[ T_{v,o,\text{uncom}}(z) = \frac{0.052(z + 0.99)(z - 0.27)}{(z - 1)(z^2 - 1.18z + 0.54)}. \]

(4-46)

Figure 4-16 shows the bode plots of the \( T_{v,o,\text{uncom}}(z) \), whose crossover frequency \( \omega_{c,v} \) is 728 Hz. Note that the crossover frequency of the current loop \( \omega_{c,i} \) is 2 kHz, which is not much faster than the uncompensated voltage loop. Therefore, a crossover frequency of 200 Hz for \( T_{v,o}(z) \) is selected considering the crossover frequency of the current loop. In addition, a phase margin of 60 degrees is anticipated.

Following the same steps as in the current controller design, a digital PI controller \( G_{v,\text{pi}}(z) \) is selected for voltage loop compensation, shown as

\[ G_{c,j}(z) = G_{v,\text{pi}}(z) = K_{v,\text{pi,p}} + K_{v,\text{pi,i}} \frac{1}{z - 1}. \]

(4-47)

With the aid of the MATLAB Control System Designer, the parameters of proportional gain \( K_{v,\text{pi,p}} \) and the integral gain \( K_{v,\text{pi,i}} \) are found to become

\[ K_{v,\text{pi,p}} = 0.27 \ \Omega, \]

\[ K_{v,\text{pi,i}} = 0.01 \ \Omega. \]

(4-48)

Substitution of (4-48) into (4-47), yields
\[ G_{c,i}(z) = \frac{0.27z - 0.26}{z - 1}. \] (4-49)

Bode plots of the voltage controller \( G_{c,\text{pi}}(z) \) and the compensated voltage loop gain \( T_{v,o}(z) \) are depicted in Figure 4-16 as well. \( G_{c,\text{pi}}(z) \) increases the loop gain at low frequencies, while decreases the loop gain at high frequencies. It reshapes the voltage loop to reach the desire crossover frequency and the desired phase margin.

![Bode plots](image)

Figure 4-16. Bode plots of the uncompensated and the compensated voltage loop gain, as well as the voltage compensator (PI controller).

### 4.5 Summary

In order to verify the control design of the current loop and the voltage loop, the corresponding closed loop bode plots and the closed loop step responses are presented at Figure 4-18 and Figure 4-19 respectively. According to Figure 4-18 and Figure 4-19, the magnitude of the output current only manifests 84.4% (-1.47 dB) of that of the input current reference at 50 Hz. In dual loop control, however, regulation error in the inner loop can be compensated by the outer loop, which adjusts the reference for the inner loop. In addition, the current loop reacts fast to the input changes, reaching the steady state at 1.2 ms under a step signal excitation.
The voltage loop regulates the voltage of the neutral point to half of the dc bus voltage. It is required that the neutral point voltage ripple is less than 80 V, which is 10% of the maximum dc bus voltage. It is also desired that in nominal operation the voltage ripple is less than 20 V, being 5% of the maximum midpoint voltage.

Figure 4-18 shows the bode plot of the closed voltage loop, in which the loop gain is 1.02 dB at 50 Hz and below 0 dB when the frequency is more than 200 Hz. This means that the voltage input references of 50 Hz, 150 Hz will be amplified, while the input references whose frequencies are 250 Hz, 350 Hz, 450 Hz and 550 Hz will be attenuated.

It is beneficial to attenuate all the ac components in the voltage input reference, so that the voltage ripple of the midpoint can be further reduced. Nevertheless, the attenuation
of low frequency ac signals requires a low bandwidth voltage loop, which limits the dynamic performance of the voltage loop. An alternative solution is to embed notch filters at specific frequencies. However, inclusion of notch filters complicates the control loop.

Since the reference input for the voltage loop predominantly consists of a dc component, the employment of a digital PI controller, which reshapes the crossover frequency of voltage loop to 200 Hz, is a simple, yet effective solution to reach a stabilized midpoint voltage within a voltage ripple of 20 V. In addition, according to Figure 4-18, the voltage loop responds relatively fast under a step signal input, reaching the steady state within one grid cycle with a 23.5% overshoot.

### 4.6 Conclusion

The analytical modeling and the control design of the MVB have been carried out in this chapter. First, a simplified circuit topology of the MVB is derived for the ease of analysis. Next, the averaged small-signal model and the discrete-time small-signal model of the simplified circuit are constructed and compared, from which the discrete-time model is selected for the control design of the MVB. Due to the resonance in the \( LC \) network, an active damping strategy is implemented, by creating a virtual series resistance to the neutral inductors.

Finally, a dual-loop structure is employed to control the MVB. The inner current loop, which is compensate by a PI controller, responds fast to the reference input and the variation of the neutral current, while the voltage loop, which is also compensated by a PI controller, corrects the regulation error of the current loop. All the control parameters derived in this chapter for the digital dual-loop control of the MVB are summarized in Table 4-2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
<td>( f_{\text{amp}} )</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Active damping coefficient</td>
<td>( H_{\text{damp}} )</td>
<td>4.9</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Virtual resistance</td>
<td>( R_d )</td>
<td>1.5</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Current loop crossover frequency</td>
<td>( \omega_{c,i} )</td>
<td>2</td>
<td>kHz</td>
</tr>
<tr>
<td>Voltage loop crossover frequency</td>
<td>( \omega_{c,v} )</td>
<td>0.2</td>
<td>kHz</td>
</tr>
<tr>
<td>Proportional gain of the current controller</td>
<td>( K_{i,\text{pi,p}} )</td>
<td>6.0</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Integral gain of the current controller</td>
<td>( K_{i,\text{pi,i}} )</td>
<td>4.4</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Proportional gain of the voltage controller</td>
<td>( K_{c,\text{pi,p}} )</td>
<td>0.27</td>
<td>( \Omega^{-1} )</td>
</tr>
<tr>
<td>Integral gain of the current controller</td>
<td>( K_{c,\text{pi,i}} )</td>
<td>0.01</td>
<td>( \Omega^{-1} )</td>
</tr>
</tbody>
</table>
The simulation and experimental verifications of the proposed MVB under various neutral current settings are demonstrated in this chapter. The performance of the ASCB configuration is compared to that of the MVB. The MVB demonstrates a doubled neutral current handling capacity at 50 Hz, and it shows less HF current circulation in the split-capacitor branch. It is concluded that the MVB stabilizes the dc bus midpoint of the 3P4W shunt APF with a voltage ripple being less than 20 V under various asymmetric load conditions.

## 5. SIMULATION AND EXPERIMENTAL VERIFICATION

**Introduction**

**Simulation verification**

**Experimental verification**

**Conclusion**
5.1 Introduction

The proposed MVB, which adopts a dual-switching-leg, actively stabilizes the dc bus midpoint voltage by moving extra energy stored from one of the split capacitors to the other. Because of the dual-switching-leg arrangement and the interleaved control, the neutral current handling capacity of the MVB is doubled compared to that of the ACSB configuration. In addition, the interleaved control prevents HF current circulation in the split capacitors branch. Furthermore, the MVB operates under ZVS condition when the neutral current is less than the nominal phase current, which is 29 $A_{\text{rms}}$.

To verify the performance of the proposed MVB, computer simulations and experimental tests are carried out. The performance of the ACSB configuration has also been investigated, and the results are compared with those of the MVB in terms of midpoint voltage stability, neutral current handling capacity, and the HF current ripple content.

Both simulation and experimental results of the ACSB configuration and the MVB are presented under the maximum neutral current conditions. These conditions are defined based on the maximum rating of the converter system, the desired midpoint voltage ripple, and the harmonic mitigation requirement which demands the shunt APF to respond to harmonic orders up to 11th.

5.1.1 Maximum ratings of the MVB and the ACSB configuration

When one phase of the shunt APF sinks the nominal current from the PCC, and the other two phases inject the nominal current to the PCC, or vice versa, the shunt APF operates under the worst asymmetric load. The neutral current becomes 58 $A_{\text{rms}}$, being twice of the nominal phase current, and the current unbalance factor (IUF) [67], in this case, is 200%.

However, the ACSB configuration, which adopts a single-switching-leg, can only process a neutral current up to 33 $A_{\text{rms}}$. This means that the ACSB configuration provides limited voltage imbalance compensation under the worst asymmetric load, while the voltage imbalance compensation capability of the proposed MVB is not compromised. Table 5-1 lists the maximum ratings of the ACSB configuration and the MVB.

<table>
<thead>
<tr>
<th>Description</th>
<th>MVB</th>
<th>ACSB</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum phase current</td>
<td>33</td>
<td>33</td>
<td>$A_{\text{rms}}$</td>
</tr>
<tr>
<td>Maximum neutral wire current</td>
<td>66</td>
<td>33</td>
<td>$A_{\text{rms}}$</td>
</tr>
<tr>
<td>Voltage imbalance correction capacity*</td>
<td>100</td>
<td>50</td>
<td>%</td>
</tr>
</tbody>
</table>

* The voltage imbalance capability mentioned above is specified under the worst asymmetric load condition, where a 58 $A_{\text{rms}}$ zero-sequence current is presented in the neutral wire.
5.1.2 Simulation and experimental parameters

The general simulation and experimental parameters of the ACSB configuration and the MVB are listed in Table 5-2. All the parameters in Table 5-2 are consistent with the analysis in the previous chapters. During harmonic mitigation operation, the shunt APF injects or sinks harmonics current to or from the PCC. Therefore, it is possible that the neutral wire conducts harmonic current from the 3rd order up to the 11th order.

Table 5-2. Simulation parameters of the ACSB configuration and the proposed MVB.

<table>
<thead>
<tr>
<th>General parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus voltage</td>
<td>$V_{bus}$</td>
<td>760</td>
<td>V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{sw}$</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>$f_{samp}$</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Nominal power of the APF</td>
<td>$P_{nom}$</td>
<td>20</td>
<td>kVA</td>
</tr>
<tr>
<td>Grid phase-to-neutral voltage</td>
<td>$V_{g}$</td>
<td>230</td>
<td>V rms</td>
</tr>
<tr>
<td>Proportional gain of the current controller</td>
<td>$K_{i,pi,p}$</td>
<td>6.0</td>
<td>Ω</td>
</tr>
<tr>
<td>Integral gain of the current controller</td>
<td>$K_{i,pi,i}$</td>
<td>4.4</td>
<td>Ω</td>
</tr>
<tr>
<td>Proportional gain of the voltage controller</td>
<td>$K_{v,pi,p}$</td>
<td>0.27</td>
<td>Ω$^{-1}$</td>
</tr>
<tr>
<td>Integral gain of the current controller</td>
<td>$K_{v,pi,i}$</td>
<td>0.01</td>
<td>Ω$^{-1}$</td>
</tr>
<tr>
<td>Split capacitor</td>
<td>$C_{N1}, C_{N2}$</td>
<td>100</td>
<td>µF</td>
</tr>
<tr>
<td>Desired upper limit of the midpoint voltage ripple</td>
<td>$\Delta V_N$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Harmonic orders of the neutral current</td>
<td>$h_i$</td>
<td>3, 5, 7, 9, 11</td>
<td>/</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ACSB configuration</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neutral inductors</td>
<td>$L_{N1}, L_{N1}$</td>
<td>220</td>
</tr>
<tr>
<td>Inductor series resistors</td>
<td>$R_{LN1}, R_{LN2}$</td>
<td>76</td>
</tr>
<tr>
<td>Proposed MVB</td>
<td>Value</td>
<td>Unit</td>
</tr>
<tr>
<td>Neutral inductor</td>
<td>$L_N$</td>
<td>220</td>
</tr>
<tr>
<td>Inductor series resistor</td>
<td>$R_{LN}$</td>
<td>76</td>
</tr>
</tbody>
</table>

5.2 Simulation verification

The simulations are carried out in MATLAB/Simulink environment, and a discrete-time solver with a sample time of 0.5 µs is selected. Note that only simulations, from which the midpoint voltage ripple satisfies the desired upper limit (20 V), are presented and discussed. In addition, the simulation results, in which the frequency of the neutral current is 50 Hz, 150 Hz, or 250 Hz, are presented visually in waveforms. While for the neutral current with the 7th, the 9th and the 11th harmonic orders, the simulation results are summarized in Table 5-3.

5.2.1 ACSB configuration

Figure 5-1 shows simulation results of the ACSB configuration under an asymmetric load, which injects a neutral current of 30 A rms at 50 Hz to the midpoint. These results include
the three-phase output currents $i_a$, $i_b$ and $i_c$, the neutral inductor current $i_{LN}$, the neutral current $i_N$, the charging and discharging current of the split capacitors $i_C$, and the voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. A load transient is added at 0.5 s to demonstrate the fast-dynamic performance.

![Simulation results](image)

Figure 5-1. Simulation results of the ACSB configuration under an asymmetric load, which injects a neutral current of $30 \, A_{rms}$ at 50 Hz to the midpoint point. (a) Three-phase output currents $i_a$, $i_b$ and $i_c$. (b) Comparison of the neutral current $i_N$ and the inductor current $i_{LN}$. (c) Charging and discharging current of the split capacitors $i_C$. (d) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. Note that the midpoint or the neutral point voltage of the ACSB is the same as the split capacitor voltage $v_{CN2}$. As shown in Figure 5-1 (d), the voltages of the split capacitors $v_{CN1}$ and $v_{CN2}$ are stabilized with a voltage ripple being around 10 V, which meets the desired voltage ripple requirement in Table 5-2.

However, due to the phase current limitation ($33 \, A_{rms}$) and the existence of high current ripple in the neutral inductor, the maximum neutral current $i_N$ that the ACSB can handle is $30 \, A_{rms}$. This is approximately 50% of the neutral current under the worst asymmetric load. Moreover, the neutral inductor current $i_{LN}$ introduces HF current ripple (20 kHz) to the split capacitors, while tracking the neutral current $i_N$, as shown in Figure 5-1 (b). As a result, the HF ripple, which is close to 50 A_{pp}, passes to the charging and discharging current of split capacitors $i_C$, as shown in Figure 5-1 (c). This HF ripple current circulates through the split-capacitors branch, causing additional midpoint voltage variation as well as possible overheating of the split capacitors.
Figure 5-2. Simulation results of the ACSB configuration under a harmonic asymmetric load, which injects a neutral current of 30 A rms @150 Hz to the midpoint point. (a) Three-phase output currents $i_a$, $i_b$, and $i_c$. (b) Comparison of the neutral current $i_N$ and the inductor current $i_{LN}$. (c) Charging and discharging current of the split capacitors (d) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$.

Figure 5-3. Simulation results of the ACSB configuration under a harmonic asymmetric load, which injects a neutral current of 29 A rms @250 Hz to the midpoint point. (a) Three-phase output currents $i_a$, $i_b$, and $i_c$. (b) Comparison of the neutral current $i_N$ and the inductor current $i_{LN}$. (c) Charging and discharging current of the split capacitors (d) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$.

Figure 5-2 and Figure 5-3 present the simulation results of the ACSB configuration under harmonic asymmetric loads, corresponding to a neutral current injection of 30 A rms at 150 Hz and a neutral current injection of 29 A rms at 250 Hz, respectively. The voltage of
the split capacitors in both cases is stabilized with a voltage ripple less than 20 V, which meets the desired ripple limit. As with the previous simulation, the maximum neutral current the ASCB can handle is also approximately 50% of the neutral current under the worst asymmetric load. In addition, a close-to-50 A peak HF ripple exits in the charging and discharging current of the split capacitors.

Table 5-3 summarizes the simulation results of the ASCB configuration under various neutral current injections, ranging from 30 A rms at 50 Hz, 30 A rms at 150 Hz, 29 A rms at 250 Hz, 28 A rms at 350 Hz, 21 A rms at 450 Hz and 15 A rms at 550 Hz. These frequencies of the neutral currents are selected based on the harmonic mitigation requirement of the 3P4W shunt APF, and the RMS values are limited by the maximum current rating of the neutral wire and the desired midpoint voltage ripple.

Table 5-3. Simulation results of the ACSB configuration under various neutral currents.

<table>
<thead>
<tr>
<th>Neutral current [iN]</th>
<th>Neutral inductor current [iLN]</th>
<th>Midpoint voltage ripple [VΝ,pp]</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 A rms @050 Hz</td>
<td>33 A rms</td>
<td>10 V</td>
</tr>
<tr>
<td>30 A rms @150 Hz</td>
<td>33 A rms</td>
<td>15 V</td>
</tr>
<tr>
<td>29 A rms @250 Hz</td>
<td>33 A rms</td>
<td>18 V</td>
</tr>
<tr>
<td>28 A rms @350 Hz</td>
<td>33 A rms</td>
<td>20 V</td>
</tr>
<tr>
<td>21 A rms @450 Hz</td>
<td>27 A rms</td>
<td>20 V</td>
</tr>
<tr>
<td>15 A rms @550 Hz</td>
<td>22 A rms</td>
<td>20 V</td>
</tr>
</tbody>
</table>

5.2.2 Proposed MVB

The maximum neutral current that the proposed MVB can handle is increased by 100% compared to that of the ACSB configuration, because of the employment of a dual-switching-leg. Therefore, the proposed MVB can fully compensate the voltage imbalance even under the worst load asymmetry.

Figure 5-4 shows the simulation results of the MVB under the worst asymmetric load condition, in which a neutral current of 58 A rms at 50 Hz is injected to the neutral point. These results include the three-phase output currents $i_a$, $i_b$ and $i_c$, the neutral current $i_N$, the neutral inductor currents $iLN1$ and $iLN1$, the total inductor current $iL$, the charging and discharging current of the split capacitors $iC$, and the voltage of the split capacitors $vCN1$ and $vCN2$. A load transient is added at 0.5 s to demonstrate the fast-dynamic performance.

Due to the interleaving control of the dual-switching-leg in the MVB, the ripple currents of the two neutral inductors counteract with each other, as shown in Figure 5-4 (c). As a result, the HF ripple in the total inductor current $iL$ is decreased significantly, and the total inductor current $iL$ tracks the neutral current $iN$ smoothly, as shown in Figure 5-4 (d).
Only a small amount of HF ripple current, approximately 8 $A_{pp}$, propagates to the midpoint, as shown in Figure 5-4 (e).

The voltages of the split capacitors $v_{CN1}$ and $v_{CN2}$ are stabilized with a voltage ripple less than 10 V (see in Figure 5-4 (f)). This means that the midpoint voltage meets the requirement of the voltage ripple in Table 5-2.

![Simulation results of the proposed MVB under the worst asymmetric load condition](image)

Figure 5-4. Simulation results of the proposed MVB under the worst asymmetric load condition, in which a neutral current of 58 $A_{rms}$ @50 Hz is injected to the midpoint point. (a) Three-phase output current $i_a$, $i_b$ and $i_c$. (b) Neutral current $i_N$. (c) Neutral inductor current $i_{LN1}$ and $i_{LN2}$. (d) Comparison of the neutral current $i_N$ and the total inductor current $i_L$. (e) Charging and discharging current of the split capacitors $i_C$ (f) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$.

The simulation results of the MVB under harmonic asymmetric loads are presented in Figure 5-5 and Figure 5-6, in which a neutral current injection of 58 $A_{rms}$ at 150 Hz and a neutral current injection of 36 $A_{rms}$ at 250 Hz are simulated to verify the MVB. The voltage of the split capacitors in both cases is stabilized with a voltage ripple around 20 V. As with the previous simulations, the interleaving of the dual-switching-leg counteracts most of the HF ripple through the total inductor, so that only a small amount of HF ripple current, approximately 8 $A_{pp}$, propagates to the midpoint.
Figure 5-5. Simulation results of the proposed MVB under a harmonic asymmetric load, which injects a neutral current of 58 A\textsubscript{rms} @150 Hz to the midpoint point. (a) Three-phase output current \(i_a, i_b\) and \(i_c\). (b) Neutral current \(i_N\). (c) Neutral inductor current \(i_{LN1}\) and \(i_{LN2}\). (d) Comparison of the neutral current \(i_N\) and the total inductor current \(i_L\). (e) Charging and discharging current of the split capacitors \(i_C\) (f) Voltage of the split capacitors \(v_{CN1}\) and \(v_{CN2}\).

Table 5-4 summarizes the simulation results of the MVB under various neutral current injections, ranging from 58 A\textsubscript{rms} at 50 Hz, 58 A\textsubscript{rms} at 150 Hz, 36 A\textsubscript{rms} at 250 Hz, 24 A\textsubscript{rms} at 350 Hz, 18 A\textsubscript{rms} at 450 Hz and 10 A\textsubscript{rms} at 550 Hz. These frequencies of the neutral currents are selected based on the harmonic mitigation requirement of the 3P4W shunt APF, and the RMS values are limited by the maximum current rating of the neutral wire and the desired midpoint voltage ripple.

<table>
<thead>
<tr>
<th>Neutral current [i\textsubscript{N}]</th>
<th>Neutral inductor current [i\textsubscript{LN1}, i\textsubscript{LN2}]</th>
<th>Midpoint voltage ripple [V\textsubscript{N,pp}]</th>
</tr>
</thead>
<tbody>
<tr>
<td>58 A\textsubscript{rms} @50 Hz</td>
<td>31 A\textsubscript{rms}</td>
<td>10 V</td>
</tr>
<tr>
<td>58 A\textsubscript{rms} @150 Hz</td>
<td>31 A\textsubscript{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>36 A\textsubscript{rms} @250 Hz</td>
<td>22 A\textsubscript{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>24 A\textsubscript{rms} @350 Hz</td>
<td>18 A\textsubscript{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>18 A\textsubscript{rms} @450 Hz</td>
<td>16 A\textsubscript{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>10 A\textsubscript{rms} @550 Hz</td>
<td>14 A\textsubscript{rms}</td>
<td>20 V</td>
</tr>
</tbody>
</table>
Figure 5-6. Simulation results of the proposed MVB under a harmonic asymmetric load, which injects a neutral current of 36 $A_{\text{rms}}$ @250 Hz to the midpoint point. (a) Three-phase output current $i_a$, $i_b$ and $i_c$. (b) Neutral current $i_N$. (c) Neutral inductor current $i_{LN1}$ and $i_{LN2}$. (d) Comparison of the neutral current $i_N$ and the total inductor current $i_L$. (e) Charging and discharging current of the split capacitors $i_C$. (f) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$.

5.3 Experimental verification

A 20 kVA 3P4W shunt APF prototype, as shown in Figure 5-7, has been built to verify the proposed MVB. The prototype adopts two SEMIKRON three-phase IGBT power modules, and five IGBT gate drivers SKYPER 42 LJ R. An external dc power supply provides a constant voltage to the input of the prototype. Experimental tests have been carried out in an off-grid mode, where the various neutral currents are generated by sending unbalanced three-phase current references.
The signal acquisitions and control implementation are realized in a dSPACE MicroLabBox, which contains a processor domain and a FPGA domain, as shown in Figure 5-8. In the MicroLabBox, control model configuration is dealt with in the processor domain, and demanding computation is implemented in the FPGA domain.

PCB boards, an interface board, a few measurement boards, and several over-current and over-voltage boards, are built in this project. The interface board provides a hub for the MicroLabBox, the measurement boards, protection boards, and gate drivers. On the one hand, the measured current and voltage signals are loaded to the MicroLabBox for the dual-loop control, on the other hand, these signals are directly fed into the protection boards for over-current and over-voltage hardware protection.

The system overview of the 20 kVA 3P4W shunt APF under test is shown in Figure 5-9, where the interactions between current and voltage measurements, signal acquisition, control signal generation, and driver signal generation are demonstrated. The MicroLabBox is connected to a PC, which configures the control model for the shunt APF in the MATLAB/Simulink environment. A 30 kW three-phase resistive load is connected to the shunt APF to verify the effectiveness of the proposed MVB under various neutral currents.
5.3.1 The ACSB configuration

Figure 5-10 and Figure 5-11 show the experimental results of the ASCB configuration under an asymmetric load, which inject a neutral current of 31 A_{rms} at 50Hz to the neutral point. These results include the neutral inductor current $i_{LN}$, the neutral current $i_N$, total dc bus voltage $V_{bus}$, and the voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. A load transient is added at $t=2.187$ s to evaluate the dynamic performance.

Because of the maximum phase current limitation (see Table 5-1), the ASCB configuration, which adopts a single-switching-leg, can only process a neutral current up to 31 A_{rms}, which corresponds to a 33 A_{rms} in the neutral inductor current. Due to the large switching frequency ripples in the inductor current, a large HF ripple current propagates into the midpoint of the split dc bus. This HF current circulates inside the split-capacitor branch.

At the current transient instant, $t=2.187$ (see Figure 5-11), the voltage ripple of the split capacitors is around 10 V, which is half of the desired maximum voltage ripple limit. In addition, the voltage of the midpoint is stabilized with a ripple of 5 V, corresponding to around 0.7% of the total dc bus voltage. Therefore, it can be concluded that the ASCB
configuration keeps the voltage of the midpoint well stabilized under a high neutral current up to 31 A\text{rms} at 50 Hz.

![Figure 5-10. Experimental results of the ASCB configuration under an asymmetric load, which injects a neutral current of 31 A\text{rms} @50 Hz: comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$.
](image)

$V_\text{bus}$ (V)

- 720
- 740
- 760
- 780

- 2.1
- 2.15
- 2.2
- 2.25
- 2.3

(a)

$V_{CN1}$, $V_{CN2}$ (V)

- 360
- 370
- 380
- 400

- 2.1
- 2.15
- 2.2
- 2.25
- 2.3

(b)

$i_N$ (A)

- 100
- 50
- 0
- -50
- -100

- 2.1
- 2.12
- 2.14
- 2.16
- 2.18
- 2.2
- 2.22
- 2.24
- 2.26
- 2.28
- 2.3

(c)

$t=2.187 \text{ s}$

Figure 5-10. Experimental results of the ASCB configuration under an asymmetric load, which injects a neutral current of 31 A\text{rms} @50 Hz: comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$.

Figure 5-11. Experimental results of the ASCB configuration under a load transient, which injects a neutral current of 31 A\text{rms} @50 Hz to the midpoint at 2.187 s. (a) Total dc bus voltage $V_\text{bus}$.

(b) Voltage of the split capacitors $V_{CN1}$ and $V_{CN2}$.

(c) Neutral current $i_N$.

Figure 5-12 to Figure 5-15 present the experimental results of the ACSB configuration under asymmetric loads, corresponding to a neutral current injection of 31 A\text{rms} at 150 Hz and a neutral current injection of 28 A\text{rms} at 250 Hz, respectively. The voltage of the split capacitors in both cases is stabilized with a voltage ripple less than 20 V, which meets the desired midpoint voltage ripple limit. As with the previous experiment test, the maximum neutral current the ASCB can handle is approximately 50% of the neutral current under the worst asymmetric load. In addition, a large HF ripple exits in the charging and discharging current of the split capacitors.
Figure 5-12. Experimental results of the ASCB configuration under an asymmetric load, which injects a neutral current of $31 \text{ A}_{\text{rms}}$ @150 Hz: comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$.

Figure 5-13. Experimental results of the ASCB configuration under a load transient, which injects a neutral current of $31 \text{ A}_{\text{rms}}$ @150 Hz to the midpoint at 2.176 s. (a) Total dc bus voltage $V_{\text{bus}}$. (b) Voltage of the split capacitors $v_{\text{CN1}}$ and $v_{\text{CN2}}$. (c) Neutral current $i_N$.

Figure 5-14. Experimental results of the ASCB configuration under an asymmetric load, which injects a neutral current of $28 \text{ A}_{\text{rms}}$ @250 Hz: comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$. 
Figure 5-15. Experimental results of the ASCB configuration under a load transient, which injects a neutral current of 28 $A_{rms}$ @250 Hz to the midpoint at 1.945 s. (a) Total dc bus voltage $V_{bus}$. (b) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. (c) Neutral current $i_N$.

Table 5-5 summarizes the experimental results of the ASCB configuration under various neutral current injections, ranging from 31 $A_{rms}$ at 50 Hz, 31 $A_{rms}$ at 150 Hz, 28 $A_{rms}$ at 250 Hz, 17 $A_{rms}$ at 350 Hz, 14 $A_{rms}$ at 450 Hz and 14 $A_{rms}$ at 550 Hz. These frequencies of the neutral currents are selected based on the harmonic mitigation requirement of the 3P4W shunt APF, and the RMS values are limited by the maximum current rating of the neutral wire and the desired midpoint voltage ripple.

Table 5-5. Experimental results of the ACSB configuration under various neutral currents.

<table>
<thead>
<tr>
<th>Neutral current $[i_N]$</th>
<th>Neutral inductor current $[i_{LN}]$</th>
<th>Midpoint voltage ripple $[V_{N,pp}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 $A_{rms}$ @50 Hz</td>
<td>33 $A_{rms}$</td>
<td>5 V</td>
</tr>
<tr>
<td>31 $A_{rms}$ @150 Hz</td>
<td>33 $A_{rms}$</td>
<td>12 V</td>
</tr>
<tr>
<td>28 $A_{rms}$ @250 Hz</td>
<td>32 $A_{rms}$</td>
<td>20 V</td>
</tr>
<tr>
<td>17 $A_{rms}$ @350 Hz</td>
<td>23 $A_{rms}$</td>
<td>20 V</td>
</tr>
<tr>
<td>14 $A_{rms}$ @450 Hz</td>
<td>21 $A_{rms}$</td>
<td>20 V</td>
</tr>
<tr>
<td>14 $A_{rms}$ @550 Hz</td>
<td>21 $A_{rms}$</td>
<td>20 V</td>
</tr>
</tbody>
</table>

5.3.2 Proposed MVB

Figure 5-16 and Figure 5-17 show the experimental results of the MVB under the worst asymmetric load condition, and the experimental results under a neutral current transient of 58 $A_{rms}$ at 1.889 s, respectively. These results include the neutral inductor current $i_{LN1}$, $i_{LN2}$, the total inductor current $i_L$, the neutral current $i_N$, the total dc bus voltage $V_{bus}$, and the voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. 
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Figure 5-16. Experimental results of the MVB under the worst asymmetric load condition, in which a neutral current of 58 A_{rms}@50 Hz is injected to the midpoint. (a) Neutral inductor currents $i_{LN1}$, $i_{LN2}$ and total inductor current $i_L$. (b) Comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$.

Because of the interleaving of the dual-switching-leg, the current ripple in the total inductor current is much smaller than of the individual neutral inductor current, as shown in Figure 5-16 (a). The measured neutral current almost overlaps the total inductor current as shown in Figure 5-16 (b). This means that a good neutral current tracking is maintained, so that only a small amount of charging and discharging current is injected into the split capacitors, thus keeping the voltage of the midpoint stabilized.

At the load transient instant, $t=1.889$ s (see Figure 5-17), the voltage ripple of the split capacitors is around 15 V, which is lower than the desired maximum voltage ripple limit. In addition, the voltage of the midpoint is stabilized with a ripple of 10 V, corresponding to around 1.3% of the total dc bus voltage. Therefore, it can be concluded that the MVB
keeps the voltage of the midpoint well stabilized under a high neutral current up to 58 A\textsubscript{rms} at 50 Hz.

Figure 5-18. Experimental results of the MVB under an asymmetric load, which injects a neutral current of 32 A\textsubscript{rms} @150 Hz to the midpoint. (a) Neutral inductor currents $i_{LN1}$, $i_{LN2}$ and total inductor current $i_L$. (b) Comparison of the neutral current $i_N$ and the neutral inductor current $i_{LN}$.

Figure 5-19. Experimental results of the MVB under a load transient, which injects a neutral current of 32 A\textsubscript{rms} @150 Hz to the midpoint at 1.912 s. (a) Total dc bus voltage $V_{bus}$. (b) Voltage of the split capacitors $v_{CN1}$ and $v_{CN2}$. (c) Neutral current $i_N$.

The experimental results of the MVB under asymmetric loads are presented from Figure 5-18 to Figure 5-21, corresponding to a neutral current injection of 32 A\textsubscript{rms} at 150 Hz and a neutral current injection of 24 A\textsubscript{rms} at 250 Hz, respectively. The voltage of the split capacitors in both cases is stabilized with a voltage ripple less than 20 V, which meets the desired midpoint voltage ripple limit. As with the previous experiments, the interleaving of the dual-switching-leg counteracts most of the HF ripple through the total inductor, so that only a small amount of HF ripple current propagates to the midpoint.

Table 5-6 summarizes the experimental results of the MVB under various neutral current injections, ranging from 58 A\textsubscript{rms} at 50 Hz, 32 A\textsubscript{rms} at 150 Hz, 24 A\textsubscript{rms} at 250 Hz, 18 A\textsubscript{rms} at
350 Hz, 17 A_{rms} at 450 Hz and 16 A_{rms} at 550 Hz. These frequencies of the neutral currents are selected based on the harmonic mitigation requirement of the 3P4W shunt APF, and the RMS values are limited by the maximum current rating of the neutral wire and the desired midpoint voltage ripple.

![Figure 5-20](image)

Figure 5-20. Experimental results of the MVB under an asymmetric load, which injects a neutral current of 21 A_{rms} @250 Hz to the midpoint. (a) Neutral inductor currents \(i_{LN1}, i_{LN2}\) and total inductor current \(i_L\). (b) Comparison of the neutral current \(i_N\) and the neutral inductor current \(i_{LN}\).

![Figure 5-21](image)

Figure 5-21. Experimental results of the MVB under a load transient, which injects a neutral current of 21 A_{rms} @250 Hz to the midpoint at 1.696 s. (a) Total dc bus voltage \(V_{bus}\). (b) Voltage of the split capacitors \(v_{CN1}\) and \(v_{CN2}\). (c) Neutral current \(i_N\).

Table 5-6. Experimental results of the MVB under various neutral currents.

<table>
<thead>
<tr>
<th>Neutral current ([i_N])</th>
<th>Neutral inductor current ([i_{LN1}, i_{LN2}])</th>
<th>Midpoint voltage ripple ([V_{N,pp}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>58 A_{rms} @050 Hz</td>
<td>31 A_{rms}</td>
<td>10 V</td>
</tr>
<tr>
<td>32 A_{rms} @150 Hz</td>
<td>19 A_{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>21 A_{rms} @250 Hz</td>
<td>15 A_{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>19 A_{rms} @350 Hz</td>
<td>15 A_{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>17 A_{rms} @450 Hz</td>
<td>14 A_{rms}</td>
<td>20 V</td>
</tr>
<tr>
<td>16 A_{rms} @550 Hz</td>
<td>14 A_{rms}</td>
<td>20 V</td>
</tr>
</tbody>
</table>
5.4 Conclusion

In this chapter, the proposed MVB has been proven to be effective regarding the dc bus midpoint voltage stabilization under various neutral current conditions. The experimental results from Figure 5-17 verify that the voltage ripple of the split capacitors is maintained around 1.3% of the total dc bus voltage even under the worst asymmetric load condition, in which a neutral current of 58 A\text{rms} at 50Hz is injected into the midpoint.

Compared to the ASCB configuration, the MVB demonstrates advantages in terms of the doubled neutral current handling capacity at 50 Hz and less HF current circulation through the split-capacitor branch. In addition, the IGBT switches of the MVB operate at ZVS condition under a wider operation range, of which the neutral current is less than 29 A\text{rms}. As a comparison, the IGBT switches of the ASCB configuration only operates under ZVS when the neutral current is less than 14.5 A\text{rms}.

However, the handling capacity of the neutral current of the MVB is compromised at the multiples of the fundamental frequency. As listed in Table 5-5 and Table 5-6, the maximum neutral current of the MVB, whose midpoint voltage ripple is desired to be less than 20 V, is close to that of the ASCB configuration at harmonic current orders of 7\textsuperscript{th}, 9\textsuperscript{th} and 11\textsuperscript{th}. It is mainly because the total inductor current cannot keep up with the neutral currents that are multiples of the fundamental frequency. This mismatch between the total inductor current and the neutral current introduces low-frequency ripple to the charging and discharging current of the split capacitors, leading to an excessive voltage ripple at the midpoint.

Nevertheless, neutral current predominantly consists of fundamental frequency in EPDNs, where harmonic contents are only a fraction of the fundament current. Therefore, it can be concluded that the proposed MVB stabilizes the midpoint with a voltage ripple being less than 20 V under various asymmetric load conditions.
The main conclusions of this thesis regarding design choice selection, passive components design, dual-loop control, and the verification are given. In addition, recommendations for future work are also presented, including optimization of neutral inductors, experimental test, as well as the control loop bandwidth broadening, and the continuation of the project CONNECT.

6. CONCLUSIONS AND RECOMMENDATIONS

Conclusions

Recommendations for future work
6.1 Conclusions

This PDEng project focuses on the midpoint voltage balancer (MVB), which is based on a dual-switching-leg configuration, to divert the energy of the split capacitors so that the voltage of the dc bus midpoint is stabilized. The main goal of this project is the prototyping of an operational MVB that secures the neutral point voltage of the 20 kVA shunt APF for the ECSEL JU funded project CONNECT. In addition, the proposed MVB also has a great potential in bipolar dc micro grid applications [68].

This thesis provides design choice selection, passive components design and dimensioning, modeling, control design, and verification of the MVB. The main conclusions of the thesis are summarized in the following.

1) Design choice selections of the neutral point configuration

The proposed MVB was selected as a promising design choice for prototyping, because of the overall advantages regarding the ease of development, EMC immunity, lifespan, cost of solution, midpoint voltage stabilization performance, and dc component handling capability. Compared to the ACSB configuration, the neutral current handling capacity of the MVB is doubled, and the HF current propagation into the midpoint is reduced significantly. In addition, the MVB operates under ZVS under a wider range of load asymmetry.

2) Passive components design

The design and dimensioning of the neutral inductors and split capacitors of the MVB is presented. The inductance of the neutral inductors is set to 220 µH to allow ZVS operation of the IGBT switches in the MVB under a wider operation range. The capacitance of the split capacitors is designed as 100 µF based on the desired range of LC resonant frequency.

3) Dual-loop control of the MVB

To control the MVB in a desired manner, a discrete-time model, which properly considers the effects of digital signal acquisition and the PWM delay, is developed. A dual-loop control scheme consisting of an inner current loop and an outer voltage loop is adopted. The inner current loop, whose crossover frequency is 2 kHz, responds fast to given input. The outer voltage loop, whose crossover frequency is 0.2 kHz corrects any regulation error of the current loop. In addition, an active damping strategy is implemented in the control
loop to deal with the $LC$ resonance by creating $1.5 \, \Omega$ virtual series resistance to the neutral inductors.

4) Verification

Experimental tests verified the effectiveness of the proposed MVB. The voltage ripple of the split capacitors of the MVB is maintained around 1.3% of $V_{bus}$ even under the worst asymmetric load condition, in which a neutral current of 58 A$_{rms}$ at 50Hz is injected into the midpoint. The MVB also provides a stable midpoint, of which the voltage ripple is less than around 2.6% of $V_{bus}$, even though the neutral current has multiples of fundamental frequency (3$^{rd}$, 5$^{th}$, 7$^{th}$, 9$^{th}$ and 11$^{th}$).

6.2 Recommendations for future work

The voltage stabilization of the dc bus midpoint of the proposed MVB under various neutral current conditions has been verified through experimental tests. However, further improvements are possible as suggested in the following.

1) Inductance optimization

The inductance of the neutral inductors is designed to be 220 $\mu$H. Such a small inductance value was chosen on purpose in order to allow a high current ripple through the neutral inductors, so that the IGBT switches of the MVB fully operates on ZVS condition when the neutral current is less than 29 A$_{rms}$. Even though the ZVS theoretically eliminates the turn-on losses of the IGBT switches and the reverse recovery loss of the anti-paralleled diode, the inductor peak current during turn-off moments is increased, which introduces extra turn-off losses of the IGBT switches. Therefore, it would be beneficial to investigate an approach to derive an optimized inductance value, which also contributes to an overall switching loss reduction under wide load asymmetry conditions.

2) Control loop bandwidth broadening

The crossover frequency of the current loop is 2 kHz, and the crossover frequency of the voltage loop is 200 Hz. It is advantageous to have a higher bandwidth of the current loop, so that the total inductor current can track the neutral current without much delay even under 11$^{th}$ of the fundamental frequency. However, the bandwidth of the current loop is limited by the sampling frequency and the computation speed of the digital control platform, and it also related to the switching frequency. Nevertheless, it would be an
interesting point to test the MVB with a high-bandwidth current loop, which can be obtained by implementing the whole control model into the FPGA domain of the dSPACE platform.

3) Experimental test optimization

The maximum neutral current the MVB can handle while maintaining a less-than-20 V ripple in the experiment test is much less than that in the simulation at 150 Hz and 250 Hz, as shown in Figure 6-2. This means that the experimental results could be improved, considering the control design is already verified by simulations. Since the mismatch between the simulation results and the experimental results could be brought by the implementation delays, it would be beneficial to increasing the bandwidth of signal acquisition, implementing the control model into the FPGA domain.

4) Continuation of the project

The prototyping of the MVB is a part of the research project “design and implementation of a 20 kVA bidirectional 3P4W grid-interfacing dc-ac power converter”. Its verification success is a step forward towards the completion of the CONNECT project. The next step is the implementation of an advanced control strategy for voltage quality enhancement of a local PCC without load current measurements.
## A. List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-C</td>
<td>Conventional split capacitors</td>
</tr>
<tr>
<td>3P4W</td>
<td>Three-phase four-wire</td>
</tr>
<tr>
<td>4-Leg</td>
<td>Four-leg converter</td>
</tr>
<tr>
<td>ac</td>
<td>Alternating current</td>
</tr>
<tr>
<td>ACSB</td>
<td>Actively controlled split dc bus</td>
</tr>
<tr>
<td>APF</td>
<td>Active power filter</td>
</tr>
<tr>
<td>dc</td>
<td>Direct current</td>
</tr>
<tr>
<td>DEES-ICT</td>
<td>Design of Electrical Engineering Systems-Information and Communication Technology</td>
</tr>
<tr>
<td>DPG</td>
<td>Distributed power generation</td>
</tr>
<tr>
<td>DSO</td>
<td>Distribution system operator</td>
</tr>
<tr>
<td>ECSEL JU</td>
<td>Electronic Components and Systems for European Leadership Joint Undertaking</td>
</tr>
<tr>
<td>EES</td>
<td>Electrical Energy System</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic compatibility</td>
</tr>
<tr>
<td>EN</td>
<td>European standards</td>
</tr>
<tr>
<td>EPDN</td>
<td>Electric power distribution network</td>
</tr>
<tr>
<td>EPE</td>
<td>Electromechanics and Power Electronic</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent series resistance</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field programmable gate array</td>
</tr>
<tr>
<td>HF</td>
<td>High frequency</td>
</tr>
<tr>
<td>IEC</td>
<td>International Electrotechnical Commission</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronic Engineers</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IUF</td>
<td>Current unbalance factor</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff's circuit law</td>
</tr>
<tr>
<td>LC</td>
<td>Inductor and capacitor</td>
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<tr>
<td>MVB</td>
<td>Midpoint voltage balancer</td>
</tr>
<tr>
<td>PBM</td>
<td>Project based management</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of common coupling</td>
</tr>
<tr>
<td>PDEng</td>
<td>Professional doctorate in engineering</td>
</tr>
<tr>
<td>PEIT</td>
<td>Power electronics innovation team</td>
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<tr>
<td>PWM</td>
<td>Pulse-width modulation</td>
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### List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS</td>
<td>Root mean square</td>
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<tr>
<td>SHU</td>
<td>Shanghai University</td>
</tr>
<tr>
<td>TU/e</td>
<td>Eindhoven University of Technology</td>
</tr>
<tr>
<td>VUF</td>
<td>Voltage unbalance factor</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero voltage switching</td>
</tr>
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</table>
B. CONNECT consortium

Table B-1 lists all the 19 participants of the CONNECT consortium, which are from five European countries: Germany, Slovakia, the Netherlands, Spain, and Italy.

Table B-1 Participating organizations of the CONNECT consortium

<table>
<thead>
<tr>
<th>Country</th>
<th>Organization</th>
</tr>
</thead>
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<tr>
<td>Germany</td>
<td>Infineon Technology AG</td>
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<td>NXP Semiconductors Germany GmbH</td>
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<td>Friedrich Alexander Universität Erlangen</td>
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<td></td>
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<td>Slovenska Technicka Univerzita Bratislave</td>
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<td>The Netherlands</td>
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<td>ENEL spa</td>
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<td></td>
<td>Consorzio Nazionale Interuniversitario per la Nanoelettronica</td>
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<tr>
<td></td>
<td>Politecnico de Bari</td>
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Figure B-1. Participants of the CONNECT program.
Appendix C

C. Detailed Requirements and Specifications of the 20 kVA 3P4W shunt APF

Table C-1 lists the requirements of the 20 kVA 3P4W shunt APF under development, which includes the requirements from several perspectives: dc side, ac side, dc bus midpoint, voltage quality enhancement, and safety. The detailed specifications of the shunt APF are given in Table C-2.

Table C-1. Requirements of the 20 kVA 3P4W shunt APF.

<table>
<thead>
<tr>
<th>DC side requirements</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus voltage</td>
<td>720</td>
<td>760</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>DC current</td>
<td>/</td>
<td>26</td>
<td>33</td>
<td>A</td>
</tr>
<tr>
<td>DC power</td>
<td>/</td>
<td>20</td>
<td>23</td>
<td>kW</td>
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<table>
<thead>
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<th>Max.</th>
<th>Unit</th>
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<td>Voltage frequency</td>
<td>49.5</td>
<td>50</td>
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<td>Phase-to-phase voltage</td>
<td>360</td>
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<td>440</td>
<td>Vrms</td>
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<tr>
<td>Phase-to-neutral voltage</td>
<td>210</td>
<td>230</td>
<td>250</td>
<td>Vrms</td>
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<tr>
<td>Line current</td>
<td>/</td>
<td>29</td>
<td>33</td>
<td>Arms</td>
</tr>
<tr>
<td>Apparent power</td>
<td>/</td>
<td>20</td>
<td>/</td>
<td>kVA</td>
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<table>
<thead>
<tr>
<th>DC bus midpoint/neutral point requirements</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
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<td>Neutral wire current</td>
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<td>/</td>
<td>58</td>
<td>Arms</td>
</tr>
<tr>
<td>Midpoint voltage ripple</td>
<td>/</td>
<td>/</td>
<td>80</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage quality enhancement requirement</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Three-phase voltage unbalance factor</td>
<td>/</td>
<td>/</td>
<td>2</td>
<td>%</td>
</tr>
<tr>
<td>Total voltage harmonic distortion at PCC</td>
<td>/</td>
<td>/</td>
<td>8</td>
<td>%</td>
</tr>
<tr>
<td>Harmonic order under mitigation</td>
<td>/</td>
<td>/</td>
<td>11</td>
<td>/</td>
</tr>
<tr>
<td>Power factor at PCC(^2)</td>
<td>0.95</td>
<td>1</td>
<td>1.05</td>
<td>/</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Safety related requirements</th>
<th>Min.</th>
<th>Nom.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage during dis(connecting)</td>
<td>/</td>
<td>/</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Current during connecting</td>
<td>/</td>
<td>/</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td>Current during disconnecting</td>
<td>/</td>
<td>/</td>
<td>1</td>
<td>A</td>
</tr>
</tbody>
</table>

\(^2\) The power factor correction depends on the existence of a central energy management system that sends the reactive power command to the 20 kVA 3P4W shunt APF.
Table C-2. Specifications of the 20 kVA SP4W shunt APF.

<table>
<thead>
<tr>
<th>Three-phase voltage source inverter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>20 kHz</td>
<td></td>
</tr>
<tr>
<td>Modulation frequency</td>
<td>50 Hz</td>
<td></td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>20 kHz</td>
<td></td>
</tr>
<tr>
<td>Number of IGBT switches</td>
<td>6 /</td>
<td></td>
</tr>
<tr>
<td>IGBT dead time</td>
<td>2 µs</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown voltage</td>
<td>1200 V</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown current @ 25°C</td>
<td>80 A&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown current @ 70°C</td>
<td>70 A&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Midpoint voltage balancer</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>20 kHz</td>
<td></td>
</tr>
<tr>
<td>Modulation frequency</td>
<td>50 Hz</td>
<td></td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>20 kHz</td>
<td></td>
</tr>
<tr>
<td>Number of IGBT switches</td>
<td>4 /</td>
<td></td>
</tr>
<tr>
<td>IGBT dead time</td>
<td>2 µs</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown voltage</td>
<td>1200 V</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown current @ 25°C</td>
<td>80 A&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>IGBT &amp; diode breakdown current @ 70°C</td>
<td>70 A&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>Neutral current tracking crossover frequency</td>
<td>2 kHz</td>
<td></td>
</tr>
<tr>
<td>Voltage balancing crossover frequency</td>
<td>0.2 kHz</td>
<td></td>
</tr>
<tr>
<td>Capacitance of DC bus capacitors</td>
<td>2450 µF</td>
<td></td>
</tr>
<tr>
<td>Capacitance of dc bus split capacitors</td>
<td>100 µF</td>
<td></td>
</tr>
<tr>
<td>Capacitor equivalent series resistance</td>
<td>0.8 mΩ</td>
<td></td>
</tr>
<tr>
<td>Inductance of neutral inductors</td>
<td>220 µH</td>
<td></td>
</tr>
<tr>
<td>Series resistance of neutral inductors</td>
<td>73 mΩ</td>
<td></td>
</tr>
<tr>
<td>Maximum neutral current for ZVS</td>
<td>28 A&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Digital control</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage and current sampling time</td>
<td>50 µs</td>
<td></td>
</tr>
<tr>
<td>PWM delay</td>
<td>25 µs</td>
<td></td>
</tr>
<tr>
<td>Computation delay</td>
<td>20 µs</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Over-current and over-voltage protection of the MVB</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage protection limit of the split dc bus</td>
<td>420 V</td>
<td></td>
</tr>
<tr>
<td>Current protection limit of the neutral inductor</td>
<td>60 A</td>
<td></td>
</tr>
<tr>
<td>Current protection limit of the neutral wire</td>
<td>100 A</td>
<td></td>
</tr>
</tbody>
</table>
Appendix D

D. Project based management: decision document

Introduction
Scope
Design strategy
Work phase plan
Management
Revision history

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.0</td>
<td>09-10-2017</td>
<td>Initial version.</td>
</tr>
<tr>
<td>V1.1</td>
<td>13-10-2017</td>
<td>Major revision based on the first project based management meeting with Poul Bakker.</td>
</tr>
<tr>
<td>V2.0</td>
<td>22-02-2018</td>
<td>Detailed project plan and project deliverables in each work phase were added.</td>
</tr>
<tr>
<td>V2.1</td>
<td>27-10-2018</td>
<td>Major revision based on the second project based management meeting with Poul Bakker.</td>
</tr>
<tr>
<td>V3.0</td>
<td>25-08-2019</td>
<td>Final version</td>
</tr>
</tbody>
</table>

Current status of the project

The two-year PDEng project, *midpoint voltage stabilization and its hardware implementation for a 20 kVA three-phase four-wire (3P4W) shunt active power filter (APF)*, has been successfully completed. The designed midpoint voltage balancer (MVB) has been verified through experimental tests, and its voltage regulation performance meets the requirement under various neutral current injections.
D.1 Introduction

D.1.1 ECSEL JU

The ECSEL JU (Electronics Components and Systems for European Leadership Joint Undertaking) is a public-private partnership in the area of electronics components and systems. ECSEL JU funds research, development, and innovation projects for world-class expertise in key enabling technologies, which are essential for Europe’s competitive leadership in the era of the digital economy. Through the ECSEL JU, the European industry, SMEs, research and technology organizations are supported and co-financed by 30 ECSEL participating states and the European Union.

D.1.2 CONNECT

Project CONNET, funded by ECSEL JU, was proposed in 2017 to deal with peak power demand in electric power distribution networks (EPDNs). More information regarding peak power demand and its consequences in EPDNs can be found in section 1.2.1. CONNECT aims to research, design, develop, and showcase novel solutions for efficient devices and components of the future smart grid, with the key objective of reducing the peak power demand by at least a factor of two.

CONNECT is coordinated by Infineon Technologies AG, and it has the duration of 3 years. It involves 19 participants in 5 European countries (detailed participants list can be found in Appendix A). CONNECT receives total funding of 19.9 million Euros from ECSEL JU research and innovation action program, as well as governments of participating countries.

The technical work of CONNECT is distributed into five work packages (WPs). As shown in Figure D-1, it starts from WP1 the definition of the technical requirements, specifications, and interfaces for the subsequent research effort, to WP5 the design and implementation of communication infrastructure components. The integration of sub-systems, proof of concepts and validation against the objectives are addressed in the last stage, in which four use-cases (UCs) will be carried out, shown as follows:

- UC1. Controllable energy flow.
- UC2. Demand control for supply with high amount of distributed energy resources.

---

4 ECSEL JU participating states are Austria, Belgium, Bulgaria, Czech Republic, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Italy, Lithuania, Latvia, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey, United Kingdom and Switzerland.
UC3. Local dc micro-grid as a smart local power domain.

UC4. Secure, robust, high bandwidth communication for innovative management.

As one of the participants, TU/e contributes to WP1, WP2, and the demonstration of UC1. The global specifications of a 20 kVA 3P4W shunt APF is given in WP1, while the prototyping of the shunt APF will be carried out in WP2.

UC1 will be demonstrated in a transferium in Den Bosch in cooperation with three Dutch companies, ENEXIS BV, Heliox BV, and GreenFlux Assets BV. This UC integrates the optimized power conversion topologies from TU/e, advanced EV charging management from GreenFlux, and battery charging converters from Heliox. In addition, UC1 will be supported and facilitated by ENEXIS in terms of grid interfacing. UC1 will be applied to a local sub-grid. It will demonstrate that the power factor can be kept at unity, the voltage quality can be improved, and the EV charging profiles can be managed, so that a stable power flow into the sub-grid can be realized.

D.1.3 PDENG project

A two-year PDEng project, midpoint voltage stabilization and its hardware implementation for a 20 kVA 3P4W shunt APF is derived from WP2 of the CONNET project. The final deliverable of the PDEng project is an operational midpoint voltage balancer that stabilizes the neutral point of a 20 kVA 3P4W shunt APF under various load asymmetry conditions.

This PDEng project is fully conducted at the TU/e, within the Electromechanics and Power Electronics (EPE) group, Department of Electrical Engineering. The PDEng candidate of this project is supervised by dr. J. L. Duarte, assistant professor at the EPE group.
D.2 Scope

D.2.1 Problem definition

Voltage imbalance poses adverse effects on EPDNs and the connected electrical equipment. It leads to derating of distribution transformers, increased power loss in neutral wires. Moreover, it causes derating, reduced efficiency, and decreased life-time of induction motors that are directly coupled to the grid. In addition, it results in undesirable low-frequency harmonic components on the dc bus voltage of motor drives, which raises the temperature of the dc bus capacitors, thus degrading their predicted lifetimes.

Shunt APF can be employed to deal with voltage imbalance issues in an EPDN by injecting or sinking reversed unbalanced current to or from the point of common coupling. In EPDNs, since 3P4W is the most common configuration for residential and industrial users. Therefore, the shunt AFP that meant for voltage imbalance compensation must provide a neutral point, to which the zero-sequential current flows.

Existing configurations of neutral point creation in 3P4W shunt APF are the 2-C configuration, the 4-Leg configuration, and the ACSB configuration (see in chapter 2). The 2-C configuration suffers from the voltage mismatching across two split capacitors, and the incapability of dc current component compensation. The 4-Leg configuration associates with high development effort and common mode current in neutral wire. The ACSB configuration combines the essence of the 2-C configuration and the 4-Leg configuration. However, the ACSB configuration can only compensate the neutral current up to the maximum phase current, which is only half of the maximum neutral current during the worst load asymmetry. In addition, the associated high frequency current circulation in the split capacitors could cause overheating to the split capacitors.

D.2.2 Deliverable

Prototype

A midpoint voltage balancer (MVB) that stabilizes the voltage of the neutral point of a 20 kVA 3P4W shunt APF. Main features and advantages of the MVB are listed as follows:

<table>
<thead>
<tr>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-switching-leg configuration.</td>
</tr>
<tr>
<td>Switching frequency of 20 kHz.</td>
</tr>
<tr>
<td>Sampling frequency of 20 kHz.</td>
</tr>
<tr>
<td>Dual-loop control.</td>
</tr>
<tr>
<td>Active damping.</td>
</tr>
</tbody>
</table>
Appendix D  Project based management: decision document

**Feature**
- Fast voltage regulation response, less than a grid cycle.
- Stabilization of midpoint voltage within 20 V under various neutral current injections.

**Advantage**
- Neutral current compensation capacity up to 58 Arms.
- Interleaving of the dual-switching-leg.
- Zero voltage switching.

**Documentation**

**PDEng thesis**
- Midpoint Voltage Stabilization of Split DC Bus in Three-Phase Four-Wire Shunt Active Power Filters: Prototyping of a Midpoint Voltage Balancer for the ECSEL JU Funded Project CONNECT

**Paper**
- X. Xu, G. Tibola, J. Duarte, and F. Wang, Fast Voltage Stabilization Control of Split DC Bus Midpoint in 3P4W Shunt APFs, 21st European Conference on Power Electronics and Applications, Genova, 2019

**Deliverable to CONNECT**
- Technical report on the definition of the UC1.
- Technical report on the detailed requirements of the 20 kVA 3P4W shunt APF.
- Year reports (1st year, 2nd year, and 3rd year).
- Technical review documents.

**D.2.3 Delimitation**

1. LCL filter design of the 20 kVA 3P4W shunt APF.
2. Hardware prototyping of grid interfacing of the 20 kVA 3P4W shunt APF.
3. Advanced control strategy for voltage quality enhancement without the load current measurements.
4. Control strategy implementation in the 20 kVA 3P4W shunt APF.

**D.2.4 Results achieved**

1. The midpoint voltage ripple of the 3P4W shunt APF is maintained around 1.3% of the total dc bus voltage under a neutral current injection of 58 A_{rms} at 50 Hz.
2. The neutral current handling capacity of the MVB is doubled compared to that of the ASCB configuration.
3. The propagation of high frequency ripple current to the midpoint of the split capacitors is reduced by around 84%, due to the interleaving of the dual-switching-leg.
4. All IGBT switches of the MVB operates under ZVS, when the neutral current is smaller than then nominal phase current (29 A_{rms}).

**D.3 Design strategy**

1. Brainstorm of possible neutral point configurations for a 3P4W shunt APF.

![Brainstorm of possible neutral point configurations](image)

Figure D-2. Brainstorm of possible neutral point configurations.

2. Literature investigation.

3. Theoretical calculation, assumptions, derivation and mathematical modeling.

4. MATLAB simulations.

5. Hardware implementation.

6. Experimental tests.

**D.4 Work phase plan**

**D.4.1 Definition phase**

Time duration: from 15-08-2017 to 30-11-2017

<table>
<thead>
<tr>
<th>Task</th>
<th>Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>Understand the project in different aspects.</td>
<td>Project kick-off meeting.</td>
</tr>
<tr>
<td>Define the scope of the project.</td>
<td>Meeting with daily supervisor once a week.</td>
</tr>
<tr>
<td>Get to know the requirements of the 20 kVA 3P4W shunt APF.</td>
<td>Meet with the chair of the EPE group, discuss project scope, plan, deliverables, and cooperation between partners.</td>
</tr>
<tr>
<td>Make a sound project plan.</td>
<td></td>
</tr>
</tbody>
</table>
### Deliverable
- Task allocation within the team.
- A project execution plan.

### D.4.2 Preparation phase

**Time duration:** from 01-12-2017 to 30-04-2018

<table>
<thead>
<tr>
<th>Task</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Investigation on the existing neutral point configurations and their control strategies.</td>
</tr>
<tr>
<td>• Improvements on the selected configuration.</td>
</tr>
<tr>
<td>• Verification on the improved configuration (MVB) through MATLAB simulation.</td>
</tr>
<tr>
<td>• Get to know the Tri-phase quad-converter platform in the lab.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Meeting with daily supervisor once a week.</td>
</tr>
<tr>
<td>• Meeting with the chair of the EPE group at the end of the preparation phase.</td>
</tr>
<tr>
<td>• The 2nd CONNECT general gathering meeting in Bratislava on 21-03-2018.</td>
</tr>
<tr>
<td>• Preparation PDEng project evaluation (go/no-go) on 16-03-1018.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Deliverable</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Comparison study on different neutral point configurations.</td>
</tr>
<tr>
<td>• Suitable control strategy of the MVB.</td>
</tr>
<tr>
<td>• MATLAB simulation of 3P4W converter with actively controlled split dc bus and with the MVB will be carried out both in stand-alone and grid-connected to validate the circuit topology and its control strategy.</td>
</tr>
</tbody>
</table>

### D.4.3 Design and simulation verification phase

**Time duration:** from 01-02-2018 to 31-01-2019

<table>
<thead>
<tr>
<th>Task</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Theoretical calculation on hardware parameters, neutral inductances, split capacitances, current and voltage stress across all the switches, etc.</td>
</tr>
<tr>
<td>• Controllers design, including mathematical modeling, transfer function derivation, and stability analysis.</td>
</tr>
<tr>
<td>• Computer simulation on the designed controllers.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Communication</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Meeting with daily supervisor once a week.</td>
</tr>
<tr>
<td>• Meeting with the chair of the EPE group at the end of this phase.</td>
</tr>
<tr>
<td>• The 3rd CONNECT general gathering meeting in Amsterdam on 08-10-2018.</td>
</tr>
<tr>
<td>• Midterm PDEng project evaluation on 08-11-2018.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Deliverable</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Analytical model of a 3P4W shunt APF with active controlled split dc bus.</td>
</tr>
<tr>
<td>• Analytical model of a 3P4W shunt APF with MVB.</td>
</tr>
<tr>
<td>• Control loop design, current and voltage controllers.</td>
</tr>
<tr>
<td>• Simulation verification of the designed control loop.</td>
</tr>
</tbody>
</table>
D.4.4 Implementation phase

Time duration: from 01-03-2018 to 30-06-2019

<table>
<thead>
<tr>
<th>Task</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Hardware implementation of</td>
<td></td>
</tr>
<tr>
<td>the MVB.</td>
<td></td>
</tr>
<tr>
<td>• Component selection.</td>
<td></td>
</tr>
<tr>
<td>• PCB design and soldering.</td>
<td></td>
</tr>
<tr>
<td>• Dimensioning of neutral</td>
<td></td>
</tr>
<tr>
<td>inductors.</td>
<td></td>
</tr>
<tr>
<td>• Digital signal acquisition.</td>
<td></td>
</tr>
<tr>
<td>• Digital control realization</td>
<td></td>
</tr>
<tr>
<td>on dSPACE MicroLabBox.</td>
<td></td>
</tr>
<tr>
<td>• Experimental verification.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Communication</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Meeting with daily supervisor once a week.</td>
<td></td>
</tr>
<tr>
<td>• Meeting with the chair of EPE group at the end of this phase.</td>
<td></td>
</tr>
<tr>
<td>• The 4th CONNECT general gathering meeting in Hamburg on 26-03-2019.</td>
<td></td>
</tr>
<tr>
<td>• Prefinal PDEng project evaluation on 09-05-2019</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Deliverable</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• An operational prototype of</td>
<td></td>
</tr>
<tr>
<td>the 3P4W converter with the</td>
<td></td>
</tr>
<tr>
<td>MVB which stabilizes the</td>
<td></td>
</tr>
<tr>
<td>voltage of the neutral</td>
<td></td>
</tr>
<tr>
<td>point with a ripple smaller</td>
<td></td>
</tr>
<tr>
<td>than 80 V.</td>
<td></td>
</tr>
</tbody>
</table>

D.4.5 Finalization phase

Time duration: from 01-07-2019 to 29-08-2019

<table>
<thead>
<tr>
<th>Task</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Documentation of the whole</td>
<td></td>
</tr>
<tr>
<td>project.</td>
<td></td>
</tr>
<tr>
<td>• Final defense preparation.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Communication</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• Meeting with daily supervisor once a week.</td>
<td></td>
</tr>
<tr>
<td>• Meeting with the chair of EPE group at the end of this phase.</td>
<td></td>
</tr>
<tr>
<td>• Final PDEng project evaluation (final defense) on 29-08-2019.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Deliverable</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>• PDEng thesis and final evaluation presentation.</td>
<td></td>
</tr>
</tbody>
</table>

D.5 Management

D.5.1 Time

Staring date of the PDEng project: 15-08-2017.
End date of the PDEng project: 29-08-2019 with 2 weeks prolongation.

Duration of work phases

5 If promising results can be obtained, then it comes to the end of this work phase. If not, start again from the design phase.
6 Work phases in this project are not always consecutive, some of which run in parallel.
Table D-1. Duration of work phases.

<table>
<thead>
<tr>
<th>Work phase</th>
<th>Duration (month)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Definition phase</td>
<td>3.5</td>
</tr>
<tr>
<td>Preparation phase</td>
<td>5</td>
</tr>
<tr>
<td>Design and simulation verification phase</td>
<td>12</td>
</tr>
<tr>
<td>Implementation phase</td>
<td>16</td>
</tr>
<tr>
<td>Finalization phase</td>
<td>2</td>
</tr>
</tbody>
</table>

**Process control**

1. Technical and progress update discussion with the scientific supervisor once a week.
2. Administrative and progress update discussion with the chair of the EPE group at the end of each work phase.
3. General gathering meeting with all participating partner in the CONNECT project once per six months, with the next one coming in Barcelona on 22-10-2019.
4. Evaluation meeting with all evaluation committee members once per six months, which was schedule on 16-03-2018, 08-11-2018, and 09-05-2019.
5. Final defense meeting with the thesis commit members on 29-08-2019.

**D.5.2 Money**

The funding for the TU/e concerning the CONNECT project as provided by the EU is 214 k€, while the funding received from the Dutch government is unknow to the PDEng trainee. Since the PDEng project is a part of the CONNECT project, it shares the funding.

**D.5.3 Quality**

The developed MVB maintains the voltage variation of the midpoint of a 3P4W shunt APF within 20 V under various neutral current injections. In addition, the response time of the midpoint voltage regulation is within one grid cycle.

**D.5.4 Stakeholder analysis**

**List of stakeholders**

1. Jorge Duarte, scientific supervisor, provides supervision and guidance throughout the course of the project.
2. Elena Lomonova, chair of the EPE group, manages the project in a high level.
3. Korneel Wijnands, professor in the EPE group, member of my PDEng evaluation committee.
4. Peter Smulders, coordinator of the DEES-ICT PDEng program, member of my PDEng evaluation committee.
5. Rian van Gaalen, administrator of the DEES-ICT PDEng program, organizes workshops, courses, summer school, and deal with all sorts of issues from PDEng trainees.
6. Gabriel Tibola, postdoc, offers help during the prototyping of the power converter, especially hardware-wise.
7. Ya Zhang, PhD candidate, provides innovative voltage enhancement control strategy for the 20 kVA grid interfacing shunt APF.
8. Marijn de Willigen and Rutger van Veen, experienced lab technicians, offers help during the prototyping of the power converter.
9. Poul Nakker, project based management coach, help PDEng trainees to conduct their project in a project based manner.

Management

1. For stakeholders with high power and high interest toward the project, fully engage and make the greatest efforts to satisfy.
2. For stakeholders with high power and less interest toward the project, put enough work to keep them satisfied, but not so much that they might become bored.
3. For stakeholders with low power and high interest, keep them informed and talk to them regularly so that no major issues would arise.
4. For stakeholders with low power and low interest, monitor them, but do not bore them with excessive information.

D.5.5 Risk analysis

Risk list

Table D-2. Risk list of the PDEng project.

<table>
<thead>
<tr>
<th>Risk</th>
<th>Effect*</th>
<th>Probability*</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unable to establish communication between Tri-phase quad-converter system and PC</td>
<td>7</td>
<td>5</td>
<td>35</td>
</tr>
<tr>
<td>IGBTs damage because of over-current or over-voltage</td>
<td>8</td>
<td>2</td>
<td>16</td>
</tr>
<tr>
<td>Project delay because of components ordering</td>
<td>7</td>
<td>7</td>
<td>49</td>
</tr>
<tr>
<td>Power rating of the prototype is lower than 20 kVA</td>
<td>8</td>
<td>4</td>
<td>32</td>
</tr>
</tbody>
</table>

* Effect (severity): 1 means low, 5 means medium, 10 means high
* Probability (chance of occurrence): 1 means rare, 5 means moderate, 10 means certain

Equation Priority = Effect*Probability provides a priority list of risks, where higher the result is, where more attention is needed to be paid.

Risk management

Table D-3. Risk management of the PDEng project.

<table>
<thead>
<tr>
<th>Risk</th>
<th>Mitigations plan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unable to establish communication between Tri-phase quad-converter system and PC</td>
<td>Accept</td>
</tr>
<tr>
<td>IGBTs damage because of over-current or over-voltage</td>
<td>Make sure hardware and software over-voltage and over-current protections work properly before doing any tests on the prototype.</td>
</tr>
<tr>
<td>Risk</td>
<td>Mitigations plan</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>---------------------------------------------------------</td>
</tr>
<tr>
<td>Project delay because of components ordering</td>
<td>Carry out the hardware parameters design as soon as possible</td>
</tr>
<tr>
<td>Power rating of the prototype is lower than 20 kVA</td>
<td>Using an extra switch leg for midpoint voltage stabilization.</td>
</tr>
</tbody>
</table>

The Tri-phase quad-converter system was initially selected for the prototyping of the 3P4W shunt APF. However, this plan failed due to the communication problems between the real-time target of the Tri-phase quad converter system and PC, and its compatibility issue with the MATLAB/Simulink. Moreover, the maximum voltage level of the Tri-phase system is not sufficient for the prototyping of the 20 kVA 3P4W shunt APF. Therefore, a SEMIKRON power stack with high-power rating was selected as an alternative for further development. In addition, a dSPACE MicroLabBox was chosen for digital control implementation.

If the combination of the SEMIKRON power stack and the MicroLabBox has been selected in the beginning of the project, the project would have been finished two to three months earlier. In conclusion, even though most project risks can be predicted in the beginning, and corresponding mitigations can be planned, risk could happen, deal with it, and carry on.

**D.5.6 Gannt Chart**

Figure D-3 A general Gannt chart of the project with timing of evaluation meetings


[67] P. CODE and C. PRIX, "Electromagnetic compatibility (EMC)–Part 3-7: Limits–Assessment of emission limits for the connection of fluctuating installations to MV, HV and EHV power systems."