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A -81.6dBm Sensitivity Ultrasound Transceiver in 65nm CMOS for Symmetrical Data-Links

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Abstract—This paper presents the design and experimental characterization of an ultrasound transceiver. The transceiver includes an on-chip transmitter and a receiver to be used in a symmetric data-link, where each sensor node has limited energy resources and is operated in air or a fluidic environment. The receiver and the transmitter operate from a 0.8V supply and consume 1.18µW and 50µW, respectively, while exchanging data at 1kbps data-rate. The receiver sensitivity is -81.6dBm at a \(10^{-3}\) Bit Error Rate (BER) level, which enables an experimentally verified transmission over 3.2m in air and a predicted transmission distance in water in the order of 2km, with a measured energy per bit performance of 51.18 nJ/b.

I. INTRODUCTION

Using ultrasound (US) has become popular in emerging communication applications where ultra low-power operation is desired. The relatively low operating frequency range compared to RF makes US a promising approach for ultra low-power systems. Prior-art [1]–[3] uses US in asymmetric data-links, where data exchange between sensors is performed from a resource-rich external master node to resource-limited slave nodes. The slave nodes are based on an always-on US receiver which is used to save energy during a long-operation time and to activate the main RF radio when high bitrate communication is desired. In this paper, we propose a symmetric US communication link to be used in a network of identical sensor nodes having a limited energy budget and immersed in a fluidic environment. US communication is attractive in this case for its favorable attenuation characteristics compared to RF waves [4]. The proposed sensor network can be deployed for energy-constrained, low bit-rate applications including environmental monitoring, detection of defects in pipelines and water distribution networks. In this work, the design of an US transceiver employing On-Off Keying (OOK) for a symmetric US data-link will be introduced. The US receiver (RX) comprises a low-noise amplifier (LNA) and a 10bit SAR ADC. On the transmitter side (TX), a class-D buffer has been chosen due to its high efficiency. OOK communication is selected. The time chosen for the "one" symbol is 3Q cycles, of which Q cycles are needed to start up and Q cycles to extinguish the oscillation. The time for the "zero" symbol is identical. Considering this, a data rate of 1kbps is specified. The transducer can be modeled by its electrical input capacitance,

\[
C_{in} = 2.1\text{nF}
\]

\[
V_{DD} = 0.8\text{V}
\]

\[
R_{m}, L_{m}, C_{m} = 434.4\Omega, 87\text{mH}, 0.192\text{nF}
\]

\[
P_{TX} = 47.82\mu\text{W}
\]

\[
Duty_{TX} = 2.5\%
\]

\[
P_{RX} = P_{TX} \cdot Duty_{TX} = 1.2\mu\text{W}
\]

\[
\text{NEF} = \approx 2
\]

\[
\text{BER} = < 10^{-3}
\]

\[
\text{Sensitivity} = \approx 80\text{dBm}
\]

\[
\text{Distance in water} = 2\text{km}
\]

Table I. SYSTEM SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_R)</td>
<td>40kHz</td>
</tr>
<tr>
<td>Data Rate</td>
<td>1kbps</td>
</tr>
<tr>
<td>(C_{in})</td>
<td>2.1nF</td>
</tr>
<tr>
<td>(V_{DD})</td>
<td>0.8V</td>
</tr>
<tr>
<td>(R_{m}, L_{m}, C_{m})</td>
<td>434.4\Omega, 87mH, 0.192nF</td>
</tr>
<tr>
<td>(P_{TX})</td>
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</tr>
<tr>
<td>(Duty_{TX})</td>
<td>2.5%</td>
</tr>
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<td>1.2\muW</td>
</tr>
<tr>
<td>(\text{NEF})</td>
<td>\approx 2</td>
</tr>
<tr>
<td>(\text{BER})</td>
<td>&lt; 10(^{-3})</td>
</tr>
<tr>
<td>(\text{Sensitivity})</td>
<td>&lt; 80dBm</td>
</tr>
<tr>
<td>(\text{Distance in water})</td>
<td>\approx 2km</td>
</tr>
</tbody>
</table>

II. SYSTEM DESIGN

A commercial US transducer [5] with a resonance frequency \(f_R\) of 40kHz is chosen. The system transfer characteristic, measured by exciting the transducer and recording the electric signal received from an identical transducer placed at 6cm distance in air is shown in Fig. 1. The bandwidth \(7.1\text{kHz}\) and the Q-factor \(5.6\) of the system are enough to support simple modulation schemes. To minimize the complexity of the base-band demodulation circuitry, OOK communication is selected. The time chosen for the "one" symbol is 3Q cycles, of which Q cycles are needed to start up and Q cycles to extinguish the oscillation. The time for the "zero" symbol is identical. Considering this, a data rate of 1kbps is specified. The transducer can be modeled by its electrical input capacitance, \(C_{in}\), in parallel with a series resonator comprising \(R_m\), \(L_m\) and \(C_m\), which models the transducer’s mechanic resonance [1]. The values of the different components in the transducer equivalent model have been estimated by impedance measurements and are reported in Table I. When driving the US transducer, a big portion of the used energy is dissipated to charge and discharge the electrical input capacitance \(C_{in}\). To minimize this loss, a 0.8V supply is chosen for the class-D buffer. Considering that transmitting a one and a zero have equal probability, the total transmitter power \(P_{TX}\) is simulated to be 47.82\muW when the buffer drives the electrical equivalent model of the transducer at frequency \(f_R\). It is assumed that the transmitting node sends once per second a 25b message, which contains e.g. data measured from internal sensors. This means that the transmitter can be duty cycled \(Duty_{TX}\) by a factor 25/1000=2.5%, bringing its average power consumption down to \approx 1.2\muW. A similar power budget is allocated for the receiver to balance the power used in the overall transceiver. The sensitivity level of the receiver can be estimated by assuming for the LNA a noise-efficiency factor (NEF) of 2 and a bias current of 0.8µA. In this case, the input integrated noise voltage is calculated...
as 2.9\(\mu\)V/\(\sqrt{Hz}\) in the transducer bandwidth. For a 10\(^{-3}\) BER in OOK, 16dB SNR at the input is sufficient, which means that -82dBm input signal can be successfully received, as shown in Table 1. Here, the effect of the quantization noise of the ADC at the input is assumed negligible, while a power of about 0.5\(\mu\)W is assigned to the ADC. The maximum communication distance that can be reached with this sensitivity is investigated by building an underwater lab setup in a water tank. The tank measures 0.4m by 1.1m by 0.5m and is filled with tap water to a depth of 0.25m. The TX transducer is driven by a 0.8V square wave at \(f_R\), while the power received by the RX transducer is recorded. Fig. 2 shows the underwater link characterization up to 1m distance, where the received power is modeled [4] according to

\[ P_{\text{rec}} = -k \cdot 10 \log d + P_0 \]  

(1)

In this equation \(d\) is the distance in cm, \(k\) is the path loss coefficient (which is found to be 1.05) and \(P_0\) is the initial power loss of -25.7dBm. This result is similar to what was reported in [4] and includes attenuation and path loss together. The received power at room temperature at 1m is \(\approx\) -47dBm. The outcome of this measurement is promising in the sense that, with the sensitivity we aim at, a communication distance in the order of 2km in water can be estimated using Eq.1. However, since the OOK communication is susceptible to echoes, the maximum achievable communication distance will be influenced by the multipath propagations in the environment.

III. CIRCUIT DESIGN

The class-D buffer in [6] is shown in Fig. 3 and redesigned to drive the US transmitting transducer. It consists of a level shifter input stage and 6 stages of inverter chain. Each stage is tapered by a factor 7 to drive a large capacitive load up to 2nF. In this circuit, thick-oxide transistors have been used together with a separate supply level, \(V_{DDH}\), which can be set higher than the one used for the receiver, to further increase the communication distance, or to cope with mediums like air where the attenuation is larger than in water. However, in this paper, the same supply is used for both TX and RX. The circuit proposed for the US LNA is shown in Fig. 4a. It exploits an inverter-based amplifier in open-loop to maximize gain and reduce the influence of the quantization noise of the ADC on the input-referred noise. Poor PSRR performance of the inverter-based topology can be tolerated in our application as we foresee a battery operated system, where the DC voltages are provided via external voltage regulators. The power overhead due to the LDOs is not considered in the rest of the paper. The inverter-based topology is chosen as both the pMOS (\(M_1\)) and the nMOS (\(M_2\)) transistors contribute to the total transconductance for a given current, thereby increasing current efficiency and enabling an NEF of 2 [7]. The capacitors \(C_{ac}\), are used to AC couple the inverter to the input of the receiver \(V_{in}\). Both transistors in the inverter are biased in the weak-inversion region and sized to have a \(gm/l_D\) ratio of about 31 [\(V^{-1}\)].
reference current $I_{bias}$ is provided to the chip, and internally mirrored (as in Fig. 4b) to bias the LNA and the error amplifier. The DC gate voltage of $M_1$ and $M_2$, $V_{bp}$ and $V_{bn}$, are provided via pseudo-resistors composed of two back-to-back diodes as shown in Fig. 4a. The value of $C_{dc}$ is 3.2pF and the pseudo-resistor value is simulated to be more than 3MΩ across PVT variations, so that the high-pass corner frequency is set below 20kHz. The DC point at the output of the inverter is stabilized via a negative feedback. This is achieved by comparing the LNA output, $V_{out}$, to a reference voltage, $V_{ref}$, and feeding back the error signal, $V_{fb}$, to the gate of two current control transistors $M_{p1}$ and $M_{p2}$. The DC feedback can efficiently compensate the errors due to leakage currents flowing in the pseudoresistors, and to mismatch between the biasing network and the transistors $M_1$ and $M_2$. $M_{p1}$ and $M_{p2}$ can indeed source (or sink) a suitable current in the output node, keeping the output DC voltage at the desired value. The schematic of the error amplifier is shown in Fig. 4c. Its output is connected to a 3.2pF capacitor, to filter out the signal from the DC stabilization loop. According to simulations, the feedback is able to stabilize the DC point with less than 7mV DC error across PVT variations. The output of the LNA is DC coupled to the ADC (Fig. 4a), which uses the same reference voltage, $V_{ref}$. The 10 bit asynchronous SAR ADC is designed as in [7]. The total current consumption of the LNA (including bias network and error amplifier) is simulated as 830nA and the sampling clock of the ADC is set to 400kHz to make the contribution of the quantization noise to the total input referred noise negligible. The simulated ADC power is $\approx 0.51\mu W$. A simulated input-referred noise density (IRND) of $20 \frac{V}{\sqrt{Hz}}$ is obtained at the typical corner, which enables a sensitivity level $<-80$dBm.

IV. MEASUREMENT RESULTS

A 65nm CMOS process is used for fabrication and the die photo of the proposed ultrasound transceiver is shown in Fig. 5. The measured transfer curve of the LNA is shown in Fig. 6, where a 30.7dB voltage gain is measured at 15kHz and the 3dB bandwidth (BW) is 40kHz. In Fig. 7, the measured IRND of the LNA is shown. The total integrated noise inside the transducer bandwidth is measured to be $2.2\mu V_{rms}$. The sensitivity level is validated with electrical BER measurements, where an OOK modulated signal with different amplitudes provided by a bench-top arbitrary signal generator (AWG Keysight 33500B) is given to the input of the receiver. 50dB attenuation is applied to the AWG output to bring the signal amplitude to the desired level. Fig. 8 shows BER plots for this electrical input signal, where a $-83$dBm input signal at 1kbps data-rate is demodulated with a $10^{-3}$ BER. Afterwards, an underwater test setup is built with transmitter, receiver and two US transducers. When a 40kHz, 0.8Vpp square wave input signal is given to the TX chip, around $\approx 80mV_{pp}$ signal (corresponding to $>54$dB SNR at the input of RX) is measured at 1m distance in the water tank. As the achievable communication distance in water exceeds the limits of a standard lab, we built another measurement test setup in air, as shown in Fig. 9, to be able to test the RX sensitivity at a manageable distance between the transducers. Here, OOK modulated random bits are generated in MATLAB and applied via an AWG to the transmitter chip, which drives the TX transducer. The resulting ultrasonic signal from the RX transducer is read-out via the receiver chain and the ADC output, $D_{out}$, is recorded via an external FPGA and transferred to a computer. There, a simple demodulation algorithm based on a band-pass filtering and a thresholding is implemented to detect the incoming bits. Due to the additional noise and echoes coming from the setup environment, a $10^{-3}$ BER with a sensitivity of $-81.6$dBm was achieved at a
communication distance of 3.2m. The total receiver power consumption of the LNA and ADC is measured as 1.18\(\mu W\). The measured power consumption of the transmitter is 50\(\mu W\). As a result, the overall energy consumption of the TX+RX link is measured as 51.18 \(nj/bit\). Furthermore, considering the Figure-of-Merit for wake-up receivers proposed \cite{8} as \(FOM_{\text{WuRx}} = \frac{\text{Energy}(J)}{\text{bit} \cdot P_{\text{sensitivity}}(W)}\), our receiver achieves a \(FOM_{\text{WuRx}}\) of \(8.2 \times 10^{-20}(J/b \cdot W)\). \(FOM_{\text{WuRx}}\) is measured excluding the power required to generate the ADC clock and the references. However, by reviewing relevant prior art \cite{7}, \cite{9} these overheads can be estimated to be much lower than the RX power and thus will not significantly change the overall results. A simple digital backend based on a threshold detector has also been implemented at transistor level and simulated: its power overhead (46nW) is negligible too in the total RX power budget.

V. DISCUSSION

The performance of the proposed US transceiver and its comparison with recent integrated US receivers is summarized in Table II. The work in \cite{3} achieves the lowest US receiver power while relaxing sensitivity. The works in \cite{1}, \cite{2} are designed as a wake-up receivers for an asymmetric US link, and achieve US receiver sensitivity of \(-81dBm\). The work in \cite{1} achieves a longer communication distance with less transmitting power, exploiting an optimized TX transducer with high transmit efficiency and a different, optimized receiving transducer. In contrast, our work uses the same commercial transducer for both transmission and reception. The proposed receiver achieves the best measured sensitivity of \(-81.6dBm\), which corresponds to a communication distance of 3.2m in air with the transducers used. Based on measurements, the communication distance predicted in water would be 2km to reach a \(10^{-3}\) BER level. To the best of our knowledge, the proposed transceiver achieves the lowest energy per bit performance of 51.18nJ/b and the best \(FOM_{\text{WuRx}}\) of \(8.82 \times 10^{-20}(J/b \cdot W)\) reported among US transceivers.

VI. CONCLUSION

Ultrasound communication is useful in resource-limited sensor networks using low bitrate communication and deployed in fluidic environments. This work focuses on the design of a symmetrical US communication link, where a similar average power budget is allocated to the transmitter and the receiver to efficiently use the available energy. Measurement results show that the proposed circuits achieve this goal at 1kbps data rate and a state-of-the-art sensitivity, energy per bit, and \(FOM_{\text{WuRx}}\) for a US transceiver.

ACKNOWLEDGEMENT

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REFERENCES


Table II. PERFORMANCE COMPARISON OF THE PROPOSED US TRANSCIVER WITH PRIOR ART

<table>
<thead>
<tr>
<th>Technology [nm]</th>
<th>65</th>
<th>250</th>
<th>65</th>
<th>65</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Frequency [kHz]</td>
<td>40</td>
<td>41</td>
<td>57</td>
<td>40</td>
</tr>
<tr>
<td>Supply Voltage [V]</td>
<td>0.6</td>
<td>0.3</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>Modulation</td>
<td>OOK</td>
<td>OOK</td>
<td>OOK</td>
<td>OOK</td>
</tr>
<tr>
<td>Data Rate [bps]</td>
<td>220</td>
<td>250</td>
<td>906</td>
<td>1000</td>
</tr>
<tr>
<td>Receiver Power [(\mu W)]</td>
<td>4.4</td>
<td>4</td>
<td>0.80</td>
<td>1.18*</td>
</tr>
<tr>
<td>Sensitivity [dBm]</td>
<td>-81</td>
<td>-81</td>
<td>-59.7</td>
<td>-81.6</td>
</tr>
<tr>
<td>(FOM_{\text{WuRx}}) ((J/b \cdot W)\cdot 10^{-20})</td>
<td>13.98</td>
<td>3.18</td>
<td>2.55</td>
<td>0.82</td>
</tr>
<tr>
<td>Transmitter Power [(\mu W)]</td>
<td>16</td>
<td>1000</td>
<td>N/A</td>
<td>50</td>
</tr>
<tr>
<td>Distance- in air [m]</td>
<td>8.6</td>
<td>6.3</td>
<td>3.3</td>
<td>3.2</td>
</tr>
<tr>
<td>Distance- in water [km]</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>2</td>
</tr>
<tr>
<td>FoM-Energy/Bit (full link)</td>
<td>8.6nJ/b</td>
<td>4(\mu J/b)</td>
<td>N/A</td>
<td>51.18nJ/b</td>
</tr>
</tbody>
</table>

*Excludes the power needed for the ADC clock and the reference generation.