

An integrated high frequency, narrow band, high-resolution synthesizer

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An Integrated High-Frequency Narrow-Band High-Resolution Synthesizer

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Abstract—A frequency synthesizer employing a new digital-frequency measurement method in a feedback loop is described. The synthesizer features high-frequency resolution and a high operating frequency. The mostly digital nature of the synthesizer and relaxed voltage-controlled oscillator requirements also make the synthesizer suitable for integration. Models for the synthesizer are developed and experimental results from a prototype are given.

Index Terms—Frequency-locked loops, frequency synthesizer, phase-locked loops, phase noise.

I. INTRODUCTION

THE SYNTHESIS of frequencies slightly offset from a nominal frequency has received some attention in the literature. In particular, the following broad classes of frequency synthesizer have been employed.

- 1) Passive or direct frequency synthesis, which involves the synthesis of a frequency from one or more reference frequencies via harmonic generators, mixers, filters, and dividers [1], [2].
- 2) Indirect or coherent synthesis employing phase-locked loops (PLL). Typically, fractional-N techniques are employed to obtain high-frequency resolution [2]–[4].
- 3) Direct digital synthesizers, which employ digital computation and digital-to-analog conversion to generate the signals [5].

The synthesizer described in this paper was designed for testing of frequency justification mechanisms employed in digital transmission systems. In particular, the application required several tens of independent frequency sources each in the range of 139.264-MHz \pm 20 parts per million (ppm), with each frequency source having a frequency resolution of about 0.1 ppm. Due to the large number of synthesizers required, the synthesizer would need to be: 1) small; 2) highly integrated; 3) low cost; 4) low power; and 5) allow several synthesizers to be placed on a printed circuit board.

The requirements ruled out the direct synthesis techniques mentioned above. Fractional-N PLL synthesizer techniques would be the most appropriate. However, due to the high-frequency resolution required, very high-quality voltage-

controlled oscillators (VCO's) or complex analog phase-compensation schemes would be required.

To meet the requirements, the synthesizer was implemented using a frequency-locked loop (FLL). A new frequency measurement method, referred to as the precise digital-frequency detector (PDFD) [6], [7], was used in the FLL to measure the difference between the output and reference frequencies. The PDFD has the ideal characteristic of no frequency offsets, however it only operates over a narrow frequency range. The PDFD was coupled with integration in an FLL so that the output frequency had an exact relationship to the reference frequency.

The rest of this paper is organized as follows. First, in Section II, the overall structure and operation of the synthesizer is described. In Section III, a linearized discrete time model for the synthesizer is given. Furthermore, the synthesizer model is shown to be equivalent to the model of a discrete-time PLL [9]. Bounds on the deviation from the linear model due to the nonlinear characteristics of the PDFD are given in Section IV. In Section V, a steady-state nonlinear mode of operation of the synthesizer is proposed for when there is a frequency offset. Using this model, the magnitude of spurs in the spectrum of the synthesizer output are derived. Finally, in Section VI, some details on the implementation of a prototype synthesizer are given. Also, experimental results are presented which support the models given in Sections III and V.

II. STRUCTURE AND OPERATION OF SYNTHESIZER

The synthesizer consists of the PDFD, a digital integrator, and a VCO in a feedback loop (see Fig. 1). The synthesizer VCO generates a square wave output. The main synthesizer input is the sampling clock of frequency f_c . A qualitative description of the operation of the synthesizer and the PDFD is now given. Initially the offset generation block is removed.

The concept of phase for a square wave will be clarified at this point. The square wave waveform $v(t)$ is related to the square wave phase $\theta(t)$ as follows:

$$v(t) = \begin{cases} 1, & p \leq \theta(t) < p + 1/2 \\ 0, & p + 1/2 \leq \theta(t) < p + 1 \end{cases} \quad p \in Z \quad (1)$$

where Z denotes the set of integers. As can be seen from (1), $\theta(t)$ going from zero to one delineates one cycle of the square wave.

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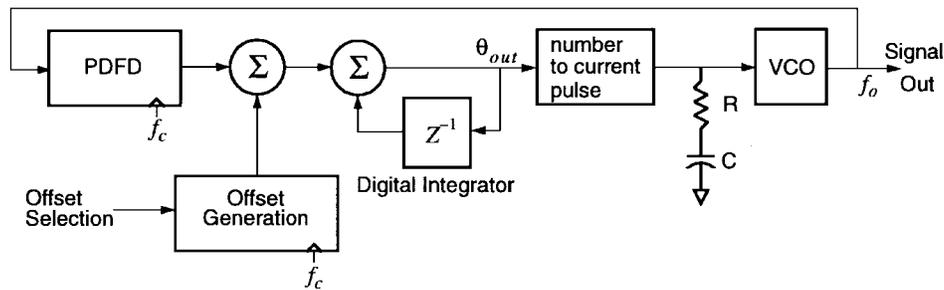


Fig. 1. Structure of synthesizer.

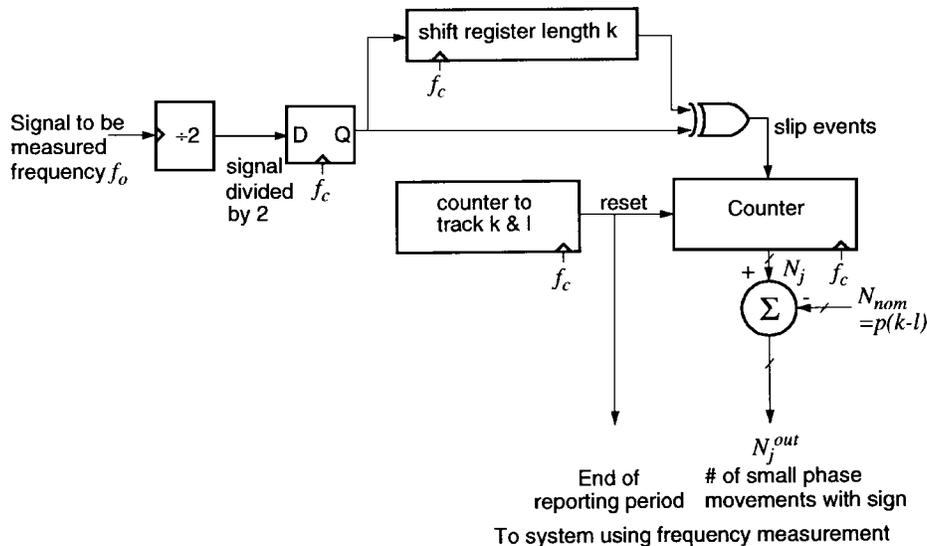


Fig. 2. Structure of a simple PDFD.

A. Description of the PDFD

A qualitative description of the operation of the PDFD is presented in this section. A more detailed analysis can be found in [6], [7].

As shown in Fig. 2, the PDFD is a simple digital circuit constructed from flip-flops and logic gates clocked at a rate f_c . A major advantage of the PDFD is that small phase movements (less than say 1/100th of a cycle) can be measured, even though the PDFD samples at a lower rate than the synthesizer output signal. Thus the clock rate f_c is low for the accuracy achieved. All other digital-frequency measurement techniques can only measure phase movements of more than a cycle or otherwise require high clock rates.

The task of the PDFD is to measure the phase movements of the output signal, of frequency $f_o(t)$, with respect to a square wave of frequency $f_{snom} \cdot f_{snom}$ is the nominal operating frequency of the synthesizer, that is the output frequency for which the offset block does not insert a frequency offset. Note also that the square wave of frequency f_{snom} to which the signal output is compared does not physically exist. f_{snom} is related to f_c by a rational number which depends on PDFD design parameters.

With regards to Fig. 2, the signal square wave of frequency f_o is divided by two to produce a square wave of 50/50 mark-

space ratio and frequency $f_o/2$. This divided-down square wave is then sampled at a rate of f_c samples per second. Fig. 3 illustrates the sampling of the square wave.

A first step in the processing is to divide the stream of binary samples into k lower sample rate streams. Each stream consists of samples spaced k/f_c s apart. Furthermore, l out of the possible k streams are used (see Fig. 3). Each of the k streams has an initial starting phase; for the i th lower sample rate stream, the starting phase is denoted by θ_{init}^i , ($i \in [0, 1, 2, \dots, l-1]$). θ_{init}^i is the phase relationship between the instant of the first sample in one of the k streams and the next edge of the signal square wave. θ_{init}^i is a dimensionless quantity defined such that θ_{init}^i/f_s is the actual time delay between the relevant epochs (Fig. 3).

Consecutive samples in each of the k streams are compared with each other using the XOR gate and shift register in Fig. 2. A one output from the XOR gate indicates when the signal square-wave phase moves a complete cycle with respect to a square wave of frequency f_{cmp} . The square wave of frequency f_{cmp} does not physically exist, as in the case of $f_{snom} \cdot f_{cmp}$ is related to the PDFD parameters f_c , f_{snom} , and k . More precisely, a one output from the XOR gate indicates a phase movement corresponding to a complete cycle when $(\theta_{init}^i + \theta_{slip})$ equals an integer, and where θ_{slip} is the phase movement of the signal square wave with respect to a square

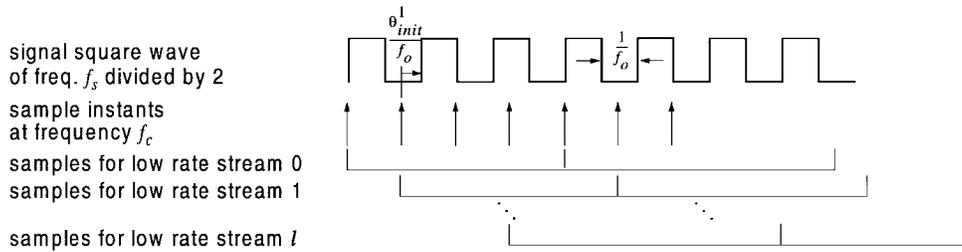


Fig. 3. Sampling of the signal and pairing the samples.

wave of frequency f_{cmp} ; that is

$$\theta_{\text{slip}} = (f_{\text{cmp}} - f_s)t. \quad (2)$$

As shown in Fig. 3, the θ_{init}^i for each of the k streams will be different, due to the different starting times. Out of the k possible streams, the l used in the PDFD can be chosen so that the θ_{init}^i will be uniformly distributed across a signal square-wave cycle.

In a period of $T = k/f_c$ s, each of the l streams will have an opportunity to report its decision on a phase movement of a complete cycle. Let the integers N_j represent the total number of complete cycle-phase movements reported by all streams in the j th interval of T s. N_j will have a value between zero and l . The value of a particular N_j in the sequence represents the phase movement of the signal square wave with respect to a square wave of frequency f_{cmp} that occurred in the j th interval.

To obtain the phase movement with respect to a square wave of frequency f_{snom} , an offset N_{nom} is subtracted from N_j (Fig. 2). N_j^{out} output from the PDFD is digitally integrated. The value of the integrator is the total phase movement, between the output square wave and a square wave of frequency f_{snom} , that has occurred since the PDFD start. The phase movement is quantized to $1/l$ th of a signal output cycle. In [6], [7], it has been shown that the PDFD characteristic approximates a perfect constant step quantizer. However, to make the analysis tractable, we will assume here that the PDFD is an ideal quantizer; that is, the PDFD is modeled by the following equation:

$$\theta_{\text{out}} = \frac{\lfloor l\theta_{\text{slip}} \rfloor}{l} \quad (3)$$

where θ_{slip} is the phase movement between the signal-out square wave and the square wave of frequency f_{snom} , since the start of the synthesizer until the present time t

$$\theta_{\text{slip}}(t) = \theta_{\text{snom}}(t) - \theta_o(t) = f_{\text{snom}}t - \int_0^t f_o(x) dx. \quad (4)$$

$\lfloor x \rfloor$ in (3) denotes the floor function; that is, the greatest integer less than or equal to x [8].

B. Description of Synthesizer

Every T s, a current pulse whose width represents the integrator value magnitude is generated by the “number-to-current pulse” block (Fig. 1). The current output can have an instantaneous current value of $+I$, 0 or $-I$ amps, with the

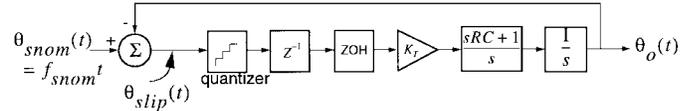


Fig. 4. Model for synthesizer.

sign of the instantaneous current being the same as the sign of the integrator.

The output current is applied to an analog filter implemented with a resistor and capacitor. The voltage out of the filter is applied to the VCO. The filter is identical to that used in charge-pump PLL's [10]. It has the transfer function from current $I(s)$ at the input, to voltage $V(s)$ output to the VCO

$$\frac{V(s)}{I(s)} = \frac{sRC + 1}{s}. \quad (5)$$

The feedback system drives the frequency of the output signal $f_o(t)$ to maintain the phase movement between $f_o(t)$ and f_{snom} , since the start of the PDFD is at zero.

Consider now the synthesizer operation with the offset generation block present. The offset block adds, at regular intervals, ± 1 to the input of the digital integrator. The offset selection determines whether $+1$ or -1 is added, and the time between when ± 1 is added. The feedback system drives the output $f_o(t)$ to maintain the state of the integrator at zero. When an offset of ± 1 is added to the integrator, the feedback system forces the phase of the output to move by $1/l$ th of a cycle, with respect to the square wave of frequency f_{snom} . This movement is in a direction so as to cancel the offset added to the integrator. With offsets added at regular intervals, the output is constantly slipping with respect to the square wave of frequency f_{snom} . Hence, the frequency of the output $f_o(t)$ is slightly offset from f_{snom} .

III. LINEARIZED DISCRETE TIME MODEL FOR SYNTHESIZER

A model of the synthesizer is shown in Fig. 4 (without frequency offsetting). Note that the sampling period for the discrete time components is T s.

The PDFD, digital integrator, and number-to-current pulse blocks of Fig. 1 have been modeled in Fig. 4 as: 1) phase movement quantizer; 2) a delay of one sampling period T ; and 3) a zeroth-order hold (ZOH).

In Fig. 4, K_T is the product of all the gains in the system and is given by

$$K_T = \frac{lK_o I_{\text{ave}}}{C} \quad (6)$$

where K_o is the gain of the VCO in megahertz per volt. I_{ave} is given as follows:

$$I_{ave} = \frac{T_p I}{T}. \quad (7)$$

T_p is the current pulse width output, in seconds, when the integrator has a value of one. I is the instantaneous pulse current, as previously mentioned. I_{ave} is the ratio of the time averaged current output to the analog filter and the value held in the integrator.

If the quantizer is removed then the synthesizer can be considered a linear system. Denote by $\Theta_{snom}(z)$ the z -transform of the series $\theta_{snom}(mT)$ ($m \in [0, 1, 2, \dots]$), which is obtained by sampling $\theta_{snom}(t)$ once every T s. Similarly, denote by $\Theta_{ol}(z)$, the z -transform of the series $\theta_{ol}(mT)$ obtained from sampling $\theta_{ol}(t)$, where $\theta_{ol}(t)$ is the phase output of the linear model of the synthesizer. The closed-loop transfer function of the synthesizer can be found to be

$$H(z) = \frac{\Theta_{ol}(z)}{\Theta_{snom}(z)} = \frac{K_f + K_p(z-1)}{K_f + K_p(z-1) + z(z-1)^2} \quad (8)$$

where

$$K_f = K_T T^2 \quad (9)$$

$$K_p = \frac{K_T T^2}{2} + \frac{K_T T}{\omega_z}. \quad (10)$$

Equation (8) is the transfer function of a type II discrete time PLL. These discrete time PLL's have been studied in [9]. In particular, (8) represents the type II PLL with extra delay of T s ($M=1$) [9]. K_p and K_f are equal to the parameters K_p^t and K_f^t in [9].

The analog filter (Fig. 1) located between the digital current outputs and the VCO can be considered to have an integral and a proportional path. The capacitor in the filter is the integral path. It integrates the current output, and the voltage across it is constantly applied to the VCO. The resistor in the filter is the proportional path. The resistor has a voltage across it when a current pulse occurs. K_p is the gain associated with the proportional path, and K_f is the gain associated with the integral path.

In [9], the values of the parameters K_p and K_f , for which the system is stable, are given. With K_p and K_f chosen for a stable system, it can be shown that in the steady state, the sampled phase error $\theta_{slip}(mT)$ is zero; hence, $\theta_{ol}(mT)$ equals $\theta_{snom}(mT)$. Which implies the output frequency equals f_{snom} , as would be expected for a type II PLL.

IV. BOUNDS ON DEVIATION FROM LINEAR MODEL

The nonlinear quantizer component of the synthesizer will cause a departure from the linear model of Section III. This section derives bounds on the difference between the output

of the real synthesizer with quantizer and the output of the linear model.

The synthesizer can be considered a digital control system. The effect of quantizers in digital control systems has received considerable attention in the literature. The results of [11] are the most relevant to the synthesizer.

The method presented in [11] obtains only the steady-state error due to a sustained maximum quantization error at every sampling period. This steady-state upper bound is not valid, as a dynamic upper bound, except for the limited case where all of the impulse responses of the control system are over-damped (constant polarity in sign). The impulse response of the synthesizer can not be over-damped due to the terms in the numerator of the synthesizer transfer function (8). Hence, the method of [11] can not be directly applied.

However, some progress can be made by considering a simplified synthesizer model. We assume that the voltage across the capacitor (that is the integral path) is effectively constant after the synthesizer start up period. For the voltage to be effectively constant requires that

$$K_f \ll K_p. \quad (11)$$

With condition (11) satisfied, K_p (the proportional path gain) can be approximately given by

$$K_p \approx l K_o I_{ave} R T. \quad (12)$$

Since we have assumed the capacitor plays no part in the dynamics of the synthesizer, we will remove it from the model. The transfer function for the simplified linear model of the synthesizer that results is given in (13), shown at the bottom of the page.

With K_p chosen as follows (14), the impulse responses of the simplified synthesizer model are overdamped, and the method of [11] can be used to obtain a dynamic upper bound on the quantization error

$$K_p \leq 1/4. \quad (14)$$

The result is that the difference between the output of the real synthesizer with quantizer [denoted $\theta_o(mT)$] and the output of the linear model [denoted $\theta_{ol}(mT)$] is bounded as follows:

$$0 \leq \theta_{ol}(mT) - \theta_o(mT) \leq \frac{1}{l}. \quad (15)$$

From (15), it can be seen that there will be a small time-varying difference between the real synthesizer output $\theta_o(mT)$ and $\theta_{ol}(mT)$ [which is to equal $\theta_{snom}(mT)$]. It can be concluded that the undesirable effect of the quantizer is to create jitter in the output signal. The peak-to-peak amplitude of this jitter will be $1/l$ th of a cycle. The spectral characteristics of this jitter are derived in Section V.

In the FLL synthesizer developed here, it is desirable to have a large closed-loop bandwidth to reduce the effects of VCO

$$H(z) = \frac{K_p}{z^2 - z + K_p} = \frac{K_p}{(z - (1 + \sqrt{1 - 4K_p})/2)(z - (1 - \sqrt{1 - 4K_p})/2)}. \quad (13)$$

phase noise. The closed-loop bandwidth of the synthesizer [without the capacitor in the model (13)] $f_{3\text{dB}}$ can be found to be

$$f_{3\text{dB}} = \frac{1}{2\pi T} \arccos \left(\frac{1 + K_p - \sqrt{1 - 6K_p + 9K_p^2 + 4K_p^3}}{4K_p} \right) \approx \frac{K_p}{2\pi T}. \quad (16)$$

Note unlike that in synthesizers based on PLL's, $f_{3\text{dB}}$ is independent of frequency-resolution requirements. However, small phase excursions, much less than a quantization level ($1/l$ th of a cycle), caused by phase noise will not be detected by the PDFD. Unlike in a PLL, these phase excursions will not be corrected, and phase noise significantly below a quantization level will not be reduced.

Phase noise larger than the quantization level and much closer in frequency than $1/T$ Hz to f_{snom} will be reduced in the same way as in a PLL. Specifically, phase noise at offset ω r/s from f_{snom} will be attenuated by the factor $1/|1 + G(j\omega)|$ where $G(s)$ is the forward gain of the synthesizer (Fig. 4) and is

$$G(s) = \frac{K_T(sRC + 1)}{s^2}. \quad (17)$$

V. STEADY-STATE OPERATION WITH FREQUENCY OFFSET AND SPUR GENERATION

The steady-state operation of the synthesizer when a frequency offset is required is now considered. In particular, a stochastic model for the operation of the synthesizer when the frequency offset is small is proposed. Using the stochastic model, the height of spurs in the spectrum of the output signal are derived.

It is assumed that the offset generation block adds plus one into the integrator every T_0 s. The case of -1 being added can be dealt with in a manner similar to the $+1$ case. Furthermore, it is assumed that T_0 is of the order of several hundred T , thus causing a very small frequency offset from f_{snom} , f_{off} . The offset f_{off} is given by

$$f_{\text{off}} = \frac{1}{lT_0}. \quad (18)$$

It is also assumed, as in Section IV, that the integral component of the analog filter (Fig. 1) is effectively constant. Furthermore, the constant integral component, which is the voltage across the capacitor, is assumed to be a constant V_{cap} volts

$$V_{\text{cap}} = \frac{f_{\text{snom}} + f_{\text{off}}}{K_o}. \quad (19)$$

A brief qualitative description of the dynamics of the synthesizer is now given. Shortly after the offset generation block adds one to the integrator, a positive current is output to the analog filter (see Fig. 5). This current drives the output phase through the proportional path of the filter. The current lasts until the output phase is sufficiently increased to cause $\theta_{\text{slip}}(t)$ to cross a quantization level (see Fig. 5). When the

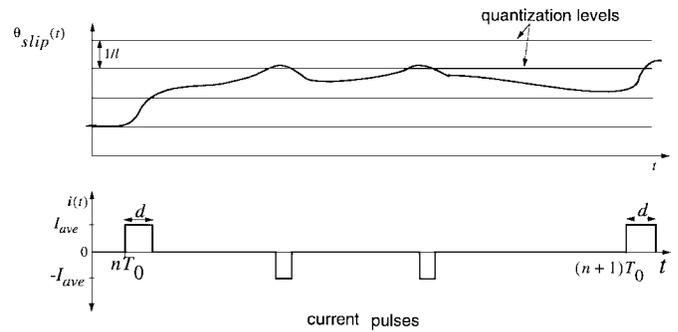


Fig. 5. Behavior of phase error and current pulse over one offset cycle T_0 for small frequency offsets.

quantization level is crossed, a -1 is output from the PDFD and the integrator returns to zero.

We denote the time-varying current output to the analog filter by $\mathbf{i}(t)$. We assume the current pulses in $\mathbf{i}(t)$ have magnitude I_{ave} and a minimum duration of T s (see Fig. 5). The short current pulses of magnitude I amps that actually occur at the analog filter input are being approximated as longer pulses of I_{ave} amps. This approximation simplifies the analysis as the current pulses will typically occur over several consecutive sampling periods. For example, to drive $\theta_{\text{slip}}(t)$ through a whole quantization level will take $1/K_p$ sampling periods. Furthermore, due to the delay after the quantizer and the ZOH (Fig. 4), current pulses will occur over at least two sampling periods.

In the time between the offset generation block adding ones, the phase error $\theta_{\text{slip}}(t)$ drifts in the space it was left in between two quantization levels. Due to the voltage across the capacitor V_{cap} , the drift will generally be upwards. However, since f_{off} is very small, noise in the various components of the synthesizer will have a significant effect on $\theta_{\text{slip}}(t)$. When $\theta_{\text{slip}}(t)$ crosses the upper quantization level, $\theta_{\text{slip}}(t)$ will be forced back below it by the PDFD and integrator. Similarly, if noise is sufficient to cause $\theta_{\text{slip}}(t)$ to occasionally cross the lower quantization level, $\theta_{\text{slip}}(t)$ will be forced back above it by the PDFD and integrator. Due to the upwards drift from V_{cap} , the number of crossings of the upper quantization level will be significantly greater than those of the lower quantization level.

This process of driving $\theta_{\text{slip}}(t)$ over a quantization level, then letting it drift between quantization levels is repeated every T_0 s. The assumption of constant V_{cap} implies that, in the long term, the current into the analog filter is zero. Thus, in the long term, the number of positive current pulses equals the number of negative current pulses.

In Appendix A, a stochastic model for $\mathbf{i}(t)$ is proposed, based on the behavior given above. The stochastic model for $\mathbf{i}(t)$ predicts that the spurs in the output spectrum will occur at frequencies $f_{\text{snom}} + f_{\text{off}} \pm n/T_0$, $n \in [1, 2, 3, \dots]$. Also, the magnitude of the spurs with respect to the fundamental frequency spectral line are predicted to be

$$\frac{T_0}{l(T_0 - d)n} \left(\text{sinc} \left(\frac{\pi nd}{T_0} \right) \right) \quad (20)$$

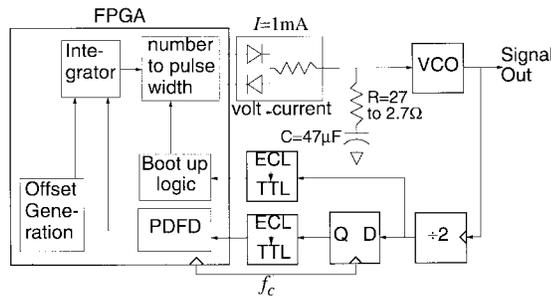


Fig. 6. Diagram of prototype synthesizer.

TABLE I
EXPERIMENTAL SYNTHESIZER PARAMETERS

Parameter	Value
f_{snom}	139.264 MHz
f_c	$(96/235) \times 139.264$ MHz (~ 57MHz)
l	96
k	97
K_p	0.48 to 0.048
K_f	6.4×10^{-4}
T	1.705×10^{-6} s
T_p	17.6×10^{-9} s

where d is the width of the positive current pulse output to the analog filter (see Fig. 5).

From (20), it can be seen that for $d \ll T_0$, the magnitude of the $n = 1$ spectral line will be approximately $1/l$. It can be concluded that for small frequency offsets (where $d \ll T_0$), the spectral purity of the synthesizer output is primarily determined by the PDFD quantization level ($1/l$).

For larger frequency offsets with T_0 being of the order of ten T , the behavior of $\theta_{slip}(t)$ is markedly different from the small-frequency offset case. A model for the large-frequency offset is not given here. However, the spur heights are significantly less than for small-frequency offsets. Furthermore, the spur heights are not determined by the PDFD quantization level, but are strongly dependent on K_p .

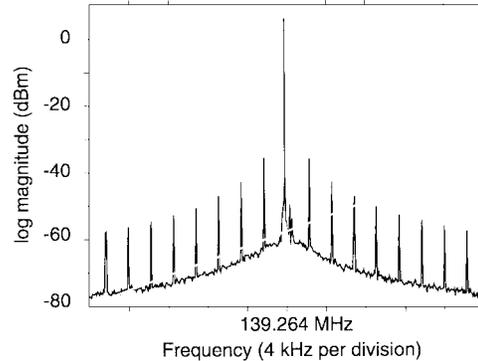
VI. EXPERIMENTAL RESULTS

1) *Prototype Synthesizer*: A prototype synthesizer was constructed using a field programmable gate array (FPGA) to implement the majority of the digital devices, see Fig. 6. An emitter-coupled logic (ECL) VCO (Motorola MC12148) was employed. A pair of diodes and a resistor were used to convert the voltage output of the FPGA to a current source. The boot-up logic (Fig. 6) was employed at start up to force the VCO frequency into the operating range of the PDFD. The synthesizer occupied just 8×5 cm on a printed circuit board, which contained eight such synthesizers. The parameters and component values for the synthesizer are given in Table I and Fig. 6.

2) *Quantization Effects*: To check that the effects of phase quantization were as predicted in Section IV, the synthesizer was run without any frequency offset and the output waveform was observed on an oscilloscope. The oscilloscope was triggered by a commercial synthesizer generating the same

TABLE II
POWER SPECTRAL LINE HEIGHTS WITH RESPECT TO MAIN
SPECTRAL LINE AT $f_{snom} + f_{off}$ FOR $T_0 = 256T$

	n	1	2	3
$K_p = 0.48$	Predicted (20)	-39.6 dB	-45.7 dB	-49.1 dB
	Experimental	-39.7 dB	-45.8 dB	-49.1 dB
$K_p = 0.178$	Predicted (20)	-39.5 dB	-45.5 dB	-49.1 dB
	Experimental	-39.8 dB	-47.1 dB	-51.4 dB
$K_p = 0.048$	Predicted (20)	-39.0 dB	-45.4 dB	-49.4 dB
	Experimental	-39.4 dB	-48.9 dB	-59.2 dB

Fig. 7. Typical output spectrum of synthesizer, for $T_0 = 256$, (giving $f_{off} = 24$ Hz) $K_p = 0.178$.

frequency as the synthesizer. The spread of the zero crossings seen on the oscilloscope was found to be 75 ps, approximately $1/10$ th of a cycle, as predicted.

3) *Spectral Lines*: The synthesizer was run with various values of K_p with $T_0 = 256T$. Dominant spectral lines at the frequencies $f_{snom} + f_{off} \pm n/T_0$, as predicted in Section V, were found. Their heights, with respect to the height of spectral line at $f_{snom} + f_{off}$, are recorded in Table II. A typical spectrum is also shown in Fig. 7.

As can be seen in Table II, the $n = 1$ spectral line is well predicted by (20) for all K_p . For K_p equal to 0.48, the spectral lines associated with higher n are also very well predicted. The excellent agreement is most likely because the assumption of $\theta_{slip}(t)$ being driven through a whole quantization level when a one is added into the integrator will be satisfied (see Appendix A). Once a one is added to the integrator, a current is pumped into the analog filter until the PDFD detects that a quantization level is crossed. Due to the delay in the PDFD and the ZOH, current will be pumped into the analog filter for at least $2T$. With K_p equal to 0.48, $\theta_{slip}(t)$ will be moved 0.96 of a quantization interval in $2T$, almost a whole quantization interval.

VII. CONCLUSION

A synthesizer based on an FLL was presented. The FLL was mathematically similar to a PLL in that the output frequency was precisely related to the reference frequency. However, unlike a PLL, absolute phase was not measured. Rather, phase-movement measurement coupled with perfect integration gave a similar result to absolute phase measurement. A stochastic

model was developed to predict the height of spurs, and the accuracy of the model was experimentally verified.

The FLL synthesizer can synthesize frequencies arbitrarily close to the nominal frequency, while maintaining a large loop bandwidth to suppress VCO phase noise. This high-frequency resolution is due to the digital nature of the FLL. Furthermore, the digital nature permits an economical highly integrated realization of the synthesizer.

However, the digital nature of the FLL introduces some noise into the synthesized output due to the quantization of phase movement. The small phase-movement quantization was acceptable for the particular application. The digital-frequency measurement method employed, the PDFD, has a narrow operating frequency range when the phase-movement quantization is small [6], [7]. This narrow operating range restricts the range of synthesizable frequencies. Reducing the phase movement quantization further restricts the range of synthesizable frequencies.

APPENDIX A

STOCHASTIC MODEL TO DETERMINE SPUR MAGNITUDE

From the behavior of the synthesizer described in Section V, a probability density function $f(i; t_1)$ for the current output to the analog filter $\mathbf{i}(t)$ can be developed (see (21), found at the bottom of the page).

For any integer n , note that the high-current pulse is centered on time nT_0 rather than following nT_0 for mathematical convenience only.

To obtain the spectrum of the synthesizer output, we first determine the spectrum of $\mathbf{i}(t)$ from its autocorrelation function. We will assume that $f(i; t_1)$ is statistically independent from $f(i; t_2)$ for all t_1, t_2 to simplify the calculation of the autocorrelation of $\mathbf{i}(t)$, $R(t + \tau, t)$. With T_0 being many times T , the assumption of statistical independence is valid.

$\mathbf{i}(t)$ is a cyclostationary process [12]. A new shifted process $\tilde{\mathbf{i}}(t)$, which has stationary statistics, is generated from $\mathbf{i}(t)$ by introducing a random variable uniformly distributed across $(0, T_0)$ [12]. The autocorrelation function of the shifted process $\tilde{\mathbf{i}}(t)$, $\bar{R}(\tau)$ can be found from the autocorrelation function of the cyclostationary process $R(t + \tau, t)$ [12]

$$\bar{R}(\tau) = \frac{1}{T_0} \int_0^{T_0} R(t + \tau, t) dt. \quad (22)$$

The result being that $R(\tau)$ is found to be the following periodic triangular waveform:

$$\bar{R}(\tau) = \begin{cases} \frac{I_{ave}^2 d}{T_0 - d} \left(1 - \frac{T_0}{d(T_0 - d)} |\tau|\right), & |nT_0 - \tau| \leq d \\ -\left(\frac{I_{ave} d}{T_0 - d}\right)^2, & |nT_0 - \tau| > d. \end{cases} \quad (23)$$

$\bar{R}(\tau)$ can be expressed as the following Fourier series

$$\bar{R}(\tau) = \sum_{n=-\infty}^{\infty} F_n e^{jn2\pi(\tau/T_0)} \quad (24)$$

$$F_0 = 0 \quad (25)$$

$$F_n = \left(\frac{I_{ave} d}{T_0 - d} \left(\text{sinc}\left(\frac{\pi n d}{T_0}\right)\right)\right)^2 \quad (26)$$

where

$$\text{sinc}(x) = \frac{\sin(x)}{x}. \quad (27)$$

The power spectrum of $\mathbf{i}(t)$ can be found by taking the Fourier transform of $\bar{R}(\tau)$.

$\mathbf{i}(t)$ modulates the VCO through the proportional path of the analog filter. The phase excursions caused by $\mathbf{i}(t)$ are of the order of $1/l$ th of a cycle, with l typically being of the order of 100. With such small phase movements, $\mathbf{i}(t)$ effectively narrow-band frequency modulates the VCO. Knowing the spectrum of $\mathbf{i}(t)$ allows the spectrum of the VCO output and, hence, the synthesizer output to be found [13]. The spectrum of the synthesizer output $\Theta_o(2\pi f)$ is found to be

$$\begin{aligned} \Theta_o(2\pi f) &= A_c \delta(f - (f_{\text{snom}} + f_{\text{off}})) \\ &+ A_c \sum_{n=-\infty}^{\infty} \frac{T_0 R K_o I_{ave} d}{n(T_0 - d)} \left(\text{sinc}\left(\frac{\pi n d}{T_0}\right)\right) \\ &\cdot \delta\left(f - \left(f_{\text{snom}} + f_{\text{off}} + \frac{n}{T_0}\right)\right) \end{aligned} \quad (28)$$

where A_c is related to the amplitude of the square wave output from the VCO. Note that if the VCO outputs a square wave, there will of course be other spectral lines at odd multiples of the fundamental frequency $f_{\text{snom}} + f_{\text{off}}$. The spectrum $\Theta_o(2\pi f)$ given in (28) only provides the spectrum close to the fundamental frequency.

If we assume that each time the offset generation adds a one to the integrator, $\theta_{\text{slip}}(t)$ will be driven through a whole quantization level, then d can be found

$$d = \frac{T}{K_p}. \quad (29)$$

Using (12) and (29), the coefficient in the summation of (28) can be simplified to

$$\frac{T_0 R K_o I_{ave} d}{n(T_0 - d)} \left(\text{sinc}\left(\frac{\pi n d}{T_0}\right)\right) = \frac{T_0}{l(T_0 - d)n} \left(\text{sinc}\left(\frac{\pi n d}{T_0}\right)\right). \quad (30)$$

$$f(i; t) = \begin{cases} \delta(i - I_{ave}), & nT_0 - \frac{d}{2} \leq t < nT_0 + \frac{d}{2} \\ \left(\frac{T_0 - 2d}{T_0 - d}\right) \delta(i) + \left(\frac{d}{T_0 - d}\right) \delta(i + I_{ave}), & nT_0 + \frac{d}{2} \leq t < (n+1)T_0 + \frac{d}{2} \end{cases} \quad (21)$$

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