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Citation for published version (APA):

Bolk, J., Ambrosius, H., Stabile, R., Latkowski, S., Leijtens, X., Bitincka, E., Augustin, L., Marsan, D., Darracq, J., & Williams, K. (2018). Deep UV lithography process in generic InP integration for arrayed waveguide gratings. *IEEE Photonics Technology Letters*, 30(13), 1222-1225. <https://doi.org/10.1109/LPT.2018.2840224>

DOI:

[10.1109/LPT.2018.2840224](https://doi.org/10.1109/LPT.2018.2840224)

Document status and date:

Published: 01/07/2018

Document Version:

Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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Deep UV Lithography Process in Generic InP Integration for Arrayed Waveguide Gratings

J. Bolk, H. Ambrosius, R. Stabile, S. Latkowski, X. Leijtens, E. Bitincka, L. Augustin, D. Marsan, J. Darracq and K. Williams

Abstract—Low-excess-loss arrayed waveguide gratings are enabled by unique application of deep UV lithography in InP integrated photonics through reduced feature sizes and more specifically, well-resolved inter-waveguide gap dimensions. Submicrometer wafer-flatness is shown to be required to achieve critical dimension uniformity better than 10 nm on 3-inch substrates. Arrayed waveguide grating devices were fabricated and the effect of inter-waveguide gap scaling on the excess losses, was measured and compared to simulations. Excess losses down to 0.15 dB were demonstrated to be lower than predicted with 2D simulations. The tapering of the etch depth inside the gaps due to the lag effect of the etch process may explain the improvements.

Index Terms— Arrayed Waveguide Grating, Indium Phosphide, Lithography, Photonic Integrated Circuit

I. INTRODUCTION

Arrayed waveguide gratings (AWGs), also known as phased arrays, enable critical (de)-multiplexer and spectrometer functionalities which are increasingly used in photonic integrated circuit (PIC) designs in optical communication [1] and sensing applications [2], [3]. Given the increasing demand for higher data rates and energy efficiency [4], the performance of these PIC components needs to improve as well. In an AWG, part of the signal is fundamentally lost due to the gap between the waveguides in the array. This loss occurs at the gaps where the waveguides, as shown in Fig. 1(a), are attached to the free propagation region (FPR), depicted as “W” in Fig. 1(b). Reducing the size of this gap can reduce the excess loss of the AWG component [5]. The minimum gap size is defined by the resolution limit of the lithography system and the patterning capability of the subsequent process flow.

AWGs fabricated in Silicon photonics platforms have been able to exploit the existing high resolution manufacturing infrastructure of the traditional electronics industry. This advantage has allowed the manufacturing of devices with Argon Fluoride (ArF) 193 nm immersion lithography used for technology nodes as low as 28 nm [6], [7]. It is, however, important to create precision photonic components on InP substrates that enable monolithic integration with lasers and

high efficiency optoelectronic devices. So far, generic InP platforms have been restricted to the use of e-beam, stepper and contact lithography. For the volume production of PICs, stepper lithography is needed, but minimum feature sizes have been limited to 250 nm [8]. This limitation comes from the fact that the shortest wavelength illumination and highest performance imaging have only been available for the latest large Silicon wafer diameters. While 4-inch InP wafers are used for high volume photonic devices and 6-inch are starting to become available, the InP industry has mostly been operating on substrates of 3-inch for high functionality PICs.

In this work, we report for the first time on technical details of the application of ArF deep UV (DUV) lithography for the fabrication of InP-based PICs, continuing our earlier research [9]. An ASML PAS5500 /1100 tool was installed at the NanoLab@TU/e cleanroom in Eindhoven and modified to be, to our knowledge, the only scanner in the world to allow for 100 nm resolution exposures with 15 nm overlay, at high speeds on InP substrates as small as 3-inch. We have developed a process flow that allows us to transfer high resolution features from the photoresist into the semiconductor material. This is a significant advantage, compared to 800 nm minimum feature size and 500 nm overlay error with a formerly used contact lithography.

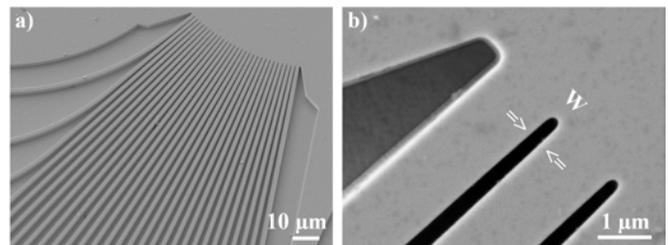


Fig. 1. a) Scanning Electron Microscope photograph of AWG at Free Propagation region, b) Zoomed in on inter-waveguide gap “W”

In the next sections, we describe the impact of wafer flatness on the dimensional control of the inter-waveguide gap in AWGs, as a consequence of the limited depth of focus (DOF) of the ArF lithography process. We present the results of the

This letter was submitted on xxxx, 2018. This research was performed in the NWO Applied and Engineering Sciences Projects: 12861 and 15367, which are funded, by the Dutch Ministry of Economic Affairs.

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improvement of the InP substrate wafer flatness to the level that is required for 100 nm lithography. We compare the simulated effect of the inter-waveguide gap scaling on excess losses of the AWGs to experimental results from fabricated devices. These excess loss measurements are presented by comparing transmission losses to co-fabricated reference waveguides. Finally, we discuss the realization of a 3D-taper inside the gaps resulting from the lag effect.

II. WAFER FLATNESS REQUIREMENTS

For scanner lithography, as with other forms of projection lithography, the minimum critical dimension (CD) that can successfully be printed with below 10% CD uniformity (CDU), can be derived from the Rayleigh criterion [10].

$$CD = k_1 \frac{\lambda}{NA} \quad (1)$$

Equation (1) shows a direct dependency on the exposure wavelength (λ), 193 nm specifically for ArF type excimer laser light sources used in this study. The minimum CD also depends on the numerical aperture (NA) of the lens system installed on the exposure tool and a constant (k_1) representing the applicable lithography processing conditions. The maximum NA of the examined system is 0.75 while the k_1 for the studied process is 0.4. A usable DOF can similarly be derived from the Rayleigh criterion to show a strong dependence on the same hardware defined parameters of wavelength (λ), (NA), and the processing constant (k_2) with a value of 0.9 with the following equation (2).

$$DOF = k_2 \frac{\lambda}{NA^2} \quad (2)$$

The DOF represents the tolerable distance along the optical axis of the lens in which the aerial image of the lithography process remains sharp. From the combination of these two equations, a reduction in minimum CD leads to a quadratic decrease in the DOF. This decrease has direct implications for the requirements with regard to the local flatness of the used wafers.

Although lithography systems are typically equipped with sophisticated leveling systems to correct wafer topography in a global sense, local topography cannot be corrected. From a wafer manufacturing point of view, the local flatness is strongly related to the global flatness of a wafer. Therefore, the detected level sensor range can be used as a figure of merit to measure and compare wafers.

III. WAFER FLATNESS DEPENDENCE

Due to the ever increasing demand for smaller feature sizes in the electronics industry, wafer flatness of large Silicon substrates was gradually improved to meet submicrometer total thickness variation on mass production substrate sizes [11]. In the InP industry, however, this demand has only recently crystallized and lithography methods with relatively large DOF have previously been sufficient. In this section, we highlight the results of the cooperation with a substrate supplier to improve the flatness of InP wafers.

Wafers with several flatness ranges were exposed on the DUV scanner with a 200 nm isolated trench design. All wafers were coated with TOK P6111 photoresist, AZ 1C5D bottom anti-reflective coating, and JSR TCX041 top anti-reflective coating. The layer thickness uniformity of these coatings,

determined at 3 times the standard deviation across the wafer, was measured to be below 1.5, 2.5, and 1.5 nm respectively on ultra-flat DSP silicon wafers, having a negligible effect on the DOF. Conventional illumination conditions were used with a numerical aperture of 0.75 and a sigma setting of 0.366. After post exposure baking, the wafers were developed with Fujifilm OPD5262. The trench widths on at least 600 measurement dies of each wafer were measured using a Hitachi S9200 CDSEM.

Fig. 2 shows CDU, defined as the size distribution of 200 nm trenches at three times the standard deviation for each measured wafer. The CDU data were plotted as a function of the measured global wafer flatness by the level sensor of the exposure tool. In this figure, the CDU values of standard single side polished (SSP) InP wafers are compared to both double side polished (DSP) InP and ultra-flat DSP InP wafers which have undergone an even further improved polishing process. The InP wafers are also compared to ultra-flat DSP Si wafers which represent the flatness benchmark for 3-inch wafers.

Polishing both sides of the InP wafer results in a significant improvement of the overall wafer flatness. This process pushes the measured level sensor range from around 8-12 μm down to a 3-4 μm range. However, this is still not enough to print 200 nm trenches with 10% uniformity over the wafer, resulting in a CDU of around 30 nm. By improving the polishing process, the level sensor range can be reduced even further to around 2 μm with a result of 20 nm CDU on the trenches. This actually comes quite close to ultra-flat Si reference wafers which have below 1 μm range and typical CDU values below 10 nm on these structures. With most recent flatness of DSP InP substrates reaching below 1 μm level sensor range, imaging of even 100 nm features shows adequate CDU results.

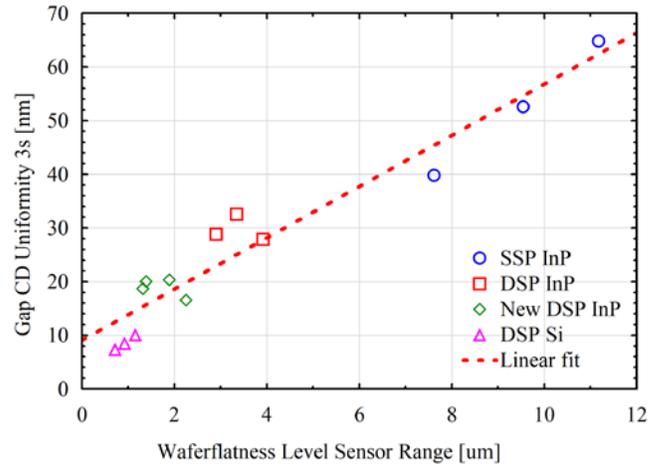


Fig. 2. CD Uniformity of 200 nm inter-waveguide gap as a function of measured level sensor range during exposure of single (SSP) and double side polished (DSP) substrates

IV. AWG GAP SCALING SIMULATIONS

Simulations were performed to quantify the anticipated effect of the inter-waveguide gap scaling. The model used for these simulations is published elsewhere [12]. A cyclic AWG with 8 \times 8 channel design, a channel spacing of 200 GHz and free spectral range (FSR) of 1600 GHz, was simulated. All waveguides were configured to have a width of 1500 nm. Fig. 3

shows the combined TE polarized transmission spectrum of output ports 1 through 8, using port 4 as input for a deeply etched AWG with 100 nm gap size. As can be seen from this figure, the power transmitted per channel deviates in a symmetrical distribution around center channels, with a minimum excess loss of 2.6 dB for the channel at 1550 nm, and an increase of the losses to 3.9 dB at the outermost channels due to diffractive losses in the FPR [5].

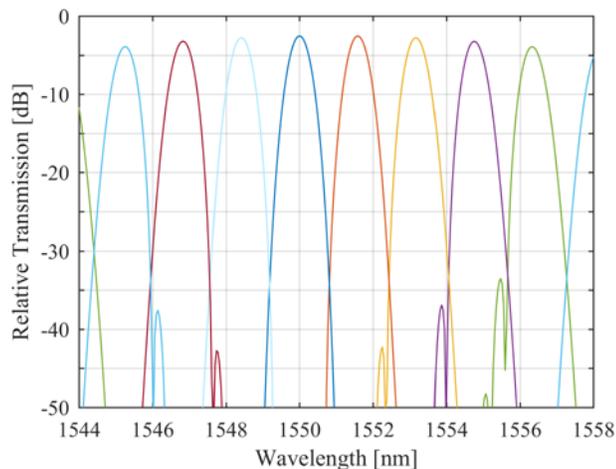


Fig. 3. Simulated AWG transmission spectrum relative to input power from input channel 4 to all output channels with 100 nm gap size

The loss in the star coupler dominates the loss in the AWG. In the above simulation, the array waveguides are assumed to be uncoupled. At small gap sizes however, this simulation overestimates the excess losses because the coupling between the waveguides in the array should be taken into account. A better representation can be obtained by calculating the overlap between the fundamental system mode of a large number of waveguides with a specific inter-waveguide gap, and the fundamental mode of a single wide waveguide matching the combined width. The result of this simulation is shown in Fig. 5, which depicts the simulated coupling loss of two star couplers in the AWG as a function of the inter-waveguide gap size. The excess loss decreases with smaller gap size. The excess loss improves by 1.8 dB by scaling the inter-waveguide gap size from 400 nm down to 100 nm, resulting in an excess loss of around 1.1 dB.

V. AWG FABRICATION AND MEASUREMENT RESULTS

Passive PIC devices were fabricated using a representative generic layer stack with a top cladding of Zn-doped InP material, an intrinsic InP layer, and a waveguide core of InGaAsP material on top of a S-doped InP substrate [8]. These layers were patterned using a double hard mask strategy with the ArF standard resist stack which was also used for the wafer flatness CDU experiments.

The resist pattern was transferred into the hard mask after which this mask was used to pattern the semiconductor material using an inductively coupled plasma etch with a cyclic $\text{CH}_4\text{-H}_2$ alternated by O_2 chemistry [13]. Etching was continued until 300 nm below the waveguiding layer, after which the hard mask was removed. The originally 600 μm thick 3-inch wafers were then ground down to 200 μm thickness, before cleaving the

devices and coating the chip facets with an anti-reflective coating for measurement purposes.

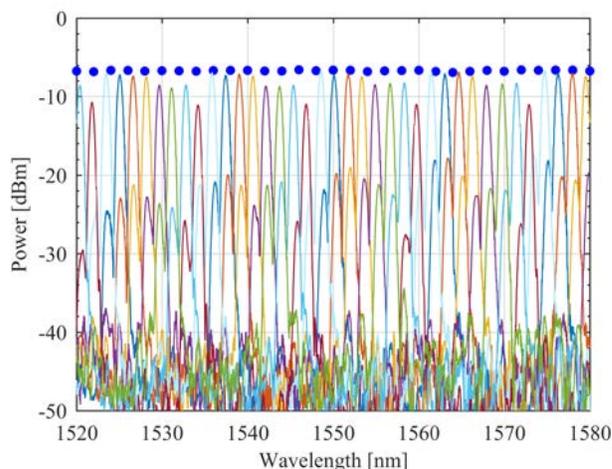


Fig. 4. Measurement results for AWG transmission with 100 nm gap size between 1520 and 1580 nm wavelength, reference signal above in blue dots

The fabricated AWG devices were assessed using an Agilent 81940A tunable laser source via a polarization maintaining lensed fiber. The fiber was coupled into one of the central input waveguides, and the TE polarized transmission spectrum was measured at each of the eight output waveguides through a lensed fiber connecting to an Agilent 81636B power meter. The spectra coming from the AWG output waveguides were compared to those of reference waveguides with similar length and curvature, running along both the inside and outside of the AWG. The combined TE polarized transmission spectrum from an AWG with 100 nm gap size is shown in Fig. 4. The reference signal is plotted in the same figure in blue dots. At this gap size, the power of some channels is almost at the same level as the reference signal. The side-lobes at approximately -20 dB level can be explained by polarization rotation of the circuit [14].

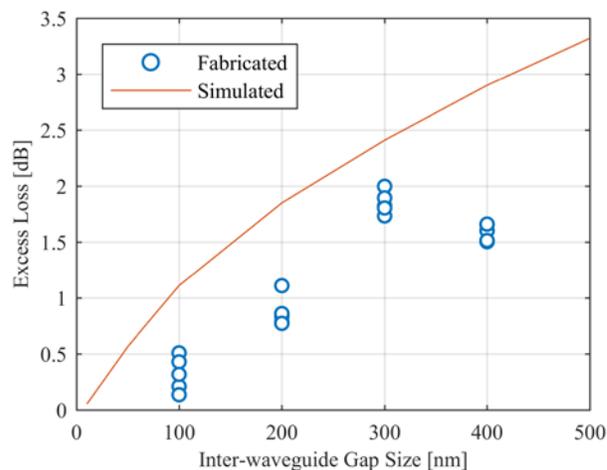


Fig. 5. Simulated and fabricated best channel excess loss for each measured FSR for AWGs with different inter-waveguide gap sizes

The losses were normalized to the maximum reference waveguide signal to represent worst case channel excess losses as opposed to average. The best channels over each FSR were then plotted as a function of designed inter-waveguide gap size in Fig. 5. This figure shows that in accordance with the

simulations, the minimum excess losses decrease with smaller gap size. The 300 nm device performs 0.5 dB worse than expected from the trend of the other measured devices. These increased excess losses may be caused by additional losses on the input waveguide or the coupling of this particular device. The fabricated device with 100 nm inter-waveguide gap size exhibits an ultra-low minimum excess loss of 0.15 dB.

VI. ROLE OF ETCH LAG

One effect that the simulations have not taken into account is that the width of the inter-waveguide gap has an influence on the effective etch depth. Due to the very high aspect ratios, defined as the depth divided by the width of a feature, etch lag occurs [15], [16]. This lag effect is the result of the difficulty to transport reactive species and ions into the trench and reaction products out of the trench. This slows down the physical-chemical process and results in an effective etch rate decrease in the trench when compared to open structures.

The lag effect was determined on multiple fabricated devices using a scanning electron microscope to measure the etch depth on cross-sections for various designed trench widths. Fig. 6 shows the lag effect inside a trench relative to the nominal etch rate on the open structure. As can be concluded from this figure, at 1250 nm trench width, the lag effect is only 12%. At a width of 250 nm however, the effective etch depth is at least 30% less than nominal.

From this trend, it can clearly be expected that when the gap size scales down even further, the lag effect will increase even more as well. On a 100 nm feature, it is therefore expected to have at least 35% lag effect, meaning that the start of the trench will have less than 65% of the etch depth while gradually transitioning to nominal as the waveguides in the array fan out. This creates a 3D taper similar to designed deep-shallow transitions in an AWG [17] which decrease the losses of the component. We suspect the simulated excess losses are worse than some of the fabricated devices because they do not include the effect of the 3D taper.

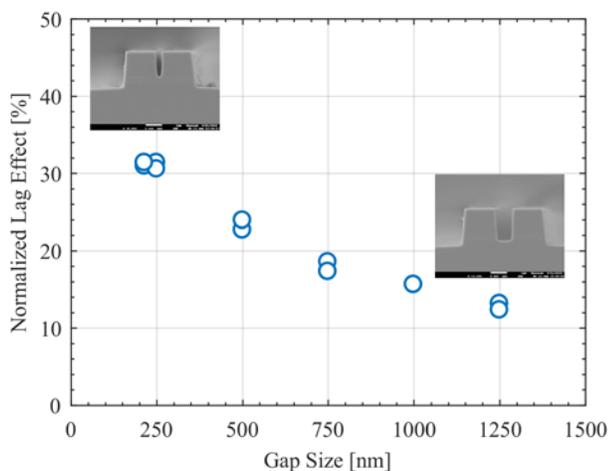


Fig. 6. Lag effect for various inter-waveguide gap sizes

VII. CONCLUSION

Excess loss of arrayed waveguide gratings in InP generic PIC technology can be improved by reducing the inter-waveguide

gap size. A specially configured scanner lithography tool enables 100 nm critical dimensions to be manufactured on 3-inch InP wafers with submicrometer flatness which have only recently started to become commercially available. Arrayed waveguide gratings with sub-dB excess losses as low as 0.15 dB, have been fabricated on InP wafers using DUV lithography. These losses seem to be lower than 2D simulation results, due to the etch lag effect inside the gaps. Using high resolution lithography for InP PIC fabrication is a highly promising scalable solution for the next generation devices.

ACKNOWLEDGMENT

We would like to acknowledge the technical staff of NanoLab@TU/e for numerous helpful discussions and support.

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