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CMOS switched current phase-locked loop

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Indexing terms: Phase-locked loop, Switched current circuits, CMOS integrated circuits

Abstract: The authors present an integrated circuit realisation of a switched current phase-locked loop (PLL) in standard 2.4µm CMOS technology. The centre frequency is tunable to 1MHz at a clock frequency of 5.46MHz. The PLL has a measured maximum phase error of 21 degrees. The chip consumes < 2mW from a 3.3V power supply.

1 Introduction

Phase-locked loops PLLs are important circuits in many aspects of telecommunication [1]. They are often implemented digitally and sometimes using analogue design techniques. Owing to the decreasing dimensions of transistors per chip, the power consumption becomes important. Therefore PLLs nowadays are often implemented in current-mode techniques to reduce the power dissipation and designed to operate from a 3.3V or even lower power supply.

In recent years several circuits have been implemented using switched current (SI) techniques. This technique uses the current as the information carrier in the discrete time domain. SI designs showed performances comparable to their equivalents in other design techniques but with the advantages of occupying less die area, low supply voltages and low power consumption [2-4].

These results prompted the authors to investigate whether it was possible to implement a PLL using SI design techniques. The PLL has an all digital architecture and has been designed in standard 2.4µm CMOS double-poly technology. The supply voltage is 3.3V, while the clock frequency is chosen to be 5.46MHz.

2 Implementation

In general, a first order PLL consists of a phase detector, a loop filter and a voltage controlled oscillator (VCO). In an all digital PLL architecture, as shown in Fig. 1, the phase detector is implemented as an exclusive-OR function, the loop filter is defined by the K-counter and the VCO is determined by the I/D-

counter and the N-divider. This architecture can be used to advantage when SI design is of concern, as we will demonstrate. The general transfer characteristic of a first order all digital PLL can be given as

$$H(s) = \frac{k_v}{s + k_v} \quad k_v = \frac{M f_0 k_d}{k N} \quad (1)$$

Here f_0 defines the centre frequency of the VCO, M and N are some integer values to define intermediate frequencies and k_d the phase detector gain factor. The parameter k defines the total number of steps of the K-counter.

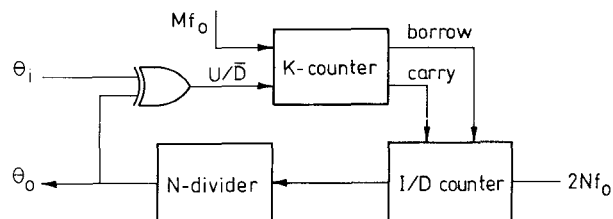


Fig. 1 All digital PLL

The global working of such a PLL is as follows. The K-counter counts up (down) when the output of the phase detector is high (low), with a step equal to

$$\Delta k = M k_d \theta_e \quad (2)$$

where $\theta_e = \theta_i - \theta_o$, the phase error between the input signal and the output signal of the VCO. Without carry/borrow pulses, the I/D counter divides its own input frequency by 2. When a carry pulse is generated, the I/D counter adds a pulse to the output sequence. In case a borrow pulse is generated a pulse is deleted. The output frequency becomes equal to

$$f_{output} = f_0 + \frac{M f_0 k_d \theta_e}{k N} \quad (3)$$

In our design we have chosen $M = N = 20$ in order to supply the K-counter as well as the I/D-counter with the same clock frequency. In Fig. 2 the complete system of the proposed first order PLL is depicted. Here the K-counter is divided into two units, K_{1up} and K_{1down} , each an integrator. In SI techniques integrators can be implemented with high precision [3, 5], resulting in accurate counters. To ensure good phase locking around zero phase error, two separated counters are used, one for the carry signals and one generating the borrow pulses. The disadvantage of this approach is the possible introduction of phase jitter. The maximum number of k is tunable with the current I_{k1} , in order to be able to adapt to other centre frequencies.

The input signal enters the PLL via a flip-flop (the phase detector PD), which ensures that K_{1up} and K_{1down} are presented with the correct input current.

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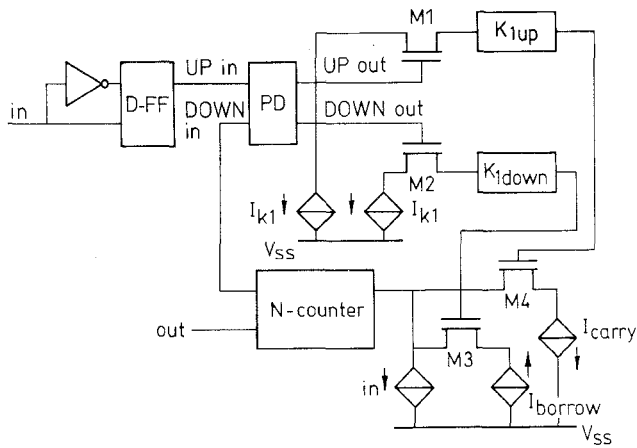


Fig.2 Block diagram of first order SI PLL

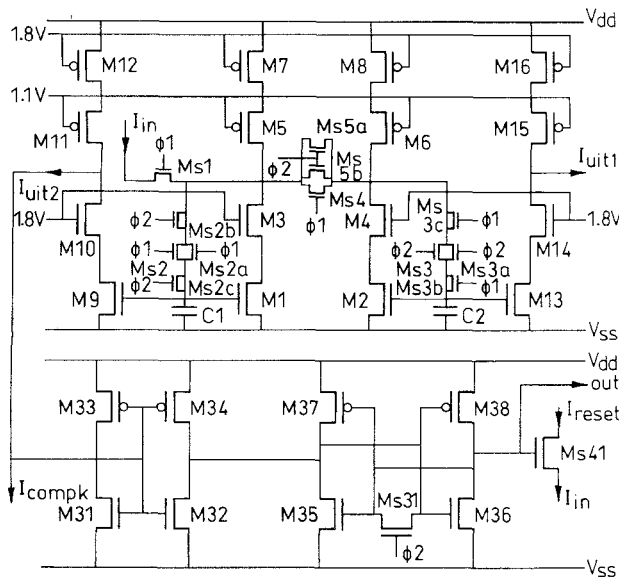


Fig.3 Schematic diagram of K-counter

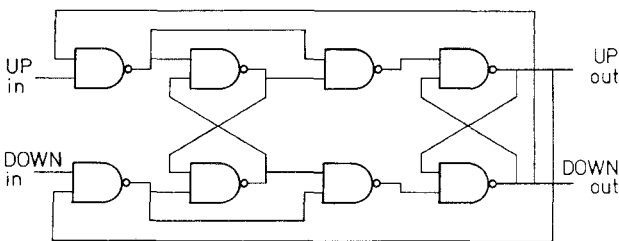


Fig.4 Block diagram of phase detector (PD)

The complementary outputs of PD are connected to K_{1up} and K_{1down} via transistors M1 and M2. Only one of the two counters K_{1up} and K_{1down} is increased during each clock period; the other remains stationary. Two sources I_{k1} are used to keep track of the counter's step size k . For the AM centre frequency of 455kHz, this value is equal to 20, yielding a hold range of ≥ 11 kHz. The reset signals of K_{1up} and K_{1down} are connected to M3 and M4. If these signals are not active (logic 0), the N -counter is provided with current I_N . When the output signal of K_{1up} is active, an extra current I_{carry} is added to the input of N . This I_{carry} is of the same magnitude as I_N , making the input current of the N -counter $2I_N$, advancing the counter by 2 instead of 1. In the same manner the output signal of K_{1down} subtracts I_{borrow} from I_N , making the input current of the N -counter zero. This causes the value of this

counter to remain unchanged. Transistors M3, M4 and the surrounding current sources perform the function of the I/D-counter. The output of the N -counter is fed back to the phase detector, so forming the loop of the PLL. The inverting output of this counter is used as the output of the PLL. Because of the 180 degrees out-of-phase lock (introduced by the phase detector), the input and output signals of the PLL are in phase.

A schematic diagram of one of the two identical K -counters is given in Fig. 3. The upper part of the circuit consists of an integrator, based on two almost identical memory cells. Transistor M1 (M2) is the memory cell transistor, M9 (M13) provides the output current of the integrator and M7 and M12 (M8, M16) are constant current sources. The remaining transistors are switches or cascoding transistors. The lower part of the Figure represents a buffer (M31-M34) and a current comparator (M35-M38, Ms31). Current I_{in} is provided via I_{k1} (Fig. 2) and voltage 'out' controls the gate of M3 or M4 in Fig. 2. The remaining currents are provided by sources (not shown). The capacitors C1 and C2 are designed in double-polytechnology. The N -counter is a K -counter with its output connected to an additional comparator (to provide a 50% duty cycle) and a D flip-flop. Finally, a block diagram of the phase detector PD is shown (Fig. 4), and can be seen as an edge triggered JK-master-slave flip-flop, designed with simple NAND gates.

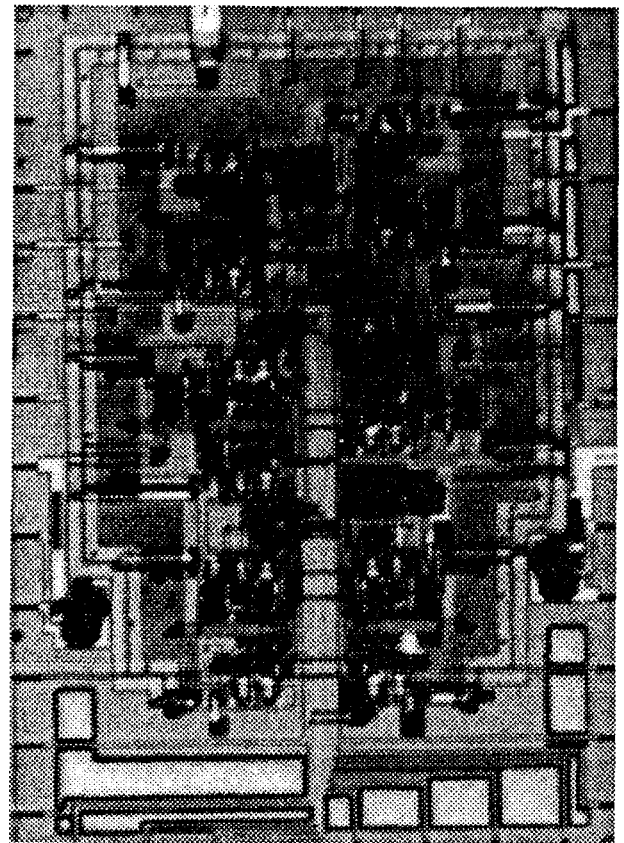


Fig.5 Microphotograph

3 Experimental results

The PLL is designed in a 2.4 μ m CMOS double-poly technology. Fig. 5 is a microphotograph of the prototype, occupying < 3 mm² area and consuming < 2 mW from a 3.3V supply. Measurements were performed at a clock frequency of 5.46 MHz.

Table 1 shows the measured relation between the centre frequency, the hold range and the current I_N with which the VCO can be tuned. One can see that the hold range is approximately at least 10kHz over the complete range of frequencies.

Table 1: Measurements

Centre frequency (kHz)	Hold range (kHz)	Current I_{k1} (μ A)
340	10	0.99
400	20	1.37
500	20	1.85
700	11	1.93
900	9	1.96
1100	9	2.1

Fig. 6 shows the locking behaviour at a frequency of 1MHz. Clearly visible is the phase error, measured to be maximal 21 degrees. The phase jitter is < 20 degrees per period, and is lower at lower frequencies. When using this PLL as a basic circuit for AM detection (for which a second order loop is better) the jitter seems to be too much. Therefore the decision to split up the counter should be reconsidered when AM detection is the target. The designed PLL is able to decode frequency shift keying signals, where jitter is not of importance.

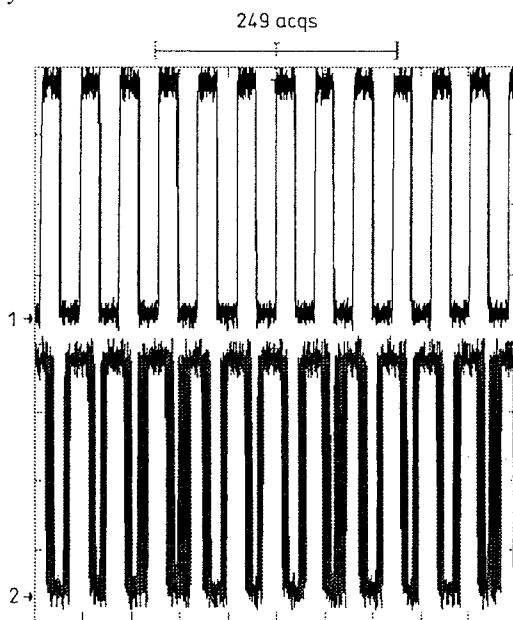


Fig. 6 Locking at 1MHz with input frequency (top) and output frequency (bottom)
Picture taken from PM3394A oscilloscope

For instance, compared to the commercially available 74HC297 PLL, the implemented switched-current PLL has up to five times fewer transistors [6]. Because our

main goal was on the design of the PLL and not in the first place on a compact layout, this difference in number of transistor is not reflected in the smaller die area (see Table 2). For the same supply voltage a lower power consumption is achieved. The prices paid for these advantages are the lower maximum clock frequency and the phase jitter, although this latter aspect can be reduced to a large extent using a single counter.

Table 2: Comparison between SI-PLL and 74HC297

Specification	SI-PLL	74HC297
Technology	2.4 μ m CMOS	3 μ m (high speed) CMOS
Total consumed power at 3.3V, 5.46MHz input frequency, 455kHz output frequency	1.85mW	2.58mW
Estimated max. clock frequency	5.5MHz	38MHz
Number of transistors	250	2322
Chip area	<3mm ²	5mm ²

4 Conclusions

We have shown that it is possible to design a complex circuit such as a PLL with SI techniques. The advantages of doing so are in the compactness of the design, low power consumption and low supply voltage. The designed PLL has an easily tunable centre frequency. For this prototype a robust technology process was used. The authors believe that using a more advanced (submicron) technology, better performances can be obtained (e.g. higher centre frequencies). The design of a second order PLL to improve the loop characteristics is under consideration. This second order loop can simply be obtained by adding an additional first order loop to the system and renders the PLL suitable for AM detection.

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