Plug-In Voltage Dip Compensation Using Mainstream Shunt Grid-Connected Converters

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***Abstract*—Voltage dips may cause adverse effects to connected devices. Series and shunt grid-connected converters have been developed to compensate voltage amplitude variations. However, existing compensation approaches either rely on information of load current or external reactive power reference. In this paper, a voltage dip compensation strategy, which requires local measurements only, is proposed. This approach enables mainstream shunt grid-connected converters, which have no external current sensors, to compensate voltage dips (and swells) in distribution grids. A converter prototype is built and tested to verify the proposed compensation strategy.**

***Keywords*—grid-connected converter, dynamic voltage restorer, voltage dip compensation**

I. INTRODUCTION

Similar to voltage unbalance and harmonics in distribution grid, voltage dips may cause device malfunction to end-users [1, 2]. Voltage dip compensators, also known as dynamic voltage restorers, has been widely adopted to mitigate voltage dips in distribution grids. A common configuration of dynamic voltage restorers is by connecting a converter in series with the grid, as shown in Fig. 1 (a) [3, 4]. Operating as a voltage source, the converter generates voltage difference between the grid voltage and the nominal voltage required by the load. An alternative configuration is by connecting a converter in parallel with the grid [5-8], as shown in Fig. 1 (b). In this case, the converter injects suitable amount of current to the grid based on the level of the voltage dip. This current introduces voltage increment across the line impedance, which is relatively high in a weak grid.

Voltage dip compensation (VDC) based on series connected converter (see Fig. 1 (a)) is a direct approach. However, all load current that flows through one of the winding of the transformer also flows into the converter. This means that the series converter needs to provide at least the same power rating as that of the load, making it a customized solution. Although proven possible [9], series-connected converter generally experiences difficulties to deliver active power to grid.

Alternatively, voltage quality compensation using shunt converters has been receiving growing attentions [5-8]. However, experimental investigation is absent in [7]. In [8],

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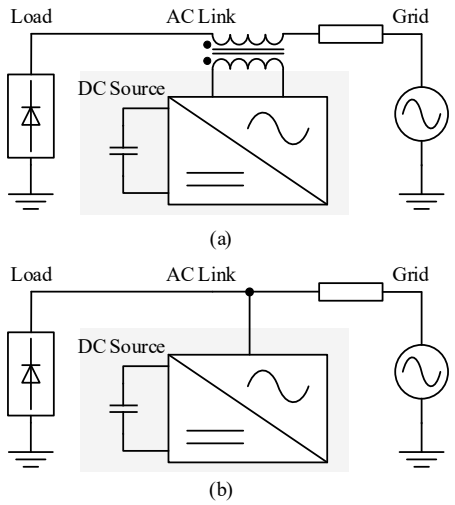


Fig. 1: Configuration of grid-connected converter for voltage dip compensation: (a) series connection, (b) parallel connection.

load information is required to generate a set point for the controller, which makes external sensors necessary. The work in [6] demonstrates that reactive power injection helps to increase voltage fundamental positive-sequence component (PSC) at the point of common coupling (PCC). Unfortunately, no details are given on how to calculate the reactive power reference. A localized strategy is presented in [8] to correct the PCC voltage fundamental PSC. However, consideration to the current rating of the converter is not provided.

This paper presents a localized VDC control strategy for mainstream three-phase grid-connected converters, either of three-phase four-wire configuration or of three-phase three-wire configuration, as shown in Fig. 2. This VDC strategy consists of reactive current generation, fundamental PSC voltage RMS value detection, and reactive current amplitude reference calculation. It decouples VDC control and active power regulation. The diagram of the proposed control strategy is shown in Fig. 3. A synchronous reference frame phase-lock-loop (SRF-PLL) [10-12] is adopted to derive the phase of the fundamental PSC of the PCC voltage. The plug-in voltage dip compensation in the grey box is an add-on to conventional active power regulation of grid-connected converters. In addition, beside voltage dip compensation, the strategy also

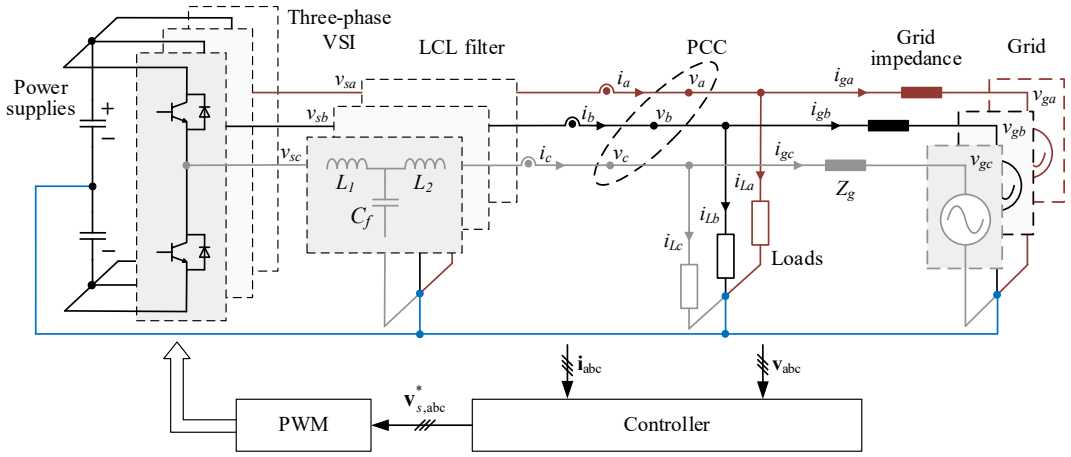


Fig. 2: Diagram of a conventional grid-connected three-phase voltage source converter.

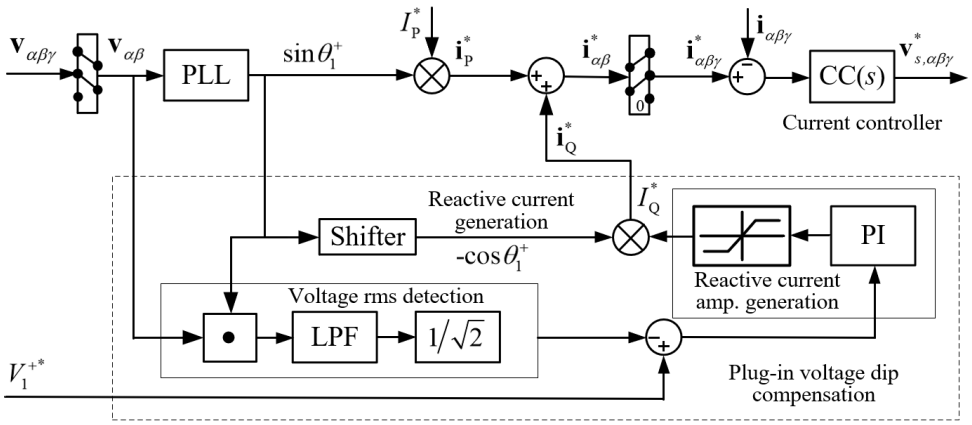


Fig. 3: Diagram of the proposed control architecture for the local voltage-dip compensation.

enables voltage swell compensation for grid-connected converters.

It is experimentally demonstrated that as long as the output current under VDC control is within the limit of the converter, the voltage dip can be eliminated. Given severe voltage dip and voltage swell conditions, which require large output current for complete voltage compensation, the shunt converter still contributes to voltage dip/swell reduction at the PCC.

II. Modelling and Design of Current Loop

In [13], the open-loop mathematic representation of the output current based on PCC voltage and modulation index in a three-phase grid-connected converter is expressed as

$$\mathbf{i}_{\alpha\beta\gamma}(s) = -\mathbf{v}_{\alpha\beta\gamma}(s)\frac{1}{Z_o(s)} + \mathbf{v}^*_{\alpha\beta\gamma}(s)\frac{k(s)H_1(s)}{Z_o(s)} \quad (1)$$

with

$$k(s) = \frac{Z_c(s)}{Z_c(s)+Z_1(s)}, \quad (2)$$

$$Z_o(s) = \frac{Z_c(s)Z_1(s)}{Z_c(s)+Z_1(s)} + Z_2(s), \quad (3)$$

where $\mathbf{i}_{\alpha\beta\gamma}$, $\mathbf{v}_{\alpha\beta\gamma}$, and $\mathbf{v}^*_{\alpha\beta\gamma}$ are the output current, PCC voltage, and modulation index in stationary reference frame. $Z_o(s)$ is the natural output impedance of the converter. It is determined by the LCL filter parameters. Z_1, Z_c and Z_2 are the impedance of the converter side inductor, the filter capacitor, and the grid-side inductor (see Fig. 2). $H_1(s)$ and $k(s)$ are a delay module and a second-order low-pass filter.

Since I_P^* and I_Q^* in Fig. 3 are slow-varying signals compared to the grid harmonic components, the modulation index $\mathbf{v}^*_{\alpha\beta\gamma}(s)$ is written as

$$\mathbf{v}^*_{\alpha\beta\gamma}(s) = \left(-\mathbf{i}_{\alpha\beta\gamma}(s) + \mathbf{i}^*_{\alpha\beta\gamma}(s)\right)CC(s), \quad (4)$$

where $CC(s)$ is the current controller. Substituting (4) into (1), it is found that the GCC system output current and PCC voltage follow

$$\mathbf{i}_{\alpha\beta\gamma}(s) = \mathbf{i}^*_{\alpha\beta\gamma}(s)\frac{CC(s)k(s)H_1(s)}{Z_o(s)+CC(s)k(s)H_1(s)} - \mathbf{v}_{\alpha\beta\gamma}(s)\frac{1}{Z_o(s)+CC(s)k(s)H_1(s)} \quad (5)$$

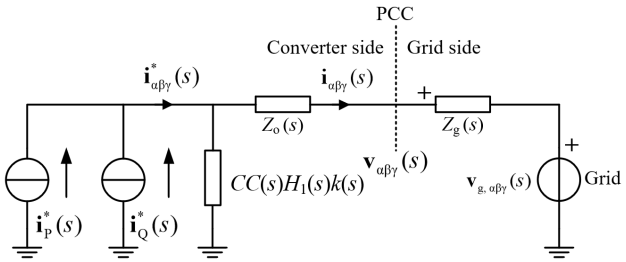


Fig. 4: Circuit diagram showing reactive current injection from the GCC.

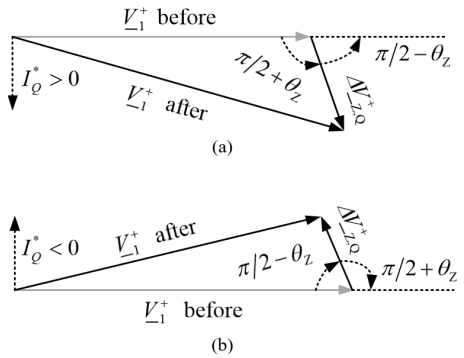


Fig. 5: Phasor diagram of PCC voltage modification: (a) voltage dip compensation (b) voltage swell compensation.

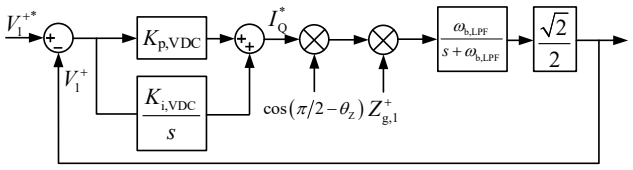


Fig. 6: Linear model of the voltage dip compensation loop.

Table 1: Parameters of current loop controller

Parameter	Symbol	Value
Proportional gain	$K_{p,CC}$	3
Integrator gain	$K_{i,CC}$	120
Resonance filter gain for the nth harmonic component	$K_{res,n}$	2000/n^2
Harmonic orders under compensation	h	3,5,7
Damping factor	ξ	0.001

According to Fig. 3, the current reference of γ component is zero, which removes zero-sequence current injection. Since this paper focuses on regulation of PSCs for PCC voltage dip compensation, only αβ components are discussed in the following.

Equation (5) is represented by an equivalent circuit diagram (see Fig. 4) for the ease of demonstration. The circuit contains a voltage source $V_{g,\alpha\beta}(s)$, two current source i_p^*, i_Q^*,converter output impedance Z_o, and grid line impedance Z_g. The current loop creates a virtual impedance, $CC(s)H_1(s)k(s)$, which is in series with the converter output impedance.

In this paper, the current controller is designed to have high gains at fundamental and low-order grid-harmonic frequencies. The transfer function of $CC(s)$ is expressed as

$$CC(s) = K_{p,CC} + K_{i,CC}\frac{1}{s} + \sum_{n\in h} K_{res,n}\frac{2s}{s^2 + 2\zeta n\omega_1 s + (n\omega_1)^2} \quad (6)$$

where $K_{p,CC}$, $K_{i,CC}$, $K_{res,n}$, h, and ξ are proportional gain, integrator gain, resonance filter gain for the nth harmonic component, harmonic orders under compensation, and damping factor respectively. The parameters of the current controller are summarized in Table 1.

Due to high loop gain at fundamental and some harmonic frequencies, the converter output current is insensitive to grid voltage $\mathbf{v}_{g,\alpha\beta}$, and is mainly determined by the fundamental PSC current reference $\mathbf{i}_P^*$ and $\mathbf{i}_Q^*$.

III. Reactive Power and PCC Voltage

According to [6], reactive power injection increases the fundamental PSC magnitude of PCC voltage. However, calculation of reactive power reference is not provided. In this section, a strategy that flexibly increases and decreases the PCC voltage is presented.

The phasor diagram in Fig. 5 demonstrates the process of PCC voltage modification, which explains the mechanism of voltage dip and swell compensation by reactive power injection. The phasor of the fundamental PSC of the PCC voltage (before compensation, $I_Q^* = 0$) is denoted as $\underline{V}_1^+$.The induced voltage drop on the grid impedance Z_g due to reactive current injection is designated as $\Delta\underline{V}^+_{Z,Q}$. The grid impedance phase angle for the fundamental PSC is referred as θ_Z.

Since an injected reactive current lags the PCC voltage by π/2, when I_Q^*>0, the voltage drop over the grid impedance lags the PCC voltage by π/2-θ$_Z$, as shown in Fig. 5 (a). When I_Q^*<0, it leads the PCC voltage by π/2+θ$_Z$, as shown in Fig. 5 (b). Due to the fact that the grid impedance is mostly inductive for low-order harmonic frequencies [14], the PCC voltage is increased under positive reactive power injection and decreased under negative reactive power injection.

IV. Modelling and Design of Voltage Dip Compensation Loop

With reference to Fig. 4, the PCC voltage fundamental PSC is modelled based on the grid voltage and the reactive current injection by

$$\underbrace{V_1^+ e^{j\theta_{PCC}}}_{\underline{V}_1^+} = \underbrace{V_{g,1}^+ e^{j\theta_g} + Z_{g,1}^+ e^{j\theta_Z} I_p^* e^{j\theta_{PCC}}}_{\underline{V}_1^+(\text{before})} + \underbrace{Z_{g,1}^+ e^{j\theta_Z} I_Q^* e^{j(\theta_{PCC}-\pi/2)}}_{\Delta\underline{V}^+_{Z,Q}} \quad (7)$$

where V_1^+ is the magnitude of the PCC voltage fundamental PSC, and θ_{PCC} is its phase. Above, I_P^*, I_Q^*, and $V_{g,1}^+$ are all amplitudes. After some arrangements, (7) becomes

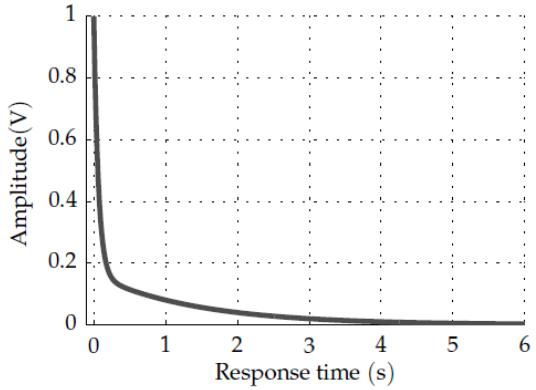


Fig. 7: Close loop step response (from input to error) of the voltage dip compensation.

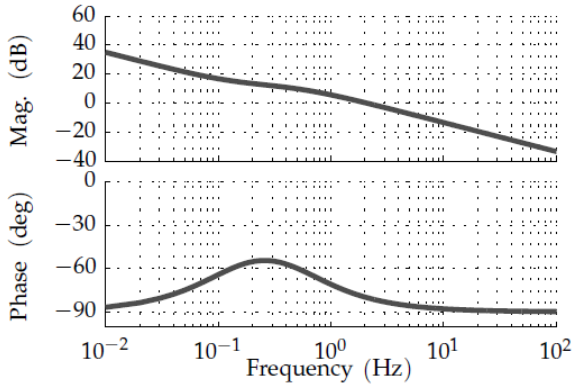


Fig. 8: Bode plot of the voltage dip compensation loop gain $H_{o,VDC}(s)$.

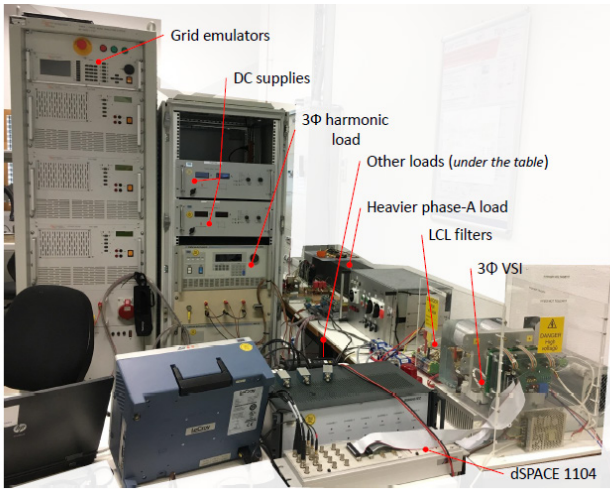


Fig. 9: Photograph of the A three-phase grid-connected converter

$$V_1^+ = V_{g,1}^+ e^{j(\theta_g - \theta_{PCC})} + Z_{g,1}^+ e^{j\theta_Z} I_p^* + Z_{g,1}^+ I_Q^* e^{j(\theta_Z - \pi/2)} \quad (8)$$

Since the induced voltage drop in the grid line impedance is much smaller than the grid voltage, the dynamics introduced from PLL is ignored. Therefore, the voltage dip compensation loop is linearized as shown in the control loop diagram in Fig. 6. According to [14], the grid line impedance for low-order harmonic frequencies lie between resistive and inductive, namely $0 \le \theta_Z \le \pi/2$. For stability analysis of the voltage dip compensation loop, the highest loop gain is considered by assuming $\cos(\pi/2 - \theta_Z) = 1$. The open loop gain of the VDC loop is expressed as

$$H_{o,VDC}(s) = \frac{\sqrt{2}}{2} Z_{g,1}^+ \left(K_{p,VDC} + K_{i,VDC} \frac{1}{s} \right) \frac{\omega_{b,LPF}}{s + \omega_{b,LPF}} \quad (9)$$

with $Z_{g,1}^+ = \omega_1 L_g$, where ω_1 is the grid angular frequency and L_g is the grid inductance.

Table 2: Parameters of voltage dip compensation loop

Parameter	Symbol	Value
Fundamental angular frequency	ω_1	100π rad/s
Bandwidth of VDC loop	$\omega_{b,VDC}$	$\omega_1/25$
Bandwidth of LPF	$\omega_{b,LPF}$	$\omega_1/1000$
Proportional gain	$K_{p,VDC}$	3
Integrator gain	$K_{i,VDC}$	2.5

By selecting the bandwidth of the VDC loop as $\omega_{b,VDC}$, the proportional gain is

$$K_{p,VDC} = \left| \frac{\sqrt{2}}{Z_{g,1}^+ \left(1 + \frac{K_{i,VDC}}{j\omega_{b,VDC}} \right)} \frac{j\omega_{b,VDC} + \omega_{b,LPF}}{\omega_{b,LPF}} \right|, \quad (10)$$

where $\omega_{b,LPF}$ is the bandwidth of the low pass filter (LPF). The integrator gain is chosen in a way that the phase margin of the VDC loop is 100°. Table 2 summarizes the VDC loop control parameters, from which a closed loop step response (from input to error) and the open loop Bode plot are derived as shown in Fig. 7 and Fig. 8 .

V. Experimental Verification

In order to verify the proposed voltage dip compensation strategy, several experimental tests are performed. Fig. 9 shows the grid-connected converter system under test. With reference to Fig. 2, the specifications of the converter system is summarized in Table 3.

Table 3: Specifications of the three-phase grid-connected converter

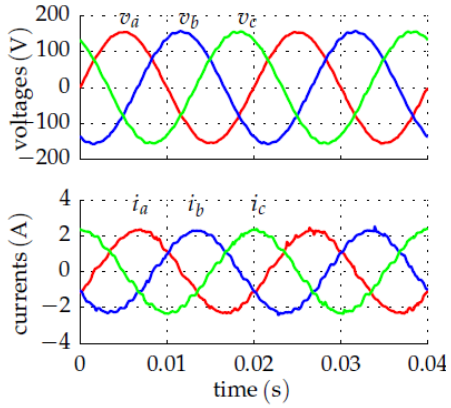
Specification	Symbol	Value
DC power supply	V_{dc}	200 V
Switching frequency	f_{sw}	11 kHz
Gird frequency	f_g	50 Hz
Gird voltage phase-to-neutral	V_g	110 V_{rms}
Converter-side inductor	L_1	3.6 mH (ESR 0.2Ω)
Filter capacitor	f_g	10 μF (ESR 0.2Ω)
Grid-side inductor	L_2	2.0 mH (ESR 0.2Ω)
Grid inductor	L_g	6.0 mH (ESR 0.4Ω)

A. PCC voltage dip/swell compensation

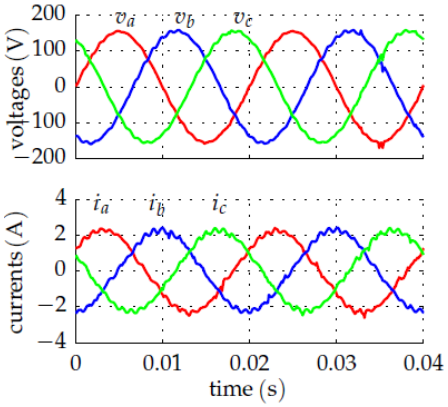
The nominal grid phase-to-neutral voltage is set to be

$$V_1^{+*} = 110 \text{ V}_{rms}. \quad (11)$$

This value is used as the reference for the PCC voltage

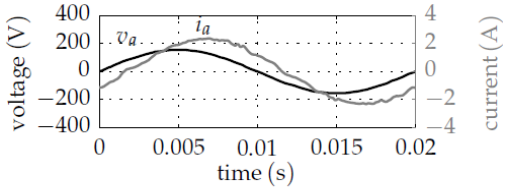


(a) $\eta_g = -1.8\%$

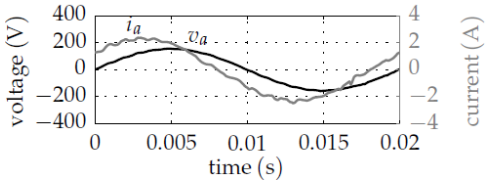


(b) $\eta_g = 1.8\%$

Fig. 10: PCC voltage and converter output current waveforms under voltage dip compensation test: the grid voltage is (a) below the nominal (b) above the nominal.



(a) $\eta_g = -1.8\%$



(b) $\eta_g = 1.8\%$

Fig. 11: PCC voltage and converter output current waveform of phase A under voltage dip compensation test: the grid voltage is (a) below the nominal (b) above the nominal.

fundamental PSC, as shown in Fig. 3. For the ease of description, two indexes,

$$\begin{cases} \eta_{\mathrm{PCC}} = \dfrac{V_1^+}{V_1^{+*}} - 1 \\ \eta_{\mathrm{g}} = \dfrac{V_{g,1}^+}{V_1^{+*}} - 1 \end{cases}, \tag{12}$$

are introduced to quantify the voltage variation level of the PCC voltage and the grid voltage. Above, η_{PCC} denotes the dip level of the PCC voltage, while η_{g} represents the variation level of the grid voltage.

The waveforms of the converter output current and the PCC voltage when the grid voltage amplitude deviates from its nominal value is shown in Fig. 10. The active current reference is set to $I_{\mathrm{P}}^* = 2$ A . In Fig. 10 (a), since the grid voltage magnitude is smaller than the set value, a positive reactive current ($I_{\mathrm{Q}}^* > 0$ in Fig. 5 (a)) is generated. This makes the converter output current lag the PCC voltage, as the waveforms of phase A shown in Fig. 11 (a).

In Fig. 10 (b), a negative reactive current ($I_{\mathrm{Q}}^* < 0$ in Fig. 5 (b)) is generated to compensate the extra grid voltage magnitude. This reactive current creates a voltage drop across the line impendence, which is almost in anti-phase of the grid voltage. In this case, the converter output current leads the PCC voltage (see Fig. 11 (b)). The PCC voltage variation of $\eta_{\mathrm{g}} = -1.8\%$ and $\eta_{\mathrm{g}} = 1.8\%$ can be found in Fig. 12, which shows that in both cases the PCC voltage dip is removed completely.

Fig. 12 shows the experimental results of the PCC voltage dip compensation when the grid voltage is deviated from its nominal value. As shown, the VDC loop removes the PCC voltage dip/swell completely when the grid voltage variation level η_{g} is within [-2.5%, 2.5%]. When the grid voltage deviation exceeds ± 2.5%, the converter still contributes to the PCC voltage support. However, the voltage dip/swell is compensated partially. Due to the limited capacity of the converter system under test, a saturator which limits the reactive current amplitude reference to [-2 A, 2 A] is added as shown in Fig. 3.

B. Dynamic performance

In this section, transient steps are added to the grid voltage and the active current reference to test the dynamic performance of the proposed voltage dip compensation algorithm on a three-phase grid-connected converter.

The experimental waveforms of the converter under grid voltage transient are shown in Fig. 13. The grid voltage steps from 100 V_{rms} to 108 V_{rms} at 0.5 s, which corresponds to the variation of η_{g} from 0% to -1.8%. At the beginning of the transient, the PCC voltage varation index η_{PCC} is negative. Afterwards, the PCC voltage dip is eliminated because of the increased injection of reactive current.

Fig. 14 shows the experimental waveforms of the converter under active current reference transient. The current reference I_{P}^* steps from 2 A to 3 A at 0.5 s. This temporarily increases the PCC voltage, resulting a positive η_{PCC}. With the help of the

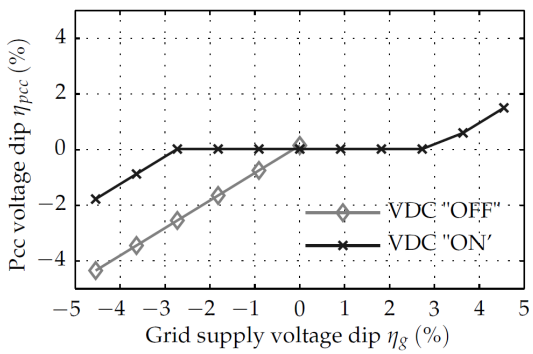


Fig. 12: PCC voltage compensation under a wide range of grid voltage variation.

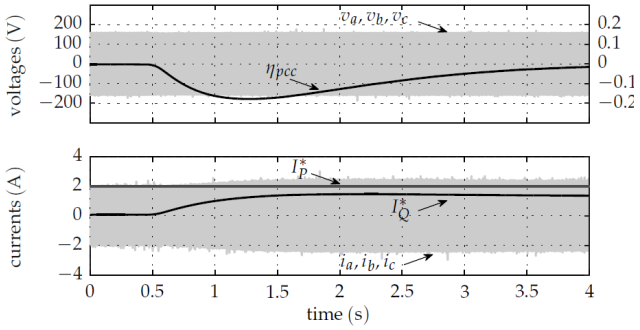


Fig. 13: Dynamic performance of the PCC voltage dip compensation under grid voltage transient (from 110 V to 108 V, i.e., η_g steps from 0 to -1.8%) at 0.5 s.

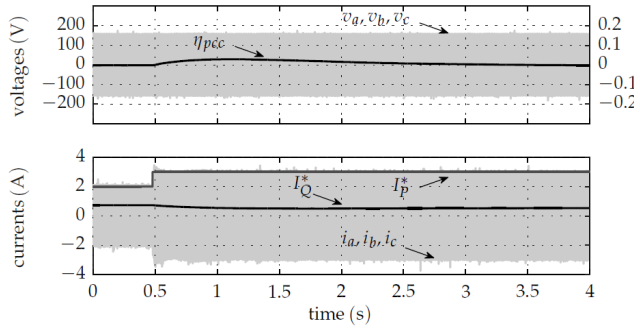


Fig. 14: Dynamic performance of the PCC voltage dip compensation under active current reference transient (from 2 A to 3 A) at 0.5 s.

VDC loop, the reactive current injection is reduced to counteract the increased PCC voltage.

Both in Fig. 13 and Fig. 14, the PCC voltage variation are settled within around 3 s, which is consistent to the analytical result in Fig. 7. Therefore, the proposed VDC algorithm functions well under transient conditions and has a good dynamic performance.

VI. Conclusion

This paper proposes a plug-in voltage dip compensation algorithm for shunt grid-connected converters. The VDC algorithm does not require information on load current. In addition, the VDC loop is decoupled from that of the active power regulation. The reactive current reference is calculated based on the measured PCC voltage, the desired PCC voltage, and the current rating of the converter system.

Experimental tests are carried out to verify the proposed algorithm. When the grid voltage deviates from its nominal value with a certain range, the converter completely corrects the voltage variation. When the grid voltage exceeds that range, the converter output reactive current is saturated by default. Nevertheless, it still contributes to the reduction of PCC voltage dip or swell.

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