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Citation for published version (APA):
Jiao, Y., van der Tol, J., & Williams, K. (2020). InP membrane technology for photonics electronics convergence. In *2020 Opto-Electronics and Communications Conference (OECC)* Article 9273617 Institute of Electrical and Electronics Engineers. https://doi.org/10.1109/OECC48412.2020.9273617

DOI:
10.1109/OECC48412.2020.9273617

Document status and date:
Published: 04/10/2020

Document Version:
Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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InP membrane technology for photonics electronics convergence

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***Abstract*—InP membrane on silicon (IMOS) technology has shown high potential in realizing high-density photonic circuits with speed and energy benefits. Intrinsic active components offered by the InP membrane promise highest optoelectronic efficiencies. It can also be intimately integrated on electronics wafers with ultrashort interconnect lengths, paving a way towards the convergence of photonics and electronics.**

Keywords—Photonic integrated circuit, InP membrane, semiconductor laser, waveguide

I. Introduction

The recent rapid development of photonic integrated circuit (PIC) technologies are attributed to the demand of reductions in size, cost and energy in communication and sensing applications [1, 2]. Driven by these, the complexity of the PICs, in terms of the number of functional components in a single chip, has grown exponentially over the past few decades. The trend can be seen from Fig. 1, which shows the number of functional components per chip over the past years [3]. For conventional PICs where active-passive components are integrated on the InP substrate, the highest integration complexity reported so far is 1700 components per chip in 2014 [4]. Integration method with electronics are typically through chip-scale wire bonding or flip-chip bonding.

However several important applications require much higher integration complexity and more intimate integration with electronics, in order to fulfill the need in functionality and performance. Examples include optical phased array (OPA) for light detection and ranging (LiDAR) [5], dense optical switch matrix [6] and transceivers for intra-chip optical interconnect. New optical waveguide system, with higher optical confinement and free of substrate, is essential to break the integration bottleneck. This can be achieved by photonic integration on a sub-micron thin membrane. On one hand it leads to smaller footprints and bend radii, on the other hand it can be brought much closer to electronics.

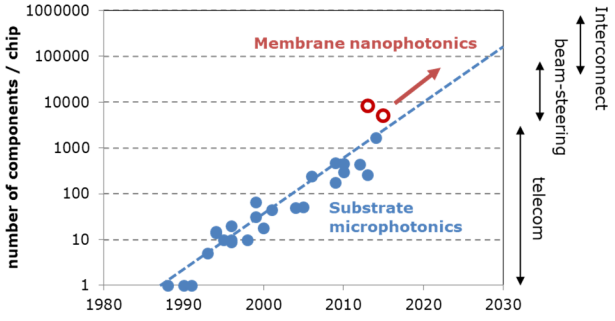

Fig. 1. Development of chip complexity. Data adapted from [3] with additional inputs from [4-6].

Besides the photonic integration on silicon-based membrane [5, 6], where integration of amplifiers is of a challenge, another promising technology is to integrate active-passive components on an InP-based membrane. The InP membrane can later be heterogeneously integrated on to electronics wafers. This is the so-called InP membrane on silicon (IMOS) technology [7, 8]. In this paper we discuss recent development on the IMOS platform.

II. InP Membrane Nanophotonics

One of the advantages of InP membrane photonics is the intrinsic integration of high-performance amplifiers, modulators and detectors with sub-micron sized nanophotonic waveguides. The active-passive integration scheme is shown in Fig. 2 [7]. A 300 nm thin InP membrane acts as the passive waveguiding layer. In areas where actives such as amplifiers are needed, an active layerstack is realized on top of the passive membrane. The active and passive cores are coupled, forming a twin-guide structure. Efficient coupling can be realized by compact taper structures (only 20 µm long).

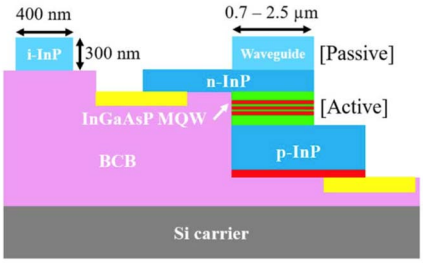

Fig. 2. The active-passive integration scheme in the IMOS platform [7].

Based on the successful demonstration of a membrane twin-guide amplifier [9], various laser circuits can be built by combining the amplifier building block with passive reflectors and filters. Recent demonstrations include distributed feedback (DFB) lasers with 10 mW output to waveguide and over 60 dB side mode suppression ratio (SMSR) and micro-ring-based tunable lasers with tuning range of 25 nm [7].

The membrane enables unique double-sided design and processing. In the recent demonstration of a uni-travelling carrier (UTC) photodiode on IMOS [10], the optical and electrical designs are performed from both sides of the membrane. The electrodes were placed on the backside of the membrane, reducing significantly the series resistance while maintaining the optical loss low. This leads to a device with compact footprint (20 µm^2), high responsivitiy (up to 0.8 A/W) and record-wide electrical bandwidth (90 GHz) among waveguide photodiodes on silicon.

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Novel nano-electro-opto-mechanical systems (NEOMS) have also been demonstrated on IMOS platform, leveraging the naturally high etch selectivity between InP and its ternary and quaternaries. A vertically coupled double membrane NEOMS have been realized (see Fig. 3), showing large phase tuning (4.8 π) from a just 140 µm long device [11]. Besides, realizing NEOMS on the IMOS compatible layerstack opens up future monolithic integration with light sources and readout detectors for sensing. A first demonstration of a NEOMS-based displacement sensor on IMOS extends the vertically coupled double waveguide into a coupled four-waveguide system [12]. Without the need of forming a resonant cavity, the sensor (with on-chip detectors) showed state-of-the-art displacement imprecision with a record-wide optical bandwidth.

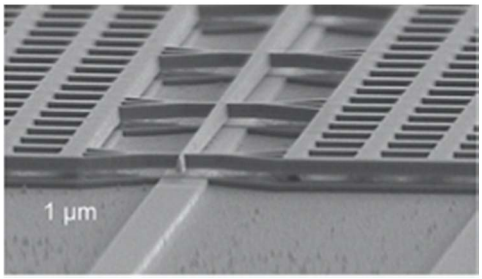

Fig. 3. Picture of the double-waveguide NEOMS on IMOS [11].

III. Electronics Co-integration

The substrate-free nature of the IMOS membrane allow it to be integrated heterogeneously onto electronics at wafer scale. The co-integration scheme is depicted in Fig. 4 [13]. The InP membrane can be wafer-scale bonded onto electronics wafers (such as the complementary metal oxide semiconductor (CMOS) wafers) using benzocyclobutene (BCB) adhesive polymer. The polymer not only provides optical and electrical isolation, but also enables high topology tolerancing, which is crucial for bonding two wafers with devices already manufactured on them. Using this approach, completed wafers from photonics and electronics foundries can be bonded together as a post-processing, relieving the need to alter the original device design or foundry process flow. This ensures minimized impact on device performances and final yield.

The proof of concept has been investigated in the EU project WIPE [14]. The photonics wafers containing optical transceivers, and the electronics wafer containing the drivers are co-designed before submitted to the respective foundry multi-project wafer (MPW) services. Manufactured wafers (3 inch) are aligned and bonded using the BCB adhesive. > 20 µm of the BCB thickness were used to accommodate complex topologies in the two wafers. Alignment accuracy of better than 4 µm can be achieved over the 3-inch wafer scale. Final steps are to open windows through the top InP membrane layer, reveal the contact pads of photonics and electronics, and realize through-polymer via interconnections (see Fig. 5) [15].

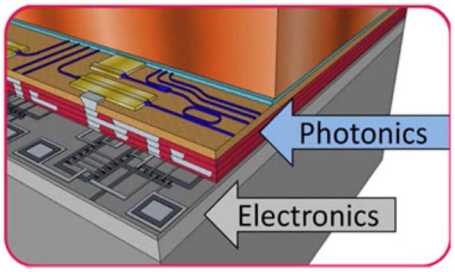

Fig. 4. Artist's impression of the IMOS platform co-integrated with electronics [13].

The demonstration was performed with BiCMOS wafers. However, the nature of IMOS allows it to integrate with a wide variety of electronics, since the post-processing technology is not sensitive to the technology node or the semiconductor materials used in the electronics.

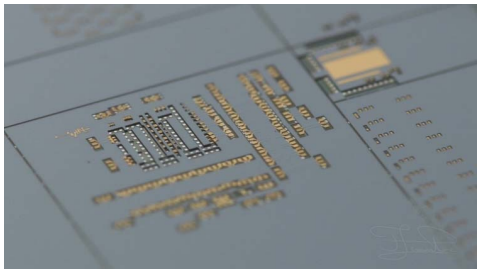

Fig. 5. Picture of a part of the co-integrated wafers, showing InP membrane layer with windows opened to access and interconnect the contact pads of photonics (gold) and electronics (aluminum) [15].

IV. Conclusion

Recent demonstrations of the InP membrane photonics have shown its high potential in breaking the density bottleneck and reaching higher density of tens of thousands per chip and beyond. Its ability to vertically integrate to electronics, without sacrificing device performances or process yield, paves the way towards a powerful co-integrated platform.

Acknowledgment

The authors acknowledge the Dutch NWO Grant Zwaartekracht, the ERC Proof of Concept Grant IMOS4ALL and the EU H2020 project WIPE. The use of the cleanroom facilities at the Nanolab@TU/e is acknowledged.

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