Low-cost and high-speed nanophotonic integrated circuits for access networks

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***Abstract*—Ever-increasing data traffic demands higher-speed and lower-cost photonic integrated circuits (PICs) for the access network. Nanophotonic ICs on a thin membrane provide a promising solution with high density, enhanced speed and reduced assembly cost through co-integration with electronics. We present our recent developments on an InP nanophotonic membrane integrated on silicon.**

Keywords—Photonic integrated circuit, Indium phosphide, membrane, nanophotonics.

I. Introduction

The ever-increasing data traffic from smartphones, video streaming and internet of things (IoT) demands a broadband optical access networks to deliver the contents to the end users. The capacity of the access nodes has increased rapidly over the past years and is expected to expand continuously towards 100G PON [1]. Photonic integrated circuits (PICs) are capable of meeting the data growth by providing a high-speed, mass manufacturable and parallelized solution. Moreover, the system miniaturization that PICs offer is very important for compact pluggable modules used in densely packed user terminals [2]. Previously, a monolithic 8-channel WDM transceiver has been demonstrated on the generic InP technology platform, with in total 320 Gbps data capacity concentrated in a footprint of only 36 mm^2 [3].

The assembly cost is a significant part of the total system costs. Currently the connection of PIC chips to control electronics is mainly through wire-bonding or flip-chip bonding. Both approaches have difficulties in scalability, since they deal with individual chips or dies, and need to be specifically tuned each time for each particular design layout in the chip. The cost and difficulty of the assembly will become unmanageable as the PIC density and complexity evolves [4]. A route to lower assembly cost while maintaining high scalability is desired.

In this paper, a PIC technology platform based on an InP photonic Membrane On Silicon (IMOS) is introduced. The InP membrane promises both high optical confinement, for density and complexity benefits, and intrinsically high optoelectronic efficiencies, for speed and full photonic functionality [5]. Recent developments in the IMOS platform as well as future perspective will be discussed.

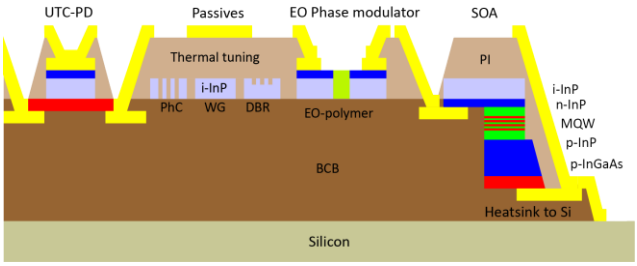

Fig. 1. Cross-sectional view of the InP membrane on silicon (IMOS) platform.

II. InP Photonic Membrane

A cross-sectional schematic illustration of the IMOS platform is depicted in Fig. 1. The InP substrate is removed from the photonic circuits and instead the entire photonic membrane layer is bonded onto a silicon carrier with a polymer-based low-index optical buffer. In this way the optical confinement of the waveguides is significantly enhanced, resulting in sub-micron waveguide dimensions (400 nm × 300 nm). A benefit of the high optical confinement is that ultra-sharp bends (R < 1 µm [6]) and compact waveguide routings can be realized for complex multi-channel systems on chip, supported by low propagation loss, down to the 1 dB/cm level [7].

The InP material system, used for the photonic membrane, also supports intrinsic and high-performance amplification and lasing. Semiconductor optical amplifiers (SOAs) have been

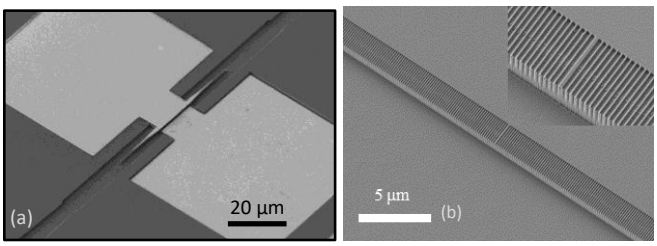

Fig. 2. Electron microscope pictures of (a) a fabricated SOA on IMOS and (b) a fabricated DFB laser cavity on IMOS.

demonstrated on the sub-micron waveguides, with gains up to 110 cm^{-1} [8]. The SOA is directly integrated in the membrane (see Fig. 1) and therefore does not require aligned die bonding and long spot size conversion [9], as in III-V-Si hybrid solutions. A fabricated SOA on IMOS is shown in Fig. 2a). Based on this SOA building block, various lasers can be constructed, using the active-passive integration scheme shown in Fig. 1. Demonstrated lasers include a micro-ring laser, tunable over 25 nm, and a single-mode DFB laser with >60 dB SMSR [10]. The fabricated high SMSR DFB laser is shown in Fig. 2(b), with uniform distributed Bragg gratings defined on top of the SOA.

The miniaturization and absence of the substrate in IMOS also enable ultra-fast optoelectronic devices. An example is a uni-travelling carrier (UTC) photodiode with electrical bandwidth beyond 67 GHz (instrument limited) [11]. Miniaturization results in an ultra-compact footprint of only 3 × 10 μm^2, while maintaining a high optical efficiency of 0.7 A/W. The removal of the substrate significantly reduces the parasitics and results in a low capacitance of a few fF.

III. Towards Photonic Electronic Co-integration

The IMOS platform can enable high-density and high-speed photonic circuits in a thin membrane, ideal for the PIC scalability demands for access networks. On the other hand, the membrane configuration also potentially enables wafer-scale vertical stacking to electronics. The silicon carrier in Fig. 1 can be replaced by CMOS containing electronics. The polymer bonding layer is highly flexible and can combine two processed wafers with complex material systems [12]. Interconnection with through-polymer vias can be realized to connect PICs with drivers in unprecedentedly short lengths and with low parasitics.

The first steps have been carried out in IMOS towards this co-integration. The membrane is being bonded, patterned and processed on a full wafer scale. Through-polymer vias have been realized as well, connecting lasers to the silicon carrier as illustrated in Fig. 1. The vias are designed in this case for thermal management purposes and can be optimized further for high-speed interconnections. A fabricated IMOS wafer (2-inch InP membrane bonded on 3-inch silicon carrier) is shown in Fig. 3 [10]. SOAs, lasers and other active-passive integrated circuits have been designed and realized on this wafer. The through-polymer vias have also been realized over locations across the entire wafer.

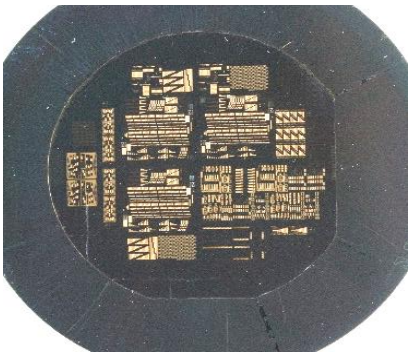

Fig. 3. A fabricated IMOS wafer containing SOAs, lasers and other active-passive integrated circuits.

IV. Conclusion

In this paper the concept of an InP photonic membrane platform on silicon, IMOS, was introduced. The platform features high density and high speed properties, which are well suited for the performance and scalability needs in the future optical access networks. Its potential vertical co-integration with electronics also opens up a route to significant cost reduction and mass manufacturing of assembling and packaging.

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