A Compact Fully Dynamic Capacitance-to-Digital Converter with Energy-Efficient Charge Reuse

A Compact Fully Dynamic Capacitance-to-Digital Converter With Energy-Efficient Charge Reuse

Haoming Xin, *Member, IEEE*, Kevin Pelzers, Peter Baltus, *Senior Member, IEEE*, Eugenio Cantatore, *Fellow, IEEE*, and Pieter Harpe, *Senior Member, IEEE*

***Abstract*—An ultra-low-power fully dynamic capacitance-to-digital converter (CDC) that exploits a novel charge reuse technique is proposed. The CDC includes a capacitive bridge as the sensing frontend and an asynchronous successive approximation register ADC for signal digitization. Passive charge sharing between the frontend and ADC is used to enable a fully dynamic operation. Instead of resetting the capacitive bridge (with large sensing and reference capacitors) for each measurement, the charge is maintained and reused over many measurements to save energy. A power-gating technique is employed to reduce the stand-by power. As a result, a figure of merit as low as 4.3 fJ/conv-step is achieved for the CDC, which is >3× better than the state of the art. Furthermore, it supports an inherent scaling of power versus speed with a minimum power of only 44 pW and a compact chip area of 6440 μm^2.**

***Index Terms*—Capacitance-to-digital converter (CDC), charge reuse, dynamic, Internet of Things (IoT), power gating.**

I. Introduction

Emerging miniaturized Internet-of-Things (IoT) sensor nodes require on-demand sensing with nW-level power consumption due to the scarce energy available. Furthermore, the sensing circuits should ideally be able to adapt their performance (speed and resolution) efficiently over a wide range, such that different applications and scenarios can be supported. Capacitive sensors are commonly used to measure many different parameters (pressure, sound, etc.), thus an ultra-low-power capacitance-to-digital converter (CDC) able to keep energy efficiency while scaling performance is needed. State-of-the-art CDCs [1], [2] can achieve a figure of merit (FoM) down to 16 fJ/conv-step, yet their power consumption is in μW-range, and have not shown efficient scalability over a broad performance span. An all-dynamic nW-level CDC with inherent power scaling with speed and resolution and an FoM down to 18 fJ/conv-step was proposed in [3]. However, the major bottleneck for the energy consumption of previous CDCs is the energy required to charge the large sensing and reference capacitors.

To address this issue, an all-dynamic CDC which includes a capacitive bridge and an asynchronous successive approximation register (SAR) ADC with a novel charge reuse technique is proposed. Instead of the traditional approach where the bridge (with large sensing and reference capacitors) is reset before each measurement, here the charge is preserved and reused over many measurements to save energy. With this approach, the energy consumed by the capacitive bridge is greatly reduced, thereby allowing the FoM of the CDC to approach the FoM of a SAR ADC. Moreover, a compact SAR ADC with unit-length digital-to-analog (DAC) capacitors [4] is used to reduce the number of capacitors and the value of the unit capacitor. Furthermore, an automatic power-gating technique [5] is exploited to minimize the leakage power of the all-dynamic CDC. This letter is an extended version of [6], and it is organized as follows: the proposed CDC is introduced in Section II, the measurement results are presented in Section III, and conclusions are drawn in Section IV.

Manuscript received August 15, 2020; revised October 24, 2020; accepted November 1, 2020. Date of publication November 5, 2020; date of current version December 1, 2020. This article was approved by Associate Editor Makoto Takamiya. This work was supported by the European Union's Horizon 2020 Research and Innovation Programme under Grant 665347. *(Corresponding author: Haoming Xin.)*

The authors are with the Integrated Circuit Group, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands (e-mail: h.xin@tue.nl).

Digital Object Identifier 10.1109/LSSC.2020.3036223

II. Proposed CDC With Charge Reuse

A. Principle of Charge Reuse in Capacitive Bridge

The proposed CDC includes a capacitive bridge and an asynchronous SAR ADC, and it has three operation phases (reset, sample, and AD conversion), as shown in Fig. 1(a) and (b). The capacitive bridge includes an off-chip sensing capacitor (C_s), an on-chip reference capacitor (C_r), and several switches to enable the three operation phases. C_p represents the parasitic capacitance of the interconnection between C_s and the CDC. The bridge output is directly sampled on the ADC DAC capacitors (C_{DAC}) through passive charge sharing to enable low-power fully dynamic operation [3]. Note that only a single-ended circuit that includes the bridge, the aggregated DAC capacitance (C_{DAC}), and the sampling switch of the SAR ADC, is shown for simplicity.

At the beginning of measurement 1, all capacitors are reset to the ground. Then, in the sample phase, the top and bottom nodes of the capacitive bridge are connected to VDD and VSS, respectively. According to the calculations shown in Fig. 1(b), a C_s-dependent output voltage V_s is then established on C_{DAC}. Even though this $C_s - V_s$ transfer function is inherently nonlinear, it is entirely predictable, thus it can be reversed in the digital domain [3]. Then, the SAR ADC digitizes the sampled V_s asynchronously and produces the digital output after a conversion delay. In the meantime, the bridge switches are off to keep the bridge capacitors floating. In this way, the charge that was previously stored in the bridge capacitors (C_r, C_s, and C_p) during the sample phase can be preserved. Furthermore, the DAC capacitors are automatically reset to the state before conversion after the AD conversion is finished. Thus, the charge that was stored in C_{DAC} is also preserved. Since the charge in all the associated capacitors is preserved, it can be reused by subsequent measurements (2 to N) to save energy. Instead of resetting the capacitors to ground before the sample phase [3] (which would require recharging of the capacitors), in the measurements with charge reuse, the reset phase is skipped and the measurements start from the previously charged state, as shown in the timing diagram of Fig. 1(a). By doing this, the capacitive bridge only needs to be fully charged once every N measurements, which significantly reduces the average bridge energy consumption. Note that the measurements without reset provide an identical output as compared to measurements with reset, even when C_s changes dynamically. For example, at the sample phase of measurement 2 [Fig. 1(c)], if C_s is increased (or decreased) by ΔC compared to the C_s value in measurement 1, an amount of charge ΔQ will be provided from (or dumped back to) the supply/decoupling capacitor. According to the calculations shown in Fig. 1(c), the output voltage without reset $V_{s,\mathrm{new}}$ exactly matches with the $C_s - V_s$ transfer function with reset.

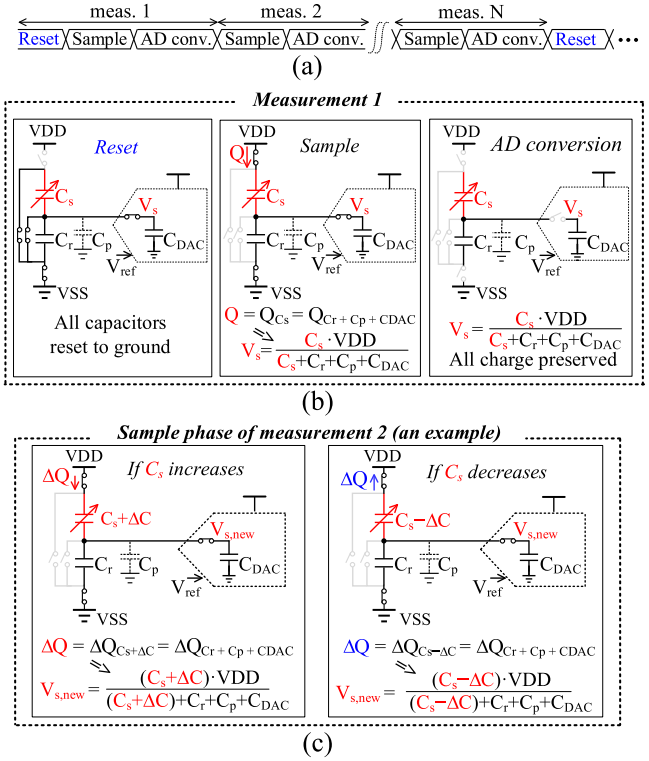

Fig. 1. (a) Overall timing diagram. (b) Illustration of the three operation phases of the CDC. (c) Example sample phase without a reset phase.

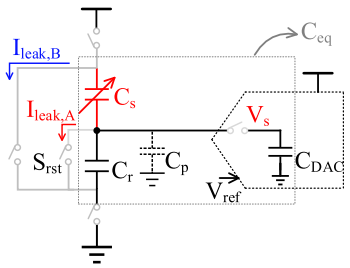

Fig. 2. Charge leakage during charge preservation.

B. Leakage in the Capacitive Bridge

Theoretically, an infinite number of measurements without reset can be performed after measurement 1. However, due to the leakage of the bridge switches, the preserved charge will slowly decline in time. As shown in Fig. 2, the current that leaks out of the middle point of the bridge ($I_{\text{leak},A}$) will cause errors in measurements with charge reuse. Taking measurement 2 as an example, the error introduced in the bridge output voltage due to $I_{\text{leak},A}$ can be calculated as

$$V_{\text{error}} = \frac{\int_0^{\Delta T} I_{\text{leak},A}(t)dt}{C_{s,\text{new}} + C_r + C_p + C_{\text{DAC}}} \tag{1}$$

where ΔT is the time difference between the sample phase of measurements 1 and 2, and $C_{s,\text{new}}$ is the sensing capacitance value at the sample phase of measurement 2. Moreover, this error will accumulate in the measurements afterward. Thus, only a limited number $(N-1)$ of measurements without reset can be performed with a certain accuracy (e.g., error $<0.5V_{\text{LSB}}$ of the ADC). After this, a measurement with a reset phase should be performed to remove the accumulated error caused by leakage, and then, a set of $N-1$ measurements can be performed again without reset.

In order to save more energy by means of charge reuse, V_{error} should be minimized, such that N can be maximized. According to (1), increasing the value of C_r and C_{DAC} could help to reduce V_{error}. However, a C_r value that is close to C_s should be used to maximize the bridge sensitivity [3], and C_{DAC} should actually be minimized to reduce the signal attenuation caused by the passive charge sharing between the bridge and ADC [3]. Thus, it is better to reduce $I_{\text{leak},A}$. To achieve this, V_s should be kept as low as possible (to minimize the voltage drop over the reset switch S_{rst}), and the off-state impedance of S_{rst} should be maximized. Note that the current that leaks from the top of the bridge ($I_{\text{leak},B}$) does not cause measurement errors. However, the lost charge because of $I_{\text{leak},B}$ needs to be refilled in the next measurement, which consumes energy. Thus, $I_{\text{leak},B}$ should also be minimized.

C. Bridge Energy Consumption With Charge Reuse

Energy saving is the major advantage of the charge reuse technique. It is clear that the bridge with charge reuse only needs to be fully charged once over many measurements if C_s is a fixed value. As will be discussed in this section, actually this conclusion still holds even if C_s changes dynamically. For measurement 1 with a reset phase, the energy drawn from the supply to charge the capacitive bridge from ground to VDD can be calculated as $E_{b,1} = C_{eq,1} \cdot VDD^2$, where $C_{eq,1}$ is the equivalent capacitance of the bridge to ground (Fig. 2) for measurement 1. Then, in measurement 2, the equivalent capacitance will change from $C_{eq,1}$ to $C_{eq,2}$ due to the change of C_s, and the bridge will not be reset to the ground but starts from the previously stored state to save energy. Depending on whether $C_{eq,2}$ is larger than $C_{eq,1}$ or not, an extra amount of charge ΔQ will be provided from or dumped back to the supply/decoupling capacitor in the sample phase of measurement 2, as mentioned previously. Thus, the energy "consumed" to charge the bridge in this case becomes: $E_{b,2} = \Delta Q \cdot VDD = (C_{eq,2} - C_{eq,1}) \cdot VDD^2$. For the case when $C_{eq,2} > C_{eq,1}$ (C_s increases), an extra amount of energy will be consumed to charge the increased C_{eq}. While for the case when $C_{eq,2} < C_{eq,1}$ (C_s decreases), $E_{b,2}$ is a negative number, which means the capacitive bridge actually gives energy back to the supply in this case. The calculation of $E_{b,2}$ is valid for all the measurements afterward with charge reuse. Assuming there are $N-1$ measurements (measurement 2 to N) without reset, the bridge energy consumption at the ith measurement ($i \in [2, N]$) can be calculated as $E_{b,i} = (C_{eq,i} - C_{eq,i-1}) \cdot VDD^2$. Here, the leakage current of the bridge is assumed to be negligible, and $C_{eq,i}$ is the equivalent capacitance of the bridge at the ith measurement. Therefore, the total energy drawn from the supply to charge the bridge for these N measurements can be calculated as

$$E_{b,\text{total}} = \sum_{i=1}^{N} E_{b,i} = C_{eq,N} \cdot VDD^2. \tag{2}$$

According to (2), $E_{b,\text{total}}$ is equal to the energy consumed to charge $C_{eq,N}$ from ground to VDD only once. Therefore, the average bridge energy consumption per measurement is reduced by N times, even if C_s changes dynamically.

D. CDC Architecture and Capacitive Bridge Implementation

Fig. 3 shows the CDC architecture and the operation waveforms. The bridge and ADC use the same supply (VDD = 0.6 V) to achieve a ratiometric measurement. A 1-V VDDH is used for the clock drivers and the ADC power-gating logic. The capacitive bridge includes a sensing and a reference arm, which produce a C_s-dependent voltage V_s and a reference voltage V_{ref} to the differential SAR ADC, respectively. The target sensing range of this prototype is from 0 to 6 pF, and the value of C_{r1} is chosen to be 5 pF. In this case, V_s will vary from 0 V to about 300 mV for the target sensing range [Fig. 4(a)]. This relatively low V_s helps to reduce $I_{\text{leak},A}$, which leads to smaller V_{error}

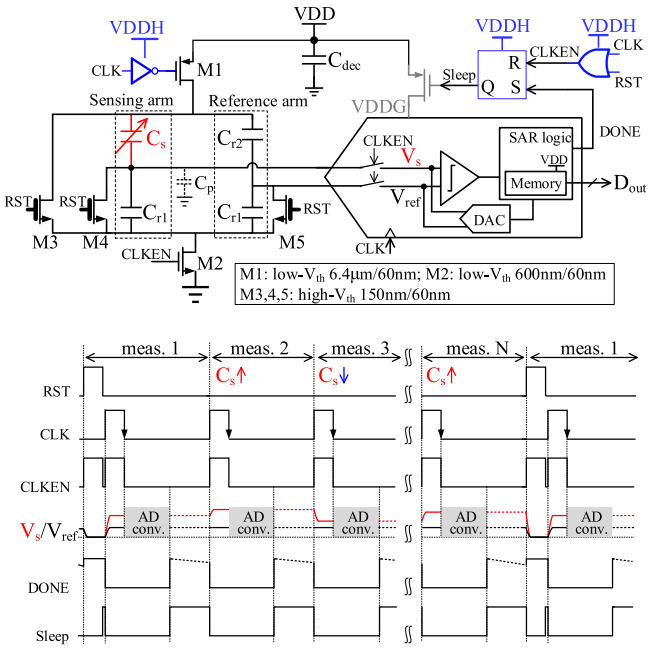

Fig. 3. Architecture and operation waveforms of the proposed CDC.

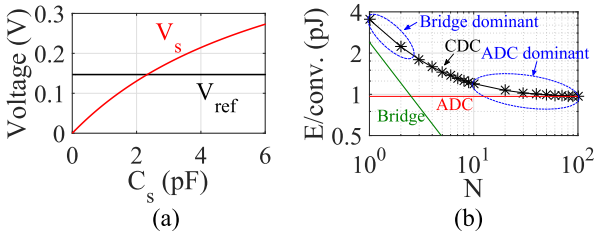

Fig. 4. (a) Calculated bridge output voltages (C_p = 1.5 pF and C_{DAC} = 512 fF) and (b) CDC energy per conversion versus N (with largest C_s, and at maximum operation rate), based on simulation and calculation.

according to (1). The value of C_{r2} is chosen to be 1.8 pF, which produces a V_{ref} of about 150 mV. To further reduce $I_{leak,A}$ (and $I_{leak,B}$), small high-V_{th} nMOS transistors (W/L = 150 nm/60 nm) are used as the reset switches. The on resistance of these small reset switches is still sufficiently low thanks to the 1-V clock drivers. According to simulations at room temperature, the errors (due to reset switches' leakage) in the differential output ($V_s - V_{ref}$) after 1 ms of charge preservation are within 140 μV for the target C_s values, which is $< 0.5V_{LSB}$ ($\approx$ 150 μV) of the ADC. Since the conversion time of the CDC is only 10 μs, one reset pulse would be enough for $N = 100$ measurements, keeping the errors caused by leakage below 0.5 LSB. Note that the ESD protection diodes in the I/O pad that connects to C_s also introduce leakage. By using customized ESD protection diodes with a relatively small size, the errors due to this leakage are not significant (as will be verified in measurements). Fig. 4(b) shows the energy per conversion of the CDC at different values of N: the bridge energy becomes negligible when $N \geq 10$. Therefore, even with a tenfold increase in $I_{leak,A}$ (e.g., due to higher temperature and/or larger ESD diodes), a similar energy reduction can still be achieved.

E. SAR ADC With Automatic Power Gating

A 10-b asynchronous SAR ADC with unit-length DAC capacitors [4] is used in this CDC. Thanks to the unit-length capacitors, the total core DAC capacitance is only 128 fF (with 128-fF parasitic capacitance). A 256-fF attenuation capacitor is added to the

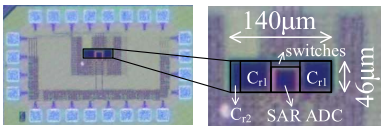

Fig. 5. Die photograph of the CDC in 65-nm CMOS.

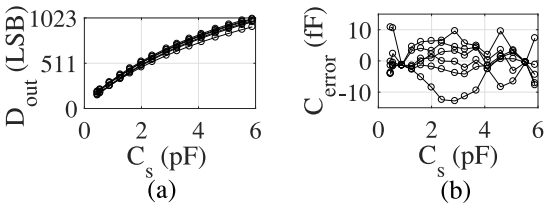

Fig. 6. (a) Measured CDC output code versus C_s for six IC samples (the CDC also supports C_s < 0.458 pF, but measurements are limited by the trimming capacitor's range) and (b) measured error versus C_s for six IC samples after calibration.

DAC array, such that the input range of the ADC is reduced to about 300 mV ($\approx$ bridge output range) for a 0.6-V VDD, while the ADC sensitivity is increased by a factor of two [3]. As a result, the total capacitance in the DAC array (C_{DAC}) becomes 512 fF. As this is $>10\times$ smaller than the equivalent capacitance seen from the bridge, passive charge sharing between the bridge and ADC gives less than 1 dB of signal attenuation. As the common-mode voltage of the bridge output is relatively low [Fig. 4(a)], an ADC comparator with pMOS input transistors is used. Furthermore, the SAR ADC (except for the memory cells) is automatically power gated [5] after the conversion is finished (Fig. 3) to minimize the leakage power of the CDC.

III. Measurement Results

Thanks to the simple architecture and compact ADC [4], a chip area of only 6440 μm^2 is achieved in 65-nm CMOS (Fig. 5). An external trimming capacitor is used to characterize the CDC, and the total C_p is estimated to be about 1.5 pF in the measurements. First, the CDC is characterized without charge reuse. The CDC supports a sensing range from 0.458 to 5.886 pF [Fig. 6(a)]. After a two-point calibration and systematic nonlinearity correction, the measurement error stays between -13 and 11 fF over the whole measurement range, for six ICs [Fig. 6(b)]. As the measurements are performed without charge reuse, the errors shown in Fig. 6(b) do not include bridge leakage errors, but are mainly caused by ADC nonlinearity.

When enabling charge reuse, the reset pulses are given at 1.25 kHz, while the CDC operates at 100 kS/s. Thus, 1 measurement with reset ($i = 1$) is followed by 79 measurements (i from 2 to 80) without reset, which form a measurement group. 2^{17} measurements in total are performed with a fixed C_s value, which leads to 1638 measurement groups. By averaging the 1638 outputs for each measurement index i, an averaged digital output for each measurement index is obtained. Then, the errors caused by bridge leakage can be calculated by comparing these averaged outputs to the averaged output when $i = 1$. Measured at room temperature, the errors due to bridge leakage for 15 different C_s values (0.458 to 5.886 pF) over all 80 measurement indexes are all within $\pm$0.5 LSB [Fig. 7(a)]. The same measurement has been done for another five IC samples, and the maximum errors due to bridge leakage (over 80 measurements and 15 different C_s values) for these ICs are similar [Fig. 7(b)].

Due to the inherent nonlinear $V_s - C_s$ transfer function, the rms noise of the CDC increases with C_s from about 4 fF_{rms} to about 12 fF_{rms} [Fig. 7(c)], and the noise when enabling charge reuse is similar to the case without charge reuse. The averaged rms noise [3] over the entire sensing range is 7 fF_{rms} and 7.3 fF_{rms} for the case

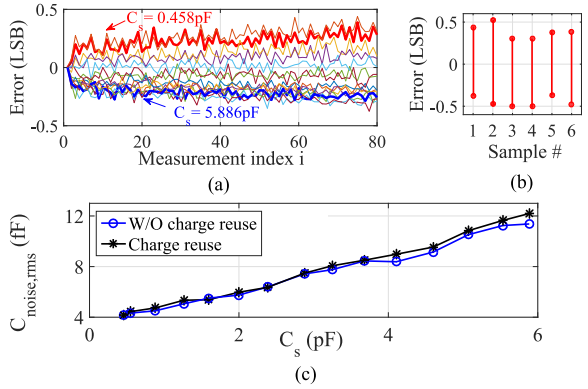

Fig. 7. (a) Measured errors due to bridge leakage over 80 measurement indexes (reset is only applied for $i = 1$), (b) measured maximum errors due to bridge leakage for six ICs, and (c) measured rms noise versus C_s.

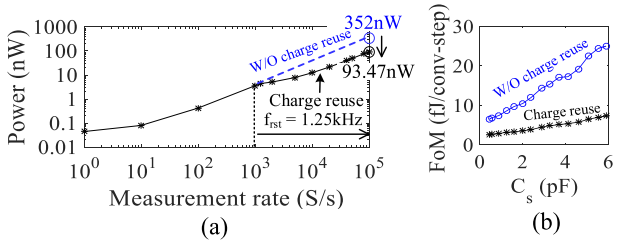

Fig. 8. (a) Measured power consumption (with largest C_s) at different measurement rates and (b) CDC FoM versus C_s at maximum measurement rate.

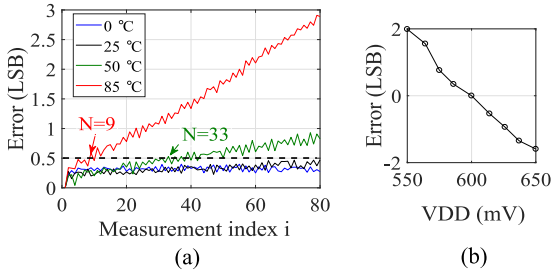

Fig. 9. (a) Measured errors due to bridge leakage at different temperatures ($C_s = 0.458$ pF, worst case) and (b) measured power supply sensitivity.

without and with charge reuse, respectively. Oversampling and averaging can optionally be used to improve the averaged resolution to < 2 fF$_{\text{rms}}$.

Thanks to the all-dynamic architecture, the measured power scales inherently with the measurement rates f_{meas} [Fig. 8(a)]. When $f_{\text{meas}} > 1.25$ kS/s, the reset pulse rate is fixed at 1.25 kHz to enable charge reuse. The higher f_{meas} is, the more energy is saved. When $f_{\text{meas}} \leq 1.25$ kS/s, each measurement requires a reset phase to avoid leakage errors. Thanks to the power-gating technique [5], the standby power of the CDC is reduced to only 44 pW. The FoM of the CDC with charge reuse increases with C_s from 2.5 fJ/conv-step to 7.3 fJ/conv-step [Fig. 8(b)], and remains significantly lower compared to the case without charge reuse. Over the entire C_s range, the average FoM with charge reuse is 4.3 fJ/conv-step.

The errors due to bridge leakage increase at higher temperature [Fig. 9(a)]. At 85 °C, $N \leq 9$ should be used to keep the errors within 0.5 LSB. However, even with $N = 9$, the CDC energy can still be effectively reduced as shown in Fig. 4(b), confirming the effectiveness of charge reuse even at high temperature. When VDD varies $\pm 10\%$ around 0.6 V, the measured error spans from -1.6 to $+2$ LSB [Fig. 9(b)] thanks to the ratiometric architecture. Furthermore,

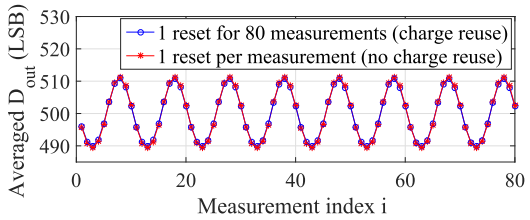

Fig. 10. Demonstration with a MEMS microphone at two reset settings. Noise has been averaged out (test with 10-kHz single-tone sound which is synchronized with the 100 kS/s measurement frequency).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[1]	[7]	[2]	[3] [d]	This work	
Method	SAR	Dual slope	SAR + TDSDM	SAR	SAR	
Technology (nm)	180	180	40	65	65	
Area (mm^2)	0.055	0.105	0.06	0.08	0.00644	
Cap. range (pF)	0~12.66	5.3~30.7	0~5	1.23~4.33	0.458~5.886	
Charge-reuse	–	–	--	--	No	Yes
Resolution (fF)	1.2	8.7 [b]	0.29	4.38 [e]	7.0 [e]	7.3 [e]
SNR (dB)	71.43	44.2 [b]	75.8	47.97 [e]	48.8 [e]	48.4 [e]
Meas. rate (S/s)	62.5k	156.25	80k	1~20k	1~100k	1.25k~100k
Power (nW)	6440	110	6640	0.1~73.8	0.044~352	4.41~93.47
E/conv. (pJ)	103	704	83	3.69 [e]	3.52 [e]	0.94 [e]
FoM (fJ/conv-step) [a]	33	5300 [b]	16	18 [e]	15.7 [e]	4.3 [e]

[a] FoM= (E/conv.)/$2^{(\text{SNR}-1.76)/6.02}$ [b] Calculated with one subrange [c] @ max. meas. rate
[d] $C_r = 2.5$pF [e] Averaged number over the whole cap. range

the CDC is verified with a capacitive MEMS microphone at two reset settings (Fig. 10). As shown, even though C_s changes dynamically, the results with charge reuse match well to the results where each measurement includes a reset.

IV. BENCHMARKING AND CONCLUSION

Table I shows the performance summary of the proposed fully dynamic CDC and a comparison with other works. Thanks to the charge reuse technique, this work achieves the lowest FoM of 4.3 fJ/conv-step. Moreover, it also achieves the lowest reported power consumption and energy/conversion of 44 pW and 0.94 pJ, respectively, with only 6440 μm^2 of chip area, making it a compact, low power, and energy-efficient interface that is suitable for energy-constrained IoT applications.

REFERENCES

[1] H. Omran, A. Alhoshany, H. Alahmadi, and K. N. Salama, "A 33fJ/Step SAR capacitance-to-digital converter using a chain of inverter-based amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 310–321, Feb. 2017.

[2] X. Tang *et al.*, "A 16fJ/conversion-step time-domain two-step capacitance-to-digital converter," in *IEEE Int. Solid- State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 296–297.

[3] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 0.1-nW-1-μW energy-efficient all-dynamic versatile capacitance-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1841–1851, Jul. 2019.

[4] P. Harpe, "A compact 10-b SAR ADC with unit-length capacitors and a passive FIR filter," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 636–645, Mar. 2019.

[5] K. Pelzers, H. Xin, E. Cantatore, and P. Harpe, "A 2.18-pJ/conversion, 1656-μm^2 temperature sensor with a 0.61-pJ·K^2 FoM and 52-pW standby power," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 82–85, 2020.

[6] H. Xin, K. Pelzers, P. Baltus, E. Cantatore, and P. J. A. Harpe, "A 4.3fJ/conversion-step 6440μm^2 all-dynamic capacitance-to-digital converter with energy-efficient charge reuse," in *Proc. Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.

[7] S. Oh *et al.*, "A dual-slope capacitance-to-digital converter integrated in an implantable pressure-sensing system," *EEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1581–1891, Jul. 2015.