Implementation of MOR for time domain simulation on real-life interconnect structures

Implementation of MOR for time domain simulation on real-life interconnect structures

Pieter Heres, Jan Niehof, and Wil Schilders
Philips Research Laboratories
Prof. Holstlaan 4
Email: p.j.heres@tue.nl ; jan.niehof@philips.com

Abstract

Stable equivalent circuit models cannot be guaranteed by currently available EM simulation tooling, resulting in non-convergence in time-domain simulations. Theoretically it is proven that available MOR methods preserve stability and passivity in the reduction process. Implementation of MOR methods and the realization of equivalent circuit models for actual use in circuit simulation are not straightforward. This paper describes the successful implementation of a MOR method, allowing the generation of equivalent circuit models suitable for time domain simulation. Two examples of time-domain simulations performed on real-life interconnect structures are given.

Introduction

The development of today's complex electronic products (e.g. mobile phones, Bluetooth) requires accurate computer simulations. For radio frequency (RF) designs in particular, many parts of the physical system, such as IC (integrated circuit) packages, PCBs (printed circuit boards) and printed components (and also the coupling between them) can only be simulated accurately using numerical electromagnetic field analysis [1,2]. In general, this results in very large matrix systems to be solved, which can be virtually impossible.

For the electromagnetic analysis of complex interconnect structures, the layout simulation tool Fasterix was developed. In Fasterix the interconnect structure is discretized and a boundary element method is used to model the structure as a lumped RLC circuit. In the current implementation, the sometimes very large RLC circuit is represented in a compact way by making use of the so-called 'supernode algorithm' [3], which generates a compact equivalent circuit model for use in circuit simulation. However, since the stability of these models is not guaranteed, transient circuit simulations often result in convergence problems.

In order to remedy these instabilities, a number of Model Order Reduction (MOR) methods, preserving stability and passivity, have been investigated. MOR replaces large systems by smaller, computationally more flexible ones, with approximately the same behaviour. Especially Krylov-subspace methods have shown themselves to be very accurate and suited for this area of application [4,5]. These Krylov-subspace methods are well known and used in many different applications. Not only linear time invariant (LTI) systems can be subject of these methods, also weakly non-linear or quadratic models are treated in the same way as LTI systems [6]. An important issue in reducing the size of models is the preservation of passivity. In order to be able to use the model in circuit simulation, the realization of an equivalent circuit is essential.

The application of Model Order Reduction methods in the layout simulator Fasterix demands a robust implementation suitable for relatively large problems, consisting of singular and non-singular matrices. Several issues of the implementation will be discussed in this paper.

Further, the realization of the reduced model is addressed. The models of the layout simulator are described in n-port models, so also the reduced models have to realized in to n-port models. Time domain simulations have to be done with these circuits.

This paper presents a special implementation of the SVD-Laguerre MOR method [4] and gives the application of this method on two design examples.

Model Order Reduction

First the basic idea of Model Order Reduction via Krylov-subspaces is explained. In general the systems considered in this paper have the form:

$$\begin{pmatrix} \mathbf{C} & \mathbf{0} \\ \mathbf{0} & -\mathbf{L} \end{pmatrix} \tfrac{d}{dt}\mathbf{x}(t) + \begin{pmatrix} \mathbf{G} & \mathbf{P}^T \\ \mathbf{P} & -\mathbf{R} \end{pmatrix} \mathbf{x}(t) = \mathbf{B}_i \mathbf{u}(t)$$

$$\mathbf{y} = \mathbf{B}_o^T \mathbf{x}(t)$$

Many methods for modelling passive electronic components or circuits can be formulated in this way. A nice example of this statement is the Partial Element Equivalent Circuit method (PEEC) by Ruehli [8]. In [7] a similar method is derived. Both matrices can be singular. These equations can be translated into an RLC-circuit. In that case, the state space vector **x** consists of voltages and currents. If the system has more than one input, then $\mathbf{B}_\mathrm{i}$ has more then one column.

A common way to find a solution for these systems is to transform the system into the frequency domain, applying a Laplace transform. The derivative $\tfrac{d}{dt}\mathbf{x}(t)$ is then transformed to $s\mathbf{X}(s)$. The complex variable s can be interpreted as a complex frequency. By eliminating the state space vector a transfer function can be formulated, which gives a direct relation between input and output in the frequency domain:

$$\mathbf{H}(s) = \mathbf{B}_o^T (\mathbf{G} + s\mathbf{C})^{-1} \mathbf{B}_\mathbf{i}$$

There are many methods to replace this large and expensive model by a smaller model, which approximates the behaviour of the original system. In general, a frequency range in which the approximation must be reasonable is predefined. Krylov subspace methods do this by generating a Krylov space $K(\mathbf{B},\mathbf{A}) = [\mathbf{B}\ ,\mathbf{AB}\ ,\mathbf{A}^2\mathbf{B}\ ,...]$ and then projecting the original system onto this space. If the number of columns of this space is smaller then the size of the original system, the system is reduced. If the number of internal nodes is much larger than the number of ports, a significant reduction both in size of the model and in computational time is obtained

The transfer function of the reduced system can be formulated as:

$$\tilde{\mathbf{H}}(s) = \tilde{\mathbf{B}}_o^T (\tilde{\mathbf{G}} + s\tilde{\mathbf{C}})^{-1} \tilde{\mathbf{B}}_\mathbf{i}$$

In the time domain the reduced model will be formulated as:

$$\tilde{\mathbf{C}}\,\tfrac{d}{dt}\tilde{\mathbf{x}}(t) + \tilde{\mathbf{G}}\tilde{\mathbf{x}}(t) = \tilde{\mathbf{B}}_i \mathbf{u}(t)$$

$$\hat{\mathbf{y}} = \tilde{\mathbf{B}}_o^T \tilde{\mathbf{x}}(t)$$

The advantage of Krylov subspace methods is that they are cheap and generally applicable.

There are several properties of the original transfer function, which have to be preserved during reduction, to be able to speak of a good approximation. To start with, obviously the behaviour of the system should be approximated well. Because we have a closed relation in

the frequency domain for this behaviour, the main goal of many Model Order Reduction methods is to approximate the behaviour in the frequency domain. However, finding a good approximation, does not guarantee stability. Stability, the property that in time domain the signal stays bounded, is a very important property. In frequency domain stability is defined as: all poles of the system are in the closed half plane of the complex plane. Poles are defined as follows: all s for which the inverse of ($\mathbf{G}+s\mathbf{C}$) does not exist. PVL, proposed by Freund and Feldmann in [9] is an example of a MOR method, which approximates the frequency behaviour of a system well, but does not always preserve stability. For the methods proposed in [4] and [5] it can be proven that stability is preserved during reduction, which makes them useful for our purpose of applying them to make time domain simulations possible.

Next to being stable, an RLC circuit is also passive. Passivity is defined as the inability to generate energy. Passivity is stronger than stability. A passive circuit is stable if it is combined with any feedback loop. Passivity should also be preserved by a MOR method.

Orthogonalisation

To make MOR method suitable for real-life applications like the layout-simulator Fasterix one should implement the Krylov subspace methods in a robust way. An important issue one then has to deal with is the orthogonalisation of the Krylov-space. Accuracy and efficiency of the methods can be influenced after taking care of the orthogonalisation of the Krylov space.

A straightforward generation of the Krylov space, essentially leads to an ill-conditioned matrix. For accuracy reasons we therefore propose to do the orthogonalisation of the Krylov columns during their generation. This improves the numerical properties of the space and avoids the need of an expensive orthogonalisation afterwards, with for instance Singular Value Decomposition.

The order in which the columns are generated and orthogonalized can be chosen, but a wrong order will lead to loss of information or generation of spurious information. The basic properties of Krylov spaces must be preserved. In the case where a Krylov space is built up for several right-hand sides simultaneously the orthogonalisation a block Arnoldi orthogonalisation as done in [5] provides us with a good order in which the columns of the Krylov space are generated and orthogonalized.

To improve the orthogonality we further propose to orthogonalize twice, to ensure that the columns are orthogonal up to machine precisions. This is done to avoid instability due to numerical round-off errors.

Improvements on the Krylov space

To make the space we project our system matrices on, as small as possible, we applied some improvement to the generation of the Krylov space.

If $\mathbf{B}_i$ has more than one column, the Krylov space consists of blocks. If the number of ports is large, the size of our reduction can grow significantly, because every input needs at least a couple of moments in the space. Observing the norm of the individual columns after orthogonalisation, we sauw that they can be almost zero. Removing them bluntly will violate the basic properties of a Krylov space, which will lead to tremendous errors. Meanwhile using the theory underlying Krylov subspace, we found a way to remove redundant column, without violating the basic properties of the Krylov space. This enables us to limit the size of a Krylov space associated to different ports.

But even with this last improvement, Krylov subspace methods generate redundant information, for instance poles far outside of our spectrum, or poles with a small residue. Using a method similar to Implicit Restart by Sorensen in [10], we are able to remove unwanted poles, from the spectrum of our reduced model.

Realization

The need for a realization of the reduced circuit is obvious. We would rather not calculate expensive time-domain results via the frequency domain results. We also would like the model to be usable in different settings and for different input signals. We want to represent the reduced n-port model in terms of a circuit, understandable for a circuit simulation.

Note that the state space vector of a general RLC-circuit consists of both voltages and current. In general, projecting the state space vectors mixes the voltages and current and therefore the reduced system has lost its physical meaning. We propose therefore to define the reduced state space vector consisting entirely of voltage unknowns. The separate rows of the reduced model can then be interpreted as current relations. With a combination of resistances, capacitors and current sources these rows in the reduced matrices can be realized. No inversion or other matrix decompositions are needed for this purpose.

Because the number of ports is preserved during reduction, we are still able to couple the ports of the reduced system to the rest of the circuit. With these circuits we were able to do stable transient simulations.

Results

The performance of the implemented MOR technique is evaluated by performing electromagnetic simulations on real-life interconnect structure with the 2.5D EM simulator Fasterix.

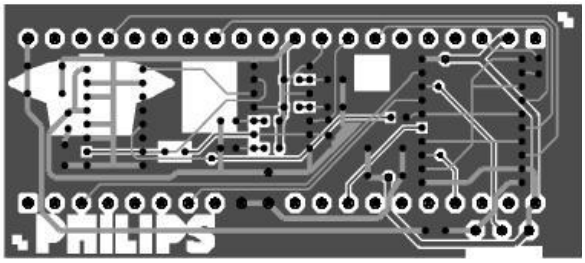

Figure 1: Layout of a 2-layer test PCB.

A transient circuit simulation is performed on the complete circuit on the test PCB shown in Figure 1. The equivalent circuit model for the complete interconnect structure is obtained using the implemented SVD-Laguerre MOR method. The full matrix consists of 4613 by 4613 elements. After reduction the matrix size is 228 by 228. The equivalent circuit model has 57 ports. The results of the simulation are given in Figure 2. The low frequency sine wave clearly shows the effects of the cross talk from the high frequency switching signal.

Figure 3 shows the layout of a double LC-filter. The inductors are implemented as printed coils. Again the implemented SVD-Laguerre MOR method is used to generate an equivalent circuit for this structure. The full matrix size is 695 by 695. The reduced system has the size 77 by 77. The equivalent circuit model has 11 ports. In the transient circuit simulation a step-shaped signal is supplied at the input. The rise and fall time of the input signal are 100 ps. The step response is observed at the output of the circuit. Both curves are given in Figure 4.

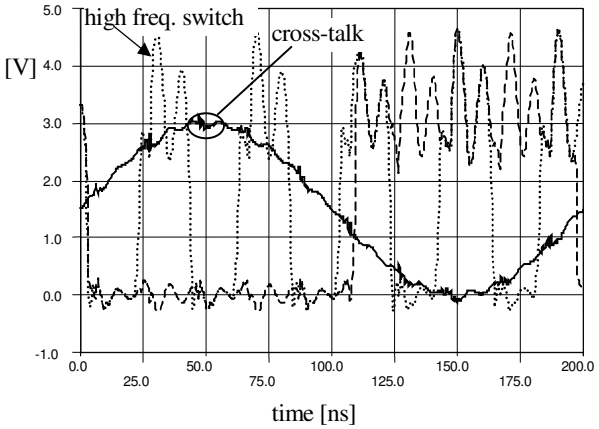

Figure 2: Transient simulation results on the test PCB.

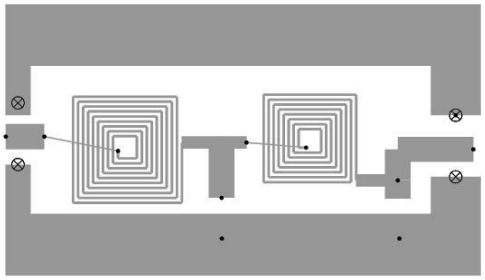

Figure 3: Double LC-filter layout structure.

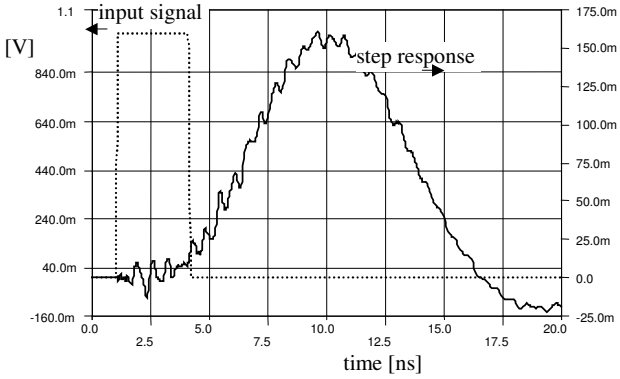

Figure 4: Results step-response simulation on LC-filter.

Conclusions

Time domain circuit simulations can now be performed on electromagnetic equivalent circuit models generated by the implemented SVD-Laguerre MOR method.

The reduced systems are provably stable and passive. Furthermore, the models generated by the implemented method are typically much smaller than those generated by the conventional equivalent circuit generation method, resulting in less evaluation time in the circuit simulator.

References

[1]T.A.M. Kevenaar, E.J.W. ter Maten, H.H.J.M. Janssen, S.P. Onneweer, *"Methods and Approaches for RF Circuit Simulation and Electromagnetic Modelling"*, Proc. SCEE 2002, Eindhoven 2002, to appear in Mathematics in Industry, Springer Verlag, Berlin.

[2]J. Niehof, N.J. Pulsford, I. Lodema, J. Meeuwis*, "Electromagnetic Simulation of Real-Life Circuits: A Mobile Phone Power Amplifier Module and an FM Radio Tuner PCB",* Proc. SCEE 2000, pp. 277-284, August 20-23, Warnemünde, Germany, 2000.

[3]R. du Cloux, G.P.J.F.M. Maas, A.J.H. Wachters, *"Quasi-static Boundary Element Method for Electromagnetic Simulation of PCBs"*, Philips J. Res., 1994, Vol. 48, pp. 117-144.

[4]Luc Knockaert and Daniel De Zutter, *"Passive Reduced Order Multiport Modeling: The Padé-Arnoldi-SVD Connection"*, Int. J. Electronics and Communications, 1999, Vol 53, pp. 254-260.

[5]A. Odabasioglu and M. Celik, *"PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm"*, IEEE Trans. Computer-Aided Design, 1999, Vol. 17, pp. 645-654.

[6]P. Gunupudi and M. Nakhla, *"Non-linear Circuit-Reduction of High-Speed Interconnect Networks using Congruent Transformation Techniques"*, IEEE Trans. Advantaged Packaging, 2001, Vol. 24, no. 3, pp 317-325.

[7]R. Du Cloux, G.P.J.F.M. Maas and A.J.H. Wachters, *"Quasi-static boundary element method for electromagnetic simulation of pcb's"*, Philips J. Res., 1994, Vol.48, pp.117-144.

[8]A.E. Ruehli, *"Equivalent Circuit Models for three dimensional multiconductor systems"*, IEEE Trans. Microwave Theory, 1974, Vol. 20, pp. 216-221.

[9]R.W. Freund and P. Feldmann *"Efficient Linear Circuit Analysis by Padé Approximation via the Lanczos Process"*, IEEE Trans. Computer-Aided Design, 1993, pp. 137-158.

[10] D.C. Sorensen, *"Implicit Application of Polynomial Filters in a k-step Arnoldi method"*, SIAM J. Matrix Analysis and Applications, 1992, Vol. 13, no.1, pp 357-385.