Protection Interface Concept for LV Grids with an Efficient Dynamic Voltage Restorer

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***Abstract*—Power quality (PQ) issues are often the reason for malfunctions and interruptions in the low-voltage (LV) utility grid. Protection from voltage sags and swells can be achieved using dynamic voltage restorer (DVR) circuits. The diffusion of grid scale energy storage has renewed interest for battery-fed DVR converters for voltage support, where sensitive loads are connected to the grid. At the same time, the next generation smart grid calls for the design of efficient and compact power converters with minimum impact on the grid. In this paper, a concept design for a battery-fed DVR is proposed with particular focus on energy efficiency and power density. The layout, operation and control strategy of the converter are presented and supported by simulation results. The study lays the basis for the implementation of a 30-kVA prototype.**

Keywords— Converter Simulation, Dynamic Voltage Restorer, Power Quality, Silicon Carbide.

I. Introduction

In nowadays power transmission and distribution systems, power quality (PQ) problems such as grid voltage unbalances, sags, transients, harmonics, etc., are considered one of the main reason of inefficiency [1]. These issues can induce sensitive electrical equipment to operate outside safe conditions, causing shutdowns, failures or excessive stress. As the number of non-linear loads such as switching power converters multiplies, PQ issues are becoming more common and harmful, and there is increasing need for grid interfaces that guarantee protection from abnormal events and reliable power supply. Moreover, increasingly common distributed generation (DG) systems, such as renewable energy sources, have to be robust enough to withstand PQ disturbances without disconnecting from the grid [2] and interrupting their service. The most common PQ issues – and also those with the worst impact – are voltage sags or swells due to remote faults in the medium voltage (MV) grid or switching of large loads. Voltage sags are defined as a decrease in the rms value of grid voltage below nominal range, ranging from 0.1 to 0.9 p.u. and last for half a cycle to one minute. On the other hand, voltage swells are defined as a fast increase in the rms grid voltage above nominal range, ranging from 1.1 to more than 2.5 p.u. and lasting for half a cycle to one minute. The sag or swell can be either balanced among the phases or unbalanced, depending on the kind of MV fault. In fact, the occurrence of voltage sags is much more frequent than swells. According to [3], the greatest share of sags is characterized by short duration (<5 s) and low magnitude (<0.5 p.u. of the nominal voltage). As far as over-voltages are concerned, the ones with amplitude greater than 1.7 p.u. – due to fast arcing transient or lighting surges – generally last less than one second [4]. Standard surge arresters, breakers and fuses placed on both sides of the distribution transformer can provide sufficient protection against these events.

Immunizing electrical equipment against PQ disturbances requires fault-tolerant design or installing uninterruptible power supplies (UPS), which often comes at high expenses. Dynamic voltage restorer (DVR) circuits, first proposed in [5], offer a cost-effective protection interface solution. DVRs are designed to inject an appropriate voltage in series with the source and compensate for disturbances, so that the load always sees a sinusoidal voltage with nominal amplitude. The converter is capable of bidirectional power flow, transferring power to the grid in case of sags and absorbing it if swells occur. Fig. 1 depicts a typical example application for a battery-fed protection interface DVR – in this case some of the sensitive non-linear loads are EV chargers. When the battery is fully charged, an energy dissipation system is required in case of voltage swells. The study in [6], a comparison of the different DVR topologies that have emerged during the years is provided, identifying mainly two categories: DVRs with integrated energy storage and DVRs without energy storage. The first kind taps the energy needed for voltage support from a dc link or an energy storage system. Nevertheless, the low availability and high cost of large-capacity energy storage solutions has limited the diffusion of this kind of DVR in the past. However, the recent price drop of grid-scale energy storage has seen renewed interest in this DVR topology [7–9], based on battery energy storage systems (BESS), ultracapacitors (UCAP), flywheels and superconductive magnets. The DVR architectures

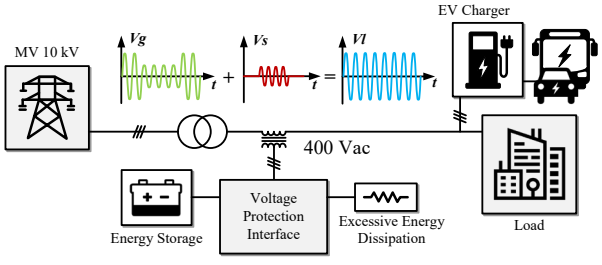

Fig.1. Example of series-connected DVR as a protection interface in a LV grid.

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without energy storage, instead, have to rely on the faulty grid power supply to function, tapping energy from shunt converters connected either on to the supply or the load side. They generally use compensation strategies based on both active and reactive power exchange. In terms of performance and reliability, the DVR with integrated energy storage was found to be the most effective, despite the higher cost for the energy storage system. This is mostly due to the fact that this topology is independent from the faulty grid and can provide high active power for voltage compensation.

A battery-fed DVR is generally a two-stage circuit: a bidirectional dc stage is used to keep constant voltage on a dc-link despite the voltage variation of the BESS, and a voltage source inverter (VSI) generates the three-phase voltage required for compensation [6]. Nevertheless, since the majority of the voltage sags/swells are low in magnitude, the use of a dc stage to boost the energy storage voltage is not always necessary for the inverter to produce the injected voltage. For this reason, a new topology, based on a dual-dc-port layout has been introduced in [10], which allows to reduce the rating for the dc stage and increase the overall efficiency. In this design, the inverter is arranged in a T-type layout [11] and can be controlled as two- or three-level, depending on the magnitude of the injected voltage. In this case, the dc stage only processes power when the battery voltage is low or the swell/sag magnitude is large.

The current trend in power electronics design is towards increased efficiency, reliability and power density, in the effort to transition to a low-carbon smart grid. For this reason, power converters like DVRs need to fulfill both the requirements of grid support and protection and have the smaller possible impact on the grid. A main drawback in the operation of high-power DVRs is the power consumption in standby mode in both dc and ac stages, as well as the long idle time in between sags/swells. This calls for an improvement in the design and component selection to maximize efficiency and usage. In this paper, we address this issues by introducing an improved topology for a dual-dc-port DVR and using wide-bandgap (WBG) devices, namely SiC MOSFETs. These devices offer comparatively better performance and efficiency compared to IGBTs [12], and allow higher switching frequency, which enables a reduction in the size of passive components. The converter architecture, control and modulation strategies are presented, and a Simulink-based model was implemented to verify the viability of the concept by simulation. The aim of this work is to obtain preliminary insight for the future realization of an efficient, high-power DVR prototype.

II. DVR Concept

The proposed converter topology is depicted in Fig. 2. The double-dc-port structure is made up of a T-type voltage-source inverter (VSI) and a three-phase interleaved dc stage [13]. All the switches used here are SiC power MOSFETs. The low-voltage (LV) dc-bus connects the battery directly to the inverter switches or to the input port of the dc stage. A common-drain switch configuration on the LV side is used to ensure bidirectional power flow. The high-voltage (HV) bus connects the output port of the dc-stage to the upper switches of the inverter legs. The choice of an interleaved dc stage poses several advantages:

1) Lower current rating for the switches and lower overall conduction losses;
2) Design of smaller filter inductors with multiphase interleaving to increase power density and reduce current ripple;
3) Possibility of fault-tolerant operation and reconfiguration of the converter for alternative functions.

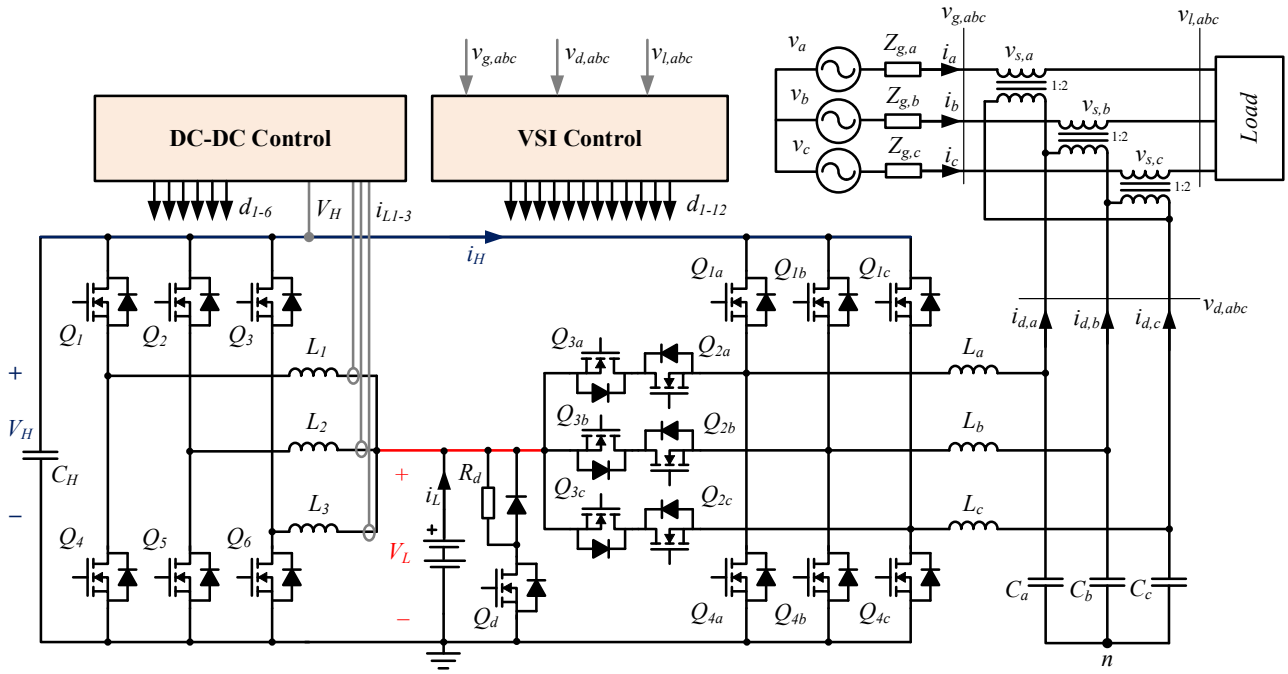

Fig.2. Circuit schematic of the proposed dynamic voltage restorer (DVR).

In addition, a battery overvoltage protection stage is included to dissipate excess energy resulting from voltage swell compensation. This stage is based on a simple chopper leg topology with a PWM-controlled bottom switch (Q_d), discharging the LV bus on a power resistor (R_d). The three-phase transformer for grid coupling is connected in series with the line feeder on its primary, while the secondary uses a delta connection to eliminate the triple harmonics from the injected voltages. The turn ratio chosen for the transformer windings is 1:2, which allows reducing the current on the secondary side and exploit the voltage rating of the SiC MOSFEs , which is desirable to reduce the ohmic losses.

A. Converter Operation

In order for the load to see nominal voltage, the series voltage $v_{s,i}$ injected by the DVR has to be

$$v_{s,i} = v_{g,i} - v_{l,i} \quad i = a,b,c \tag{1}$$

where $v_{g,i}$ and $v_{l,i}$ are respectively the grid supply and load phase voltage. The inverter rms line-to-line voltage $V_{d,LL}$ is 2 times the rms injected voltage V_s, while the rms phase current in the DVR I_d is $\sqrt{3}/2$ times the rms grid phase current I_g. A simplified circuit diagram of the converter is represented in Fig. 3, where l is the voltage level of the LV dc bus. The DVR can operate in two modes: if $0 < \sqrt{2}V_{d,LL} < l$ the series voltage is generated only using the LV dc bus in two-level operation; if $l < \sqrt{2}V_{d,LL} < 2$, the HV dc bus is also used to generate the series voltage, so that the inverter operates as three-level [14]. The bidirectional dc stage is active only in the second case to regulate the voltage on the HV dc link. It is desirable to keep the battery level high so that most of the disturbances can be corrected using the two-level mode, and thus saving additional losses in the dc stage.

B. Energy Storage considerations

Assuming that only active power is injected or drawn from the grid during a sag/swell event, the energy E_s exchanged for the compensation, given by (2), is dependent on the series rms voltage V_s and current I_g, the DVR overall efficiency η_{DVR} and the event duration Δt_e.

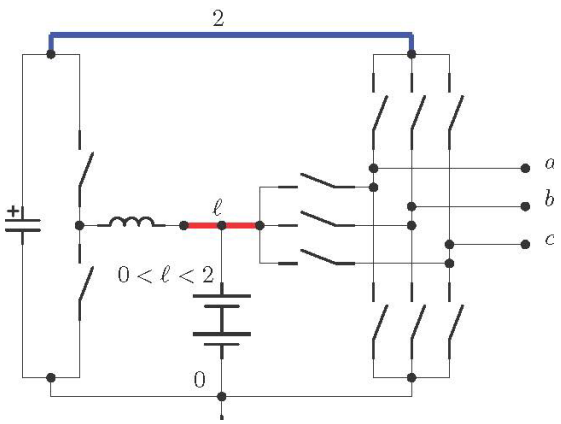

Fig.3. Simplified schematic of a dual-port DVR.

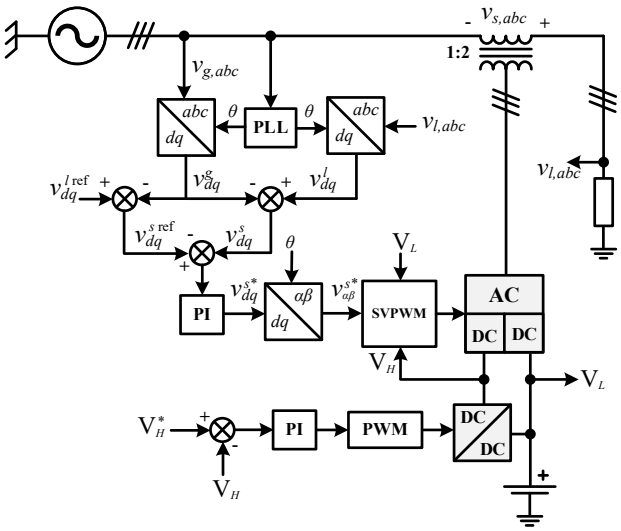

Fig.4. Diagram of the proposed control technique.

$$E_s = \frac{3V_s I_g}{\eta_{DVR}} \Delta t_e \tag{2}$$

This means that a higher-efficiency DVR reduces the energy storage rating. The minimum capacity for the BESS is

$$BC[Ah] > \hat{E}_s / V_{bess} \tag{3}$$

where $\hat{E}_s$ is the peak exchanged energy – in the worst case sag/swell scenario – and V_{bess} is the nominal battery voltage.

III. CONTROL STRATEGY

Several methods have been proposed to control DVRs. In particular, three main techniques are reported in [15], [16], namely: *pre-sag* compensation, *in-phase* compensation and *energy*-optimized compensation. The in-phase compensation method has been chosen for the purpose of this study and in the simulations. In this method the voltage is compensated in phase with the grid. A phase-locked loop (PLL) is synchronized with the grid voltage. In this way, the amplitude of the injected voltage is minimized, although this method does not cancel phase jumps – which often come with voltage disturbances. A diagram of the adopted control scheme is depicted in Fig. 4.

The bidirectional dc stage is controlled using a unified voltage loop proposed in [17], which ensures smooth transition between charging and discharging of the HV dc-link. The gate signals of each leg are phase-shifted by 120°.

A. Inverter Modulation Strategy

An asymmetrical space vector modulation (SVPWM) has to be used in order to generate the gate signals for the dual-port inverter [14]. Since the LV dc bus voltage is variable, the standard three-level SVPWM needs to be modified. Each of the converter phases can assume the three following switching states

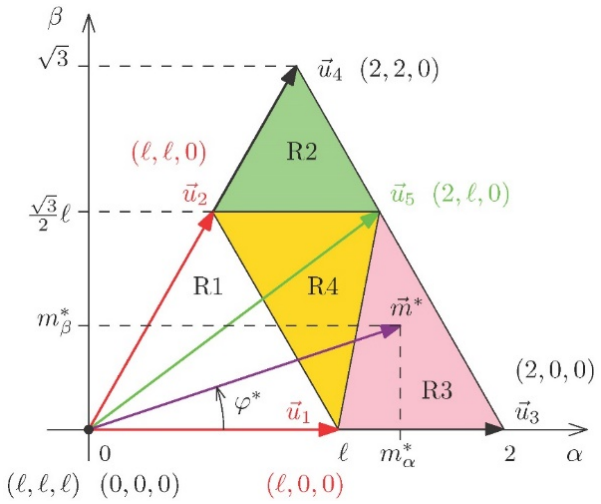

Fig.5. SVPWM vector diagram in the first sector.

$$S_{Qi} = \begin{cases} 2\ (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (1,1,0,0) \\ l\ (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (0,1,1,0) \\ 0\ (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (0,0,1,1) \end{cases} \quad (4)$$

Fig. 5 depicts the possible vectors that can be used to synthesize the voltage reference vector $\vec{m}^*$ in the stationary $\alpha\beta$ reference frame for the first sector. Groups of three vectors define four regions in the sector. As showed in Fig. 6, in each of the regions, the reference vector can be constructed as a linear combination of three vectors $(\vec{e}_0, \vec{e}_1, \vec{e}_2)$ expressed in (5), where d_1 and d_2 represent the time share of each vector within a switching period.

$$\vec{m}^* = (1 - d_1 - d_2)\,\vec{e}_0 + d_1\vec{e}_1 + d_2\vec{e}_2 \quad (5)$$

In order to calculate d_1 and d_2 across each sector, the vectors can be decomposed in their $\alpha\beta$ components, as in (6), and the refence frame is rotated using the matrix Q. The vector time shares can be obtained using (7-9).

$$\vec{m}^* = \frac{m^*_\alpha}{\|\vec{e}_\alpha\|}\vec{e}_\alpha + \frac{m^*_\beta}{\|\vec{e}_\beta\|}\vec{e}_\beta \quad (6)$$

$$\vec{m}^* = \vec{e}_0 + d_1\vec{e}'_1 + d_2\vec{e}'_2 \quad (7)$$

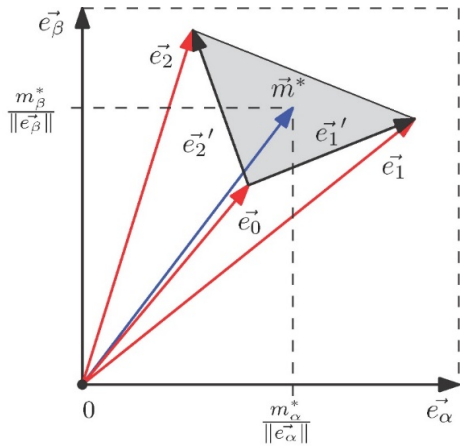

Fig.6. Construction of the voltage reference vector.

$$\begin{bmatrix} \vec{e}'_1 \\ \vec{e}'_2 \end{bmatrix} = [Q] \begin{bmatrix} \vec{e}_\alpha \\ \vec{e}_\beta \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} d_1 \\ d_2 \end{bmatrix} = [Q^{-1}]^T \begin{bmatrix} \frac{m^*_\alpha}{\|\vec{e}_\alpha\|} - e_{0\alpha} \\ \frac{m^*_\beta}{\|\vec{e}_\beta\|} - e_{0\beta} \end{bmatrix} \quad (9)$$

IV. Simulation Results

A model of the grid-connected DVR was implemented in Simulink/PLECS with the parameters reported in Tab. I. The simulation results for a the compensation of a 0.2 p.u. voltage sag are showed in Fig. 7.a-c while the results in case of a 2 p.u. swell are showed in Fig. 8.a-c. In both this simulation the initial battery voltage is set to 500V, to demonstrate the double-dc-port operation. The DVR is effective in both cases in restoring the load voltage to nominal conditions in less than half of a fundamental cycle (10 ms). The dc stage is active in boost mode, charging the HV dc link, and discharging it in

TABLE I. Simulation Parameters

Parameter	Symbol	Value	Unit
Nominal grid voltage	$V_{g,LL}$	400	V_{rms}
DVR rated power	S_{DVR}	30	kVA
LV dc-link voltage	V_L	470÷680	V
HV dc-link voltage	V_H	800	V
Switching frequency	f_s	40	kHz
Grid filter inductance	$L_{a,b,c}$	360	µH
Grid filter capacitance	$C_{a,b,c}$	2	µF
DC filter inductance	$L_{1,2,3}$	220	µH
HV dc-link capacitance	C_H	1.25	mF

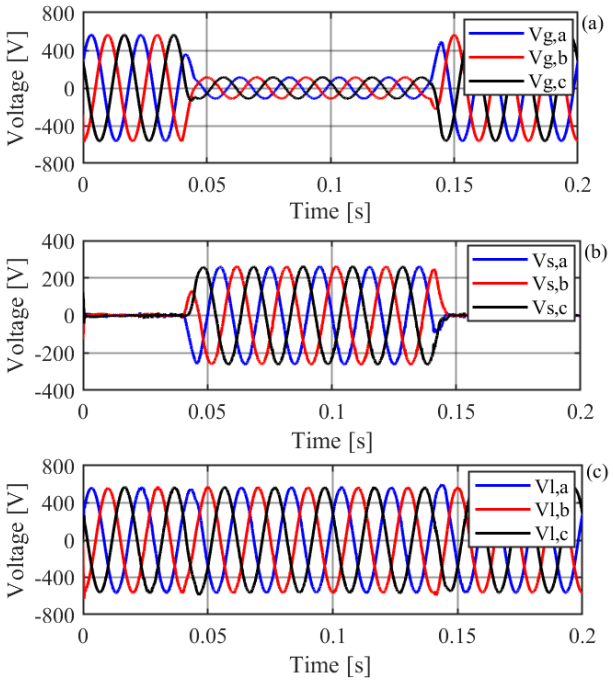

Fig. 7. Simulated waveforms of grid (a), series (b) and load (c) voltage during a 0.2 p.u. sag event at V_L=500V.

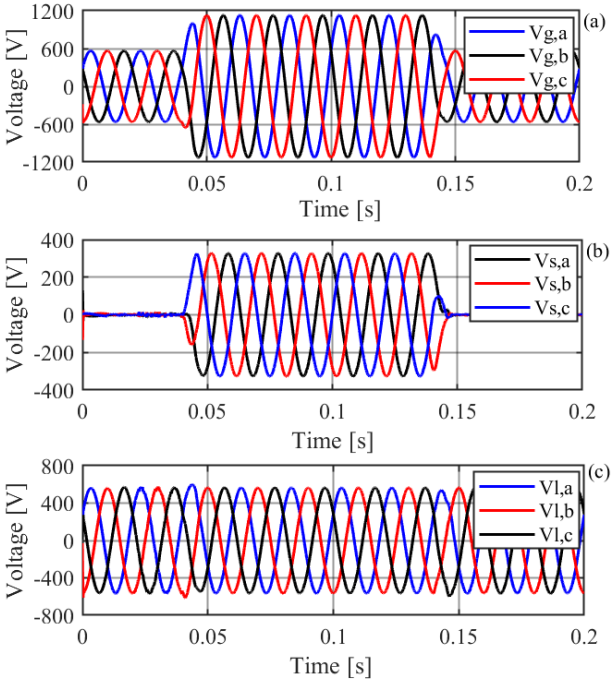

Fig. 8. Simulated waveforms of grid (a), series (b) and load (c) voltage during a 2 p.u. swell event at V_L =500V.

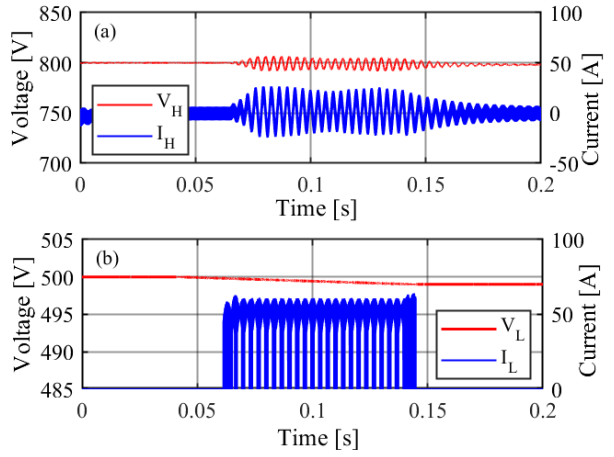

Fig. 9. Simulated waveforms of HV dc-bus voltage and current (a), and LV dc-bus voltage and current (b) during a 0.2 p.u. voltage sag at V_L =500V.

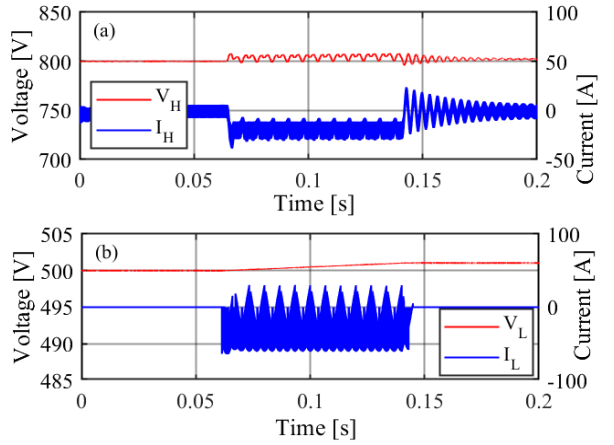

Fig. 10. Simulated waveforms of HV dc-bus voltage and current (a), and LV dc-bus voltage and current (b) during a 2 p.u. voltage swell at V_L =500V.

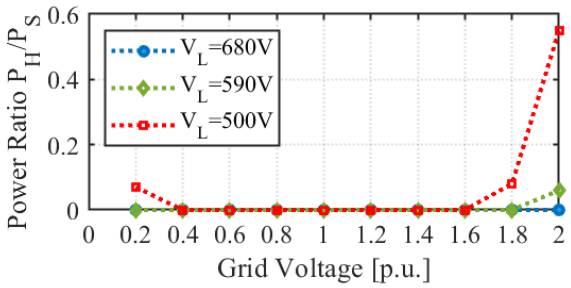

Fig.11. Ratio of the HV port active power and the total injected power vs. p.u. grid voltage at different V_L.

buck mode during the overvoltage. The voltage and current in the HV and LV ports during the voltage sag can be observed respectively in Fig.9a and Fig. 9b. Here it can be noticed that the battery voltage drops as the active power is injected to support the grid. Vice-versa, in Fig. 10a-b, the opposite power flow is evident, with the battery voltage increasing as the swell is compensated. The voltage regulation on the HV dc-link is effective in both cases, with less than 1% deviation from the nominal value. With the control technique adopted for the interleaved dc stage, the dc inductors are always in continuous conduction mode (CCM). It can be noticed in Fig. 8a and 9a that the dc stage is always switching current, even when no net active power is flowing. This generates losses in the switches and the inductors. A way to minimize these idle losses is to keep V_L as high as possible – i.e. keep the battery at high state of charge – since the current ripple magnitude is proportional to $V_H - V_L$.

The simulation also show how the power is shared between the HV and LV port for different conditions. In particular, Fig. 11 shows the ratio of the active power flowing through the HV port P_H and the total injected power P_S at different sag/swell amplitude and variable battery voltage. The dc stage is only active for high amplitude sags/swells and reaches peak power in the worst case of 2 p.u. voltage swell at minimum battery voltage. This means that the dc stage power rating can be about 45% smaller than the DVR nominal power.

Preliminary simulations considering the semiconductor and inductor power losses result in a peak efficiency around 99.17%. Fig. 12 shows the efficiency variation over the full range of output power, proportional to the sag/swell magnitude, for the extreme values of V_L, which corresponds to the battery state of charge.

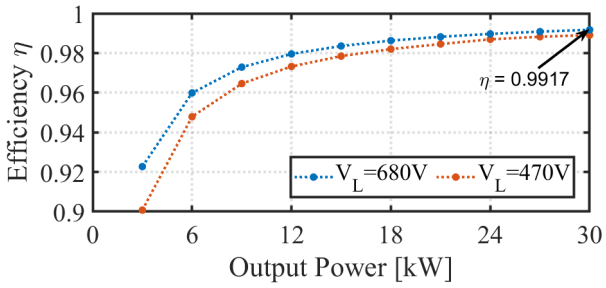

Fig.12. Simulated converter efficiency vs. output power at different V_L.

Moreover, the simulation did not show significant EMI injection in the grid voltages and currents, but further investigation is required to evaluate this aspect.

V. Conclusion

The concept of a LV grid protection interface based on a battery-fed DVR has been presented in this paper. Compared to the solutions available in literature, the proposed DVR features an interleaved bidirectional dc stage and adopts SiC MOSFET as switches. This solution aims to improve efficiency and power density. The layout and control strategy were presented and the performance of the system has been simulated in Simulink, demonstrating effective dynamic compensation of large-magnitude voltage sags and swells. The results represent the first step in the realization of a 30-kVA prototype to validate the performance and efficiency of the proposed design. Additionally, the possibility of repurposing the converter to obtain additional grid-support functionalities, such as harmonic mitigation, will be explored in future work.

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