# 40 Gb/s all-optical packet clock recovery with ultrafast lock-in time and low inter-packet guardbands

**E. Kehayas, L. Stampoulidis, H. Avramopoulos**

*Photonics Communications Research Laboratory, Electrical and Computer Engineering Department, National Technical University of Athens, Zografou, 15773, Athens, Greece*
ekeha@mail.ntua.gr

**Y. Liu, E. Tangdiongga and H. J. S. Dorren**

*COBRA Research Institute, Faculty of Electrical Engineering, Eindhoven University of Technology, 5600MB, Eindhoven, The Netherlands*
y.liu@tue.nl

**Abstract:** We demonstrate a 40 Gb/s self-synchronizing, all-optical packet clock recovery circuit designed for efficient packet-mode traffic. The circuit locks instantaneously and enables sub-nanosecond packet spacing due to the low clock persistence time. A low-Q Fabry-Perot filter is used as a passive resonator tuned to the line-rate that generates a retimed clock-resembling signal. As a reshaping element, an optical power-limiting gate is incorporated to perform bitwise pulse equalization. Using two preamble bits, the clock is captured instantly and persists for the duration of the data packet increased by 16 bits. The performance of the circuit suggests its suitability for future all-optical packet-switched networks with reduced transmission overhead and fine network granularity.



**OCIS codes:** (060.2330) Fiber optics communications; (230.1150) All-optical devices; (250.5980) Semiconductor Optical Amplifiers; (050.2230) Fabry-Perot.

## References and links

1. D. J. Blumenthal, "Optical packet switching," in Proceedings of European Conference on Optical Communication (ECOC'2004), Stockholm, Sweden, pp. 830-833 (2004).
2. E. Kehayas. G. T. Kanellos, L. Stampoulidis. D. Tsiokos, N. Pleros, G. Guekos and H. Avramopoulos, "Packet-format and network-traffic transparent optical signal processing," J. Lightwave Technol. **22**, 2548-2556 (2004).
3. S. Kimura, A. Okada, J. Endo, Y. Suzuki and M. Matsuoka, "A 10 Gbit/s burst-mode 3R receiver unit with a new equalizing amplifier for high-speed optical packet communications," in Proceedings of European Conference on Optical Communication (ECOC'2003), Rimini, Italy, pp. 1042-1043 (2003).
4. M. Mohrle, C. Bornholdt, O. Brox, S. Bauer and B. Sartorius, "Multi-section DFB lasers for high speed signal processing/regeneration," Optical Fiber Communication, (Optical Society of America, Washington, D.C., 2002), paper TuU1.
5. D. T. K. Tong, B. Mikkelsen, T. N. Nielsen, K. F. Dreyer and J. E. Johnson, "Optoelectronic phase-locked loop with balanced photodetection for clock recovery in high-speed optical time-division-multiplexed systems," IEEE Photon. Technol. Lett. **12**, 1064-1066 (2000).
6. J. Slovak, C. Bornholdt and B. Sartorius, "All-Optical 3R Regenerator for Asynchronous Data Packets at 40 Gb/s," in Proceedings of European Conference on Optical Communication (ECOC '2004), Stockholm, Sweden, pp. 388-389 (2004).
7. Z. Hu et al., "40 Gb/s Optical Packet Clock Recovery Using a Travelling-wave Electroabsorption Modulator -Based Ring Oscillator," in Proceedings of European Conference on Optical Communication (ECOC'2004), Stockholm, Sweden, pp. 436-437 (2004).
8. E. Tangdiongga, J. P. Turkiewicz, G.D. Khoe and H. de Waardt, "Clock recovery by a fiber ring laser employing a linear optical amplifier," IEEE Photon. Technol. Lett. **16**, 611-613 (2004).
9. C. Bintjas, K. Yiannopoulos, N. Pleros, G. Theophilopoulos, M. Kalyvas, H. Avramopoulos and G. Guekos, "Clock recovery circuit for optical packets," IEEE Photon. Technol. Lett. **14**, 1363-1365 (2002).

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005

10. N. Pleros, G. T. Kanellos, C. Bintjas, A. Hatziefremidis and H. Avramopoulos, "Optical Power Limiter using a saturated SOA-based Interferometric Switch," IEEE Photon. Technol. Lett. **16,** 2350 – 2352 (2004).
11. R. J. Manning and G. Sherlock, "Recovery of a π phase shift in ~12.5 ps in a semiconductor laser amplifier," Electron. Lett. **31**, 307-308 (1995).

## 1. Introduction

Optical packet switching (OPS) has been introduced as a true broadband solution for delivering bandwidth-intensive applications and alleviating the network from bandwidth bottlenecks [1]. Transmission of packet-mode traffic leads to bandwidth-on-demand use, whereas the ability to operate with short and closely-spaced packets results in finer network granularity and increases the overall transmission efficiency, respectively. In order to achieve a more efficient use of capacity and optimize the resource utilization within the network, OPS sub-systems should process each incoming data packet as a completely independent entity without additional overhead and preamble fields leading to packet-format transparency [2]. The above requirements, however, pose stringent operational characteristics on the sub-systems responsible for all-optical node synchronization, requiring clock extraction on a per-packet basis. In this rationale, the most important performance metrics of such a packet clock recovery circuit are the lock-in time and clock persistence time. Ideally, to achieve maximum bandwidth utilization, a packet clock should be generated instantaneously and persist only for the duration of the incoming data packet.

In order to keep up with or even surpass the rapid evolution of electronic techniques that can now operate with bursty traffic at 10 Gb/s [3], optoelectronic and all-optical clock recovery techniques have been recently upgraded from 10 Gb/s [4-5] to 40 Gb/s [6-7] and even to 160 Gb/s extracting the optical clock at 10 Gb/s [8]. Optical clock recovery circuits, such as electro-absorption modulators [7] and ring-lasers [8] require a significant time interval for synchronization to the data streams and are most suitable for traffic in the form of large aggregated packets. The approach reported in [7] shows very high quality recovered clock signals but requires a lock-in time of 300 ms and exhibits a clock persistence of 400 ms. Self-pulsating DFB lasers require less overhead for clock acquisition with recent results showing 3 ns lock-in time and 10 ns clock persistence at 40 Gb/s [6].

In this letter we demonstrate a 40 Gb/s all-optical packet-mode clock recovery circuit based on the concept presented in [9] extending the bit-rate and reporting better operational characteristics and more detailed performance evaluation. By fully exploiting the potential offered by this technique we show for the first time, instant 40 Gb/s clock extraction from short and closely-spaced packets using simple optical components that do not require complex and specialized fabrication techniques. The clock recovery circuit operates successfully with 40 Gb/s packets that have only 1 ns duration and sub-nanosecond spacing of 750 ps. Specifically, the optical circuit locks instantly to the incoming packet traffic, self-extracting pulsed clock packets with 400 ps clock persistence. These unique operational attributes allow for optical signal processing of packet traffic leading to optical networks with high bandwidth utilization and finer granularity.

## 2. Concept

The circuit consists of two fundamental building blocks: a retiming passive element and a reshaping optical gate. The passive element is a Fabry-Perot filter tuned to the line-rate and due to its low Q-factor (low finesse), it has a short exponential decaying impulse response that allows for independent packet-to-packet processing. Exploiting the short memory effect of the filter, incoming data packets are transformed to clock-resembling packets with intense amplitude modulation and duration similar to the data packets. Since the filter cavity transit time is equal to one bitslot, each incoming data pulse generates a short exponentially decaying pulsetrain that either partially fills the zeros within the packet or constructively interferes with successive pulses of the packet. Due to the choice of low filter finesse, the number of internal reflections within the filter is low and hence the required short impulse response is achieved.

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005

This generated clock-resembling signal, however, suffers from intense pulse-to-pulse amplitude modulation that is removed by utilizing an optical power-limiting gate [10]. The optical gate was realized using a Semiconductor Optical Amplifier (SOA) based Ultrafast Nonlinear Interferometer (UNI) powered by a local CW signal. The strong CW input power heavily saturates the SOA and, acting as a holding beam [11], it biases the amplifier close to its material transparency point. In this case, strongly amplitude modulated control pulses invoke similar gain ripples to the SOA and induce similar phase response that never exceed π-phase shift, leading to pulse equalization. Combination of these two elements results to the self-extraction of a clock packet from each incoming data packet, with low rise and fall times.

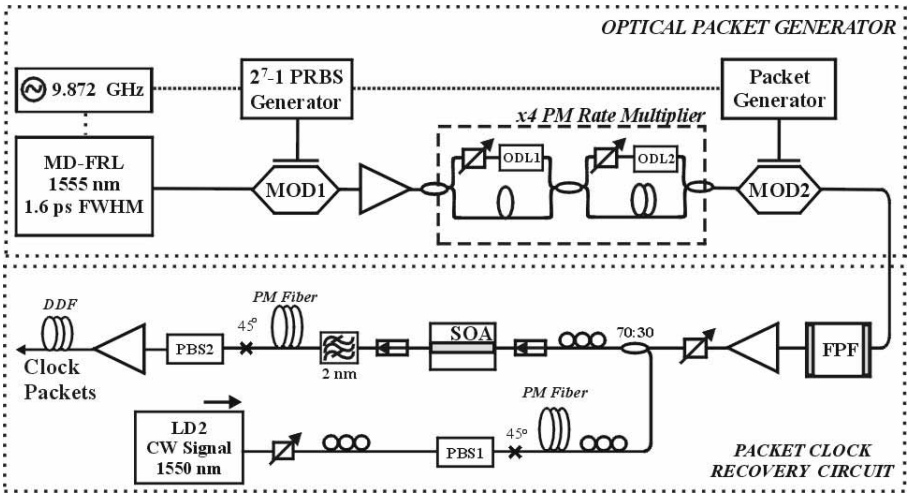


Fig. 1. Experimental setup.

## 3. Experiment

The block diagram of the experimental setup is shown in Fig. 1 and consists of the optical packet generator and the clock recovery circuit. An actively mode-locked fiber ring-laser (MD-FRL) provided a 9.872 GHz pulse train consisting of 1.6 ps pulses at 1555 nm. This pulse train was modulated to form a $2^7$-1 PRBS signal using a PRBS generator and a Ti:$LiNbO_3$ modulator (MOD1) and was then rate-upgraded in a polarization maintaining (PM) bit interleaver to generate a 39.488 Gb/s pseudo-data stream. Data packets of adjustable length and period were formed using a second electro-optic modulator (MOD2) driven by a programmable PRBS generator.

The generated packets were fed into the packet clock recovery circuit, consisting of a low-Q FPF and a SOA-based UNI gate, powered by a CW signal at 1550 nm (LD2). The FPF played the role of the passive optical resonator that extracts the line rate spectral component. Exploiting the filter memory effect, the data packets are transformed into clock packets with intense amplitude modulation. The FPF used was a bulk, micrometer-adjustable fused quartz substrate with free spectral range (FSR) equal to the line rate and finesse equal to 50. The output of the filter was amplified and inserted into the UNI gate as the control signal. The UNI gate was optimized for 40 Gb/s operation by using PM fiber that induces 5 ps of birefringent delay in the two orthogonal polarization components of the input and output ports of the gate. As a result, an asymmetric switching window with respect to the bitslot is formed, relaxing the requirement for the SOA recovery time. The CW signal power was adjusted to saturate the SOA and bias the interferometer in the saturated regime. The saturation of the nonlinear gate by the CW light injection close to the SOA material transparency yields a power-limiting power transfer function [10]. This provides the intensity modulation reduction

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005

that is necessary for generating a packet-level clock signal from the amplitude modulated Fabry-Perot output. Finally, the self-extracted clock packets were amplified in an EDFA and launched into a Dispersion Decreasing Fiber (DDF)-based pulse compressor used at the output of the UNI gate. The active element of the UNI gate was a 1.5 mm bulk InGaAsP/InP ridge waveguide SOA provided by OPTOSPEED S.A. with 27 dB small signal gain at 1550 nm and a recovery time of 80 ps, when driven with 700 mA.

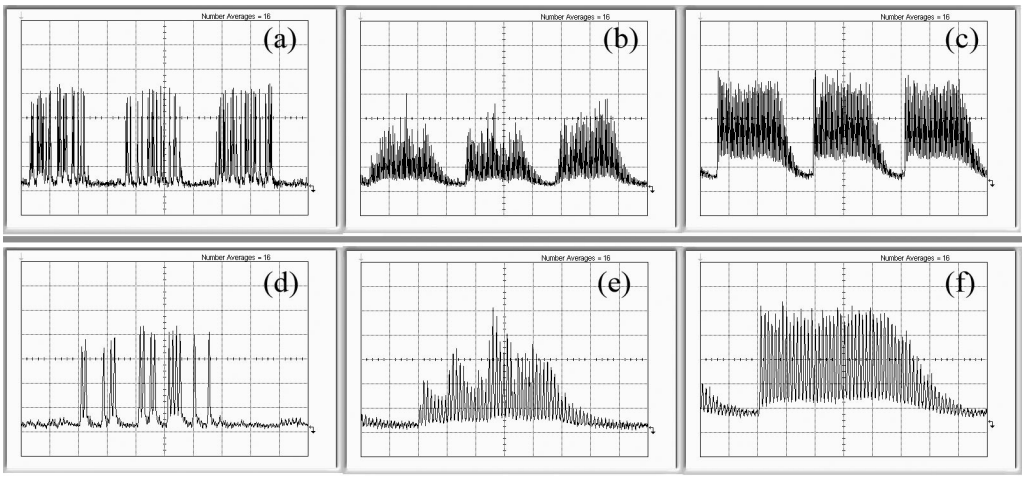


Fig. 2. Pulse traces of (a) three input data packets, (b) corresponding FPF output, (c) recovered clock packets at time base 500 ps/div and (d) single packet, (e) FPF output and (f) single recovered clock packet at time base 200 ps/div. The vertical scale is 335μW/div.

## 4. Results and discussion

The clock recovery circuit was tested using 40 Gb/s short packet traffic. Figure 2(a) shows a typical oscilloscope trace of a sequence of four, 40-bit long packets separated by 750 ps at 40 Gb/s that are used as test signals. Entering the FPF, the packet stream is convolved with the exponentially decaying response function of the filter, so that deeply amplitude modulated, but nevertheless clock resembling packets are obtained as shown in Fig. 2(b). Introduction of this signal as control signal into the saturated UNI gate results in the generation of clock packets with very short rise and fall times as depicted in Fig. 2(c). Figure 2(d), Fig. 2(e) and Fig. 2(f) provide a more detailed view of a single packet, its form after passing through the FPF and its transformation to an amplitude equalized packet clock signal. More specific, Fig. 2(f) reveals that the clock is captured from the first bit and exhibits a fall time of 16 bits, whereas the amplitude modulation (highest to lowest pulse ratio) within the 40 clock pulses is below 1 dB. The sharp rise time is a result of the heavy saturation of the SOA and determines the lock acquisition time of the circuit, whereas the fall time is due to the lifetime of the filter and determines the minimum intra-packet guardbands. Successful operation of the circuit was achieved by injecting 1 mW of optical power from the CW signal and 80 fJ/pulse from the data signal.

The timing jitter performance of the circuit was investigated using a continuous PRBS signal at 40 Gb/s with the precision time base option of an Agilent/HP 86100A Infinium digital sampling oscilloscope. Figure 3(a) and Fig. 3(d) show the eye diagrams obtained for the input signal at 40 Gb/s. The rms timing jitter for the input signal was measured to be 450 fs. Figure 3(b) and Fig. 3(e) show the eye diagram at the output of the FPF showing intense amplitude modulation due to the low finesse of the filter. The reshaping properties of the power-limiting gate is shown in Fig. 3(c) and Fig. 3(f) through the eye diagram of the

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005

recovered clock at 40 GHz with measured timing jitter of 580 fs. The slight increase in rms jitter was due to the difficulty of precisely aligning the bulk FPF used, resulting in small line-rate detuning. This effect can be eliminated by using a fiber-based FPF. The circuit was also sensitive to random phase variations originating from the susceptibility of mode-locked fiber ring lasers to environmental changes. Figure 4(a) shows the optical spectrum obtained at the output of the clock recovery circuit and Fig. 4(b) shows the corresponding autocorrelation trace. The pulses have a temporal FWHM of 4 ps, whereas their hyperbolic secant profile can be verified by the fitting evident in the figure.

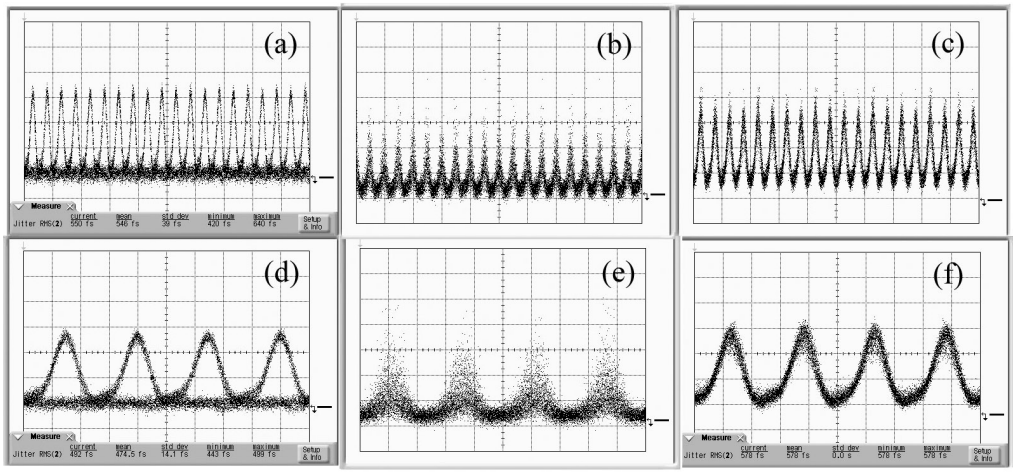


Fig. 3. Eye diagrams of (a) incoming data, (b) FPF output and (c) extracted clock at 50 ps/div and (d) incoming data, (e) FPF output and (f) recovered clock at 10 ps/div. The vertical scale of upper row is 390μW/div and the lower row vertical scale is 500μW/div.

Although the experimental data presented use a $2^7$-1 PRBS, the clock recovery circuit can be designed according to the requirements of the network traffic by tailoring the finesse of the Fabry-Perot filter. For instance, if a PRBS of $2^{31}$-1 is required, the filter should be designed to have a finesse of 80 [9]. In this case, the recovered clock packet would exhibit less than 150 ps lock-in time and a decay time of approximately 2 ns. Finally, since the FPF has over 50 nm of optical bandwidth, the clock recovery circuit is only limited by the gain bandwidth of the SOA used, making the scheme broadband and insensitive to CW laser source wavelength instabilities.

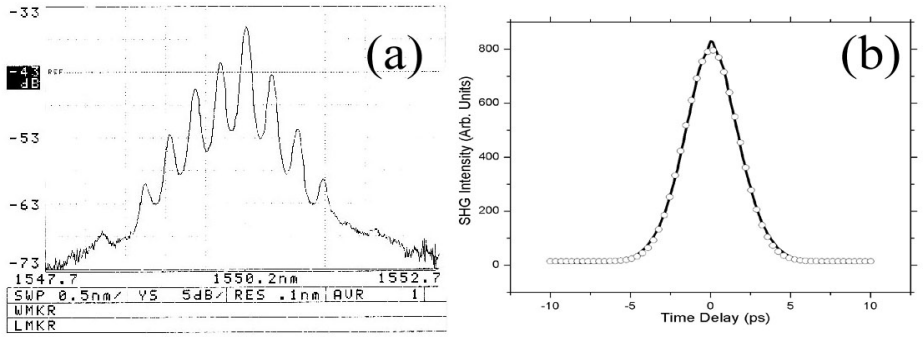


Fig. 4. Recovered clock (a) optical spectrum and (b) autocorrelation trace with sech fitting.

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005

## 5. Conclusion

We have presented a 40 Gb/s all-optical clock recovery circuit capable of operating with very short optical packets, while maintaining low guardband requirements. Clock recovery was successfully demonstrated with 40-bit long optical packets separated by 750 ps without any electronics or synchronization to local oscillators. Instantaneous clock acquisition was achieved and the clock persistence time was 16 bits (400 ps). The proposed circuit is ideal for high capacity all-optical packet-switched networks with high transmission efficiency and very fine granularity.

## Acknowledgements

This work has been supported by the European Commission through projects IST-LASAGNE (FP6-507509), IST-e-Photon/ONe (FP6-001933) and the Netherlands Organization for Scientific Research (NWO) through the NRC Photonics grant. The authors would like to thank J. P. Turkiewicz for the technical help and fruitful discussions.

#5980 - $15.00 US Received 6 December 2004; revised 11 January 2005; accepted 12 January 2005