High-resolution phase shift and digital implementation of a fuel cell powered UPS system

Please check the document version of this publication:

High-Resolution Phase Shift and Digital Implementation of a Fuel Cell Powered UPS System

Haimin Tao, Jorge L. Duarte, and Marcel A. M. Hendrix
Eindhoven University of Technology
Group of Electromechanics and Power Electronics
5600 MB Eindhoven, The Netherlands
Phone: +31 (0) 40 247-3571
Fax: +31 (0) 40 243-4364
Email: h.tao@tue.nl
URL: http://www.tue.nl

Keywords

<<Alternative energy>>, <<Converter control>>, <<DSP>>, <<Fuel cell system>>, <<Uninterruptible Power Supply (UPS)>>.

Abstract

This paper presents the digital implementation of a single-phase fuel cell powered uninterruptible power supply (UPS) and distributed generation (DG) system. The power conditioning unit of the system consists of a voltage source inverter and a three-port bidirectional dc-dc converter interfacing the fuel cell and inverter with a supercapacitor. It is shown that the control of the whole system including both the dc-dc and dc-ac stages can be carried out by a single digital signal processor (DSP). In particular, in order to eliminate limit cycle oscillations in digitally controlled dc-dc converters, the generation of high-resolution phase shifts is explained in detail. The system is suitable for residential applications and can improve the power quality for the local user. Practical design issues such as the state-of-charge (SOC) management of the supercapacitor and prototype design details are discussed. Experimental results from a 3.5 kW prototype are presented to verify the effectiveness of the digitally implemented control scheme.

Introduction

The interest in distributed generation (DG) has increased significantly in recent years. To exploit clean energy generators/resources such as fuel cells, solar and wind energy, zero-emission electric power generation systems have been developed intensively. Of particular interest are fuel cells, which use hydrogen, natural gas, or other fuels to generate electricity without increasing pollution.

On the other hand, the quality of the grid has been degrading over the past decades. Using small/micro DGs (at a power level for home applications) to improve local power quality is a practical solution. DGs also offer peak shaving to reduce the cost of energy and provide uninterruptible power supply (UPS) service during grid outages. Recently, research has been done on the use of fuel cell technology for electricity generation for residential applications [1].

The main topic of this paper is the design issues of a fuel cell powered UPS/DG system, including the digital implementation of the control scheme with a single DSP, especially the generation of high-resolution phase shifts. Thus far, very few publications have adequately presented effective solutions to the digital instrumentation of phase shift, especially to the high-resolution phase shifting.

This paper is organized as follows. First, an overview of the whole power conditioning system will be given. Second, the issue of limit cycle oscillations in digitally controlled systems and the generation of high-resolution phase shifts will be addressed in detail. Third, the digital implementation of the control system with a single DSP will be described. Following that, the control system is verified using the experimental results from a 3.5 kW laboratory prototype. Conclusions will be given in the last place.
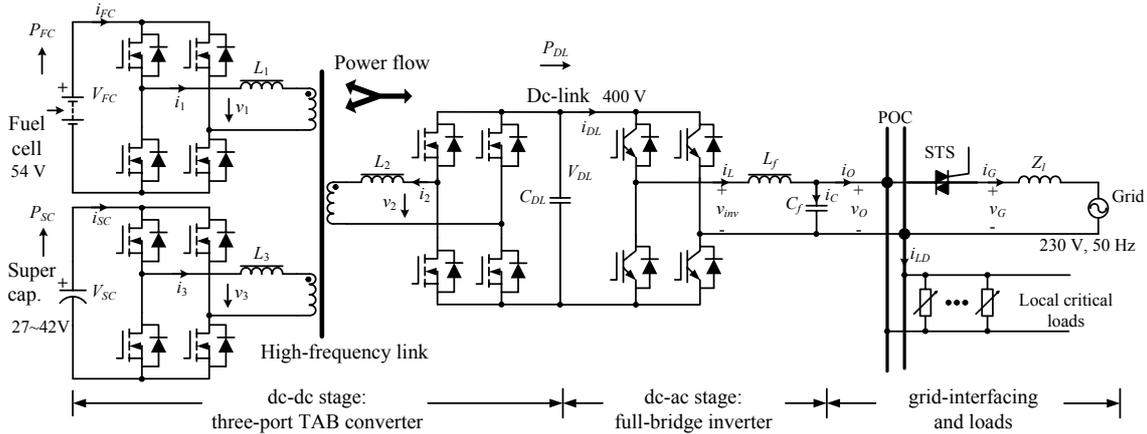
Figure 1: A single-phase fuel cell powered UPS system.

Description of the UPS system

Due to the slow transient response of fuel cells, the implementation of a fuel cell system requires an auxiliary storage device to meet load changes. Therefore the dc-dc stage for a fuel cell system has two power inputs – for the fuel cell and for the storage. A family of three-port converters presented in [2] can be employed. Fig. 1 shows the topology of the fuel cell generation system for residential applications [1]. A three-port converter is used to manage the power flow between the fuel cell, supercapacitor and inverter. The second part of the system is a full-bridge pulse-width modulated (PWM) inverter for grid-interfacing. The inverter ac output is connected to the grid through a static transfer switch (STS) – a triac. Local critical loads are directly coupled to the inverter output at the point of connection (POC).

As shown, the three-port triple-active-bridge (TAB) converter [3], is chosen as the dc-dc stage. In addition to galvanic isolation, a major advantage of this converter is the ease of matching the different voltage levels of the three ports. The leakage inductances are an integral part of the circuit. Each bridge generates a high-frequency square-wave voltage with a controlled phase angle with respect to the primary (fuel cell) side. The control scheme for the dc-dc stage aims at regulating both the dc-link voltage and fuel cell power using the two phase shifts as control variables. Furthermore, by duty ratio control this circuit can also be operated with soft-switching when the port voltage varies [3], [4]. The supercapacitor supplies/absorbs the transient power difference between the inverter and fuel cell. This is an automatic system matching the variations of the power drawn by the inverter while the power delivered by the fuel cell is kept at the same level. The system can operate in both stand-alone and grid-connected modes. By taking advantage of the transient storage capability offered by the supercapacitor, the function of reactive power compensation can be integrated into the system. Simultaneously, the inverter can be operated as an active filter to compensate for the reactive and harmonic current demanded by local loads [1]. Such operation would prevent the power network from being contaminated by local nonlinear loads.

Resolution and limit cycle

Resolution of digital PWM and phase shift

A practical problem that was encountered when implementing the digital control was the occurrence of the limit cycle oscillations (LCO): steady-state oscillations of, for example, the output voltage at frequencies lower than the converter switching frequency. As a result of nonlinear quantization effects in the analog-to-digital (ADC) and digital pulse-width modulator (DPWM) in the control loop, digitally controlled dc-dc converters can exhibit undesired LCO. The problem can also be stated as insufficient time resolution in the digital modulator to satisfy specified output voltage regulation accuracy. The general quantization effects and no-limit-cycle conditions have been extensively analyzed in [5] and [6]. To increase the effective resolution of the DPWM, a few techniques such as dithering, multiphase averaging [5] and so-called cycle-skip [7] can be applied. The cause of LCO with a digital phase shift (DPHS) modulator is similar.

To eliminate LCO, it has to be ensured that under all circumstances there is a quantized steady-state voltage that results in a zero-error value. This can be guaranteed if the resolution of the DPWM is sufficiently higher than the resolution of the ADC. Therefore, in order to retain a sufficiently high DPWM
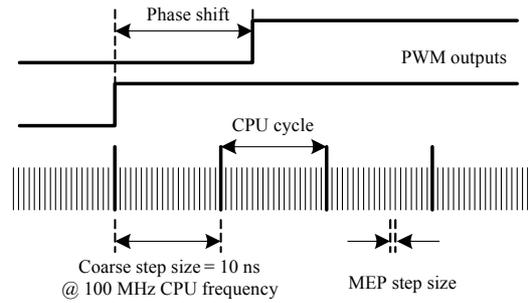
Figure 2: Micro edge positioner (MEP) operation logic.

resolution, the maximum switching frequency is often limited. For the DPHS, the problem of limit cycling is even worse because the phase shift only varies from 0 to $\pi/2$ maximum for the full control range [3]. This is to say, the resolution of the DPHS is a factor of four lower than that of the DPWM for an equivalent situation. This imposes more constraints on the implementation of high-frequency DPHS controlled converters. To be more specific, the following condition has to be met:

$$ N_{DPHS} > N_{ADC} + \log_2 \left(\frac{\pi}{2V_o} \cdot \left| \frac{\partial V_o}{\partial \varphi} \right|_{\varphi=\varphi_A} \right) \tag{1} $$

where V_o is the output voltage; N_{ADC} is the ADC resolution (in bits) of V_o; φ (in radian) is the control variable – the phase shift; and φ_A is the phase shift at the operating point. In short, the resolution requirement is directly related to how sensitive the output is to the change of the control variable.

Furthermore, the inclusion of an integral term in the control law is necessary to eliminate LCO [5]. The digital integrator is intended to fine-tune the output voltage; therefore it has to be able to adjust the phase shift command by steps as small as a least significant bit (LSB). It is recommended simply to use a 32-bit integrator in a 16-bit fixed-point DSP so that an error less than one LSB will not be neglected.

High-resolution phase shift with TMS320F280x DSP

For the three-port TAB converter, the resolution of the phase shift is essential to optimize the converter performance, for example, to minimize the reactive current in the transformer [3]. The effective resolution for the conventionally generated PWM is a function of PWM frequency and system clock frequency:

$$ N_{DPWM} = \log_2 \left(T_{PWM} / T_{SYSCLK} \right) \tag{2} $$

where T_{PWM} and T_{SYSCLK} are the PWM period and CPU clock period, respectively. For example, to generate a 100 kHz switching frequency with a 100 MHz DSP CPU clock, the resolution of the DPWM is 10 bits, while the resolution of the DPHS is only 8 bits, which is insufficient because the ADC usually has more than 10 bits of resolution.

The latest TI C2000 280x digital signal controller offers high-resolution PWM (HRPWM) and phase shift (HRPHS) in its enhanced PWM (ePWM) modules. The HRPWM is based on micro edge positioner (MEP) technology, which can finely position an edge by sub-dividing one coarse system clock of a conventional PWM generator [8]. Fig. 2 shows the coarse system clock and MEP steps. The MEP step is controlled via an 8-bit field in an extension register . The MEP can be programmed to provide precise position control on the rising edge (RE), falling edge (FE) or both edges (BE) at the same time. FE and RE are used for power topologies requiring duty cycle control, while BE is used for topologies requiring phase shifting. By configuring the MEP to BE mode, the built-in MEP unit can achieve a maximum 150 ps resolution phase shift [8], which thereby provides a maximum equivalent 6 bits extra resolution. For 100 kHz switching frequency, the resolution of the phase shift can achieve 14 bits.

Fig. 3 shows the simplified DSP program flow chart to use the HRPHS for a 16-bit fixed-point implementation. The output of the phase shift controller is a 16-bit phase shift value. Then, the low 6-bit value is loaded into the high-resolution phase shift register (TBPHSHR) and the high 10-bit is the regular phase shift value (*phi*). One detail discovered when implementing the high-resolution phase shift is that there is an internal offset of two CPU cycles in the regular phase shift. This can be corrected by subtracting 2 from *phi*. When the counter of the master module reaches zero, all the phase shift modules are synchronized to the master module with the counters loaded with the updated phase shift values. A negative phase shift (i.e., leading the master module) can be realized by setting the direction of counter to
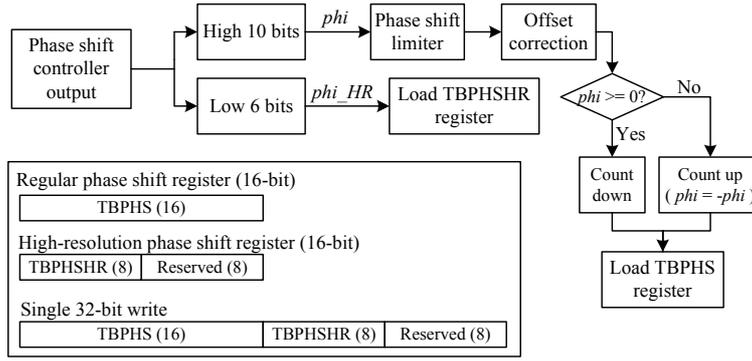
Figure 3: Simplified DSP implementation of the high-resolution phase shifting.
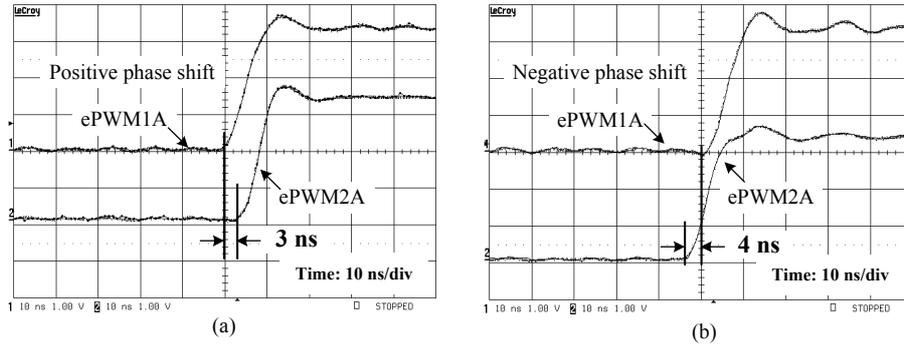

Figure 4: Measurement results of the high-resolution phase shift showing (a) a positive phase shift and (b) a negative phase shift.

count-up (see Fig. 5). Fig. 4 demonstrates the generation of the high-resolution phase shift at a time base equal to the CPU cycle (10 ns/div), where in (a) ePWM2A lags ePWM1A (the reference) by 3 ns and in (b) ePWM2A leads ePWM1A by 4 ns. As can be seen, a very precise phase shifting can be achieved.

Alternatively, the HRPHS can also be used based on a per unit (p.u.) representation of the control variable. It is quite common to express the phase shift command issued by the digital controller in a per unit or percentage basis. For instance, the maximum phase shift ($\pi/2$) can be express as 1.0, then the output of the controller is between 0 and 1. TI provides the IQmath library, which is a collection of optimized mathematical functions to port the floating point algorithm into 32-bit fixed-point code. With the IQmath library, the per unit calculation can be easily implemented. An example of how to use the HRPWM with the per unit representation of the control variable has been supplied by TI in [8]. Similarly, for using the HRPHS, Fig. 5 illustrates the mapping scheme between the per unit phase shift and the value loaded into the register. First, the phase shift is multiplied by the PWM period. The resultant is then divided into the integer part as the quotient which supplies the coarse CPU steps and the fractional part which will be positioned by the MEP logic. Following that, the fractional part is multiplied by the the MEP scale factor *(MEP_SF)*, left-shifted by 8 bits, and added to the rounding constant 0180h. Finally, the result is combined with the integer part to form a 32-bit fixed-point phase shift value which is loaded into the register. It should be noticed that when the phase shift is negative, the absolute value is used, and the fractional part *frac* is corrected as:

$$frac \leftarrow 1 - frac \tag{3}$$

and one is added to the integer part:

$$phi \leftarrow phi + 1. \tag{4}$$

This guarantees a continuous and smooth phase shift in both the positive and negative regions.

Note that the MEP scale factor varies with the system clock and DSP operating voltage and temperature. To solve this problem, TI supplies an optimizing C function which determines the optimal number of MEP steps per CPU cycle according to the CPU operating conditions. As suggested by TI, the scale factor varies slowly over a limited range with the system clock and DSP operating voltage and temperature, so the optimizing C function can be run as a very low priority background routine.
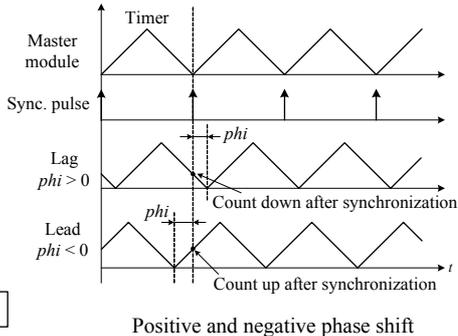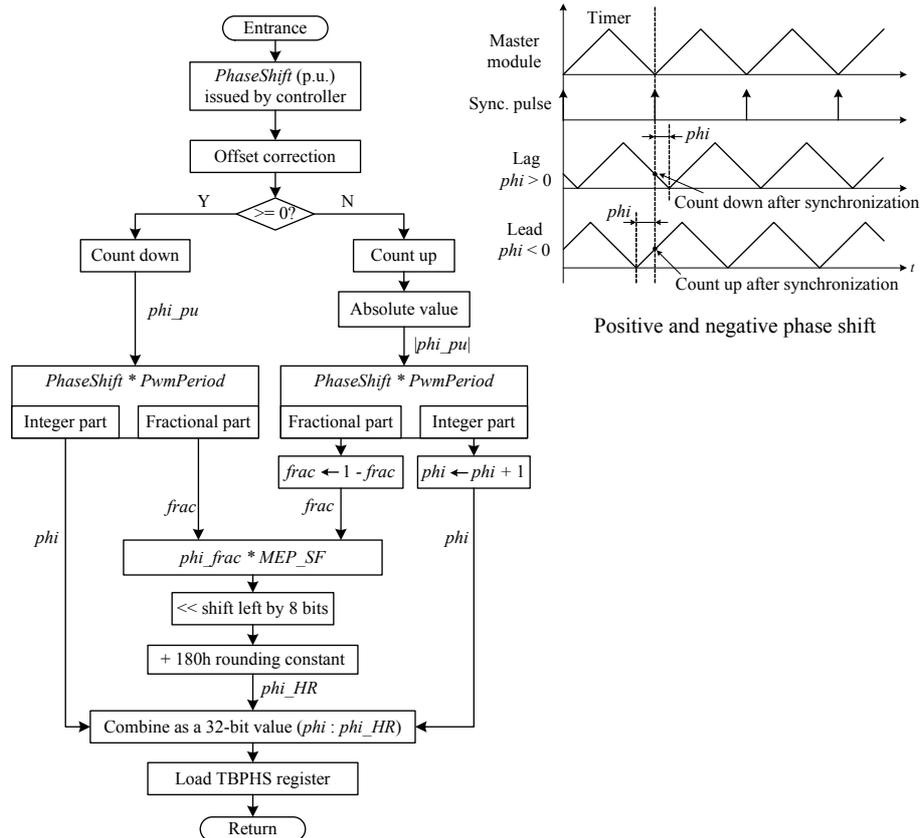
Figure 5: Mapping scheme of the high-resolution phase shifting for a per unit representation of the control variable.

DSP Implementation of the control system

Control of the dc-dc and dc-ac stages

In an attempt to simplify the control design and eliminate the communication overhead between multiple DSPs, both the dc-dc and dc-ac stages are controlled by a single DSP controller (TMS320F2808). The DSP system has six independently configurable ePWM modules (two PWM outputs per module). Each ePWM module can be directly operated in phase shift modulation mode by hardware. There is no need to implement the digital phase shift with a software interrupt routine as presented in [9]. This saves time for the CPU to execute time critical tasks. As illustrated in Fig. 6, out of 12 PWM outputs, eight (ePWM module 1, 2, 3 and 4) are configured in phase shift mode to control the dc-dc stage and the remaining 4 PWMs (ePWM module 5 and 6) are in PWM mode and used for the dc-ac stage control. With the HRPHS the dc-dc stage is operated at 100 kHz switching frequency (a higher switching frequency would also be possible), whereas the dc-ac stage is switched at 20 kHz (maximum frequency for the IGBTs used).

Two ADC sequences (AdcSeq1 and AdcSeq2) are used for the dc-dc stage and dc-ac stage, respectively. The ADC control registers are set up such that the AD conversions are triggered when the counters are zero. As soon as the conversion is complete, the ADC module generates an interrupt. The dc-dc stage interrupt has higher priority than the dc-ac stage interrupt because the dc-dc stage switching frequency is five times higher and thus this interrupt routine is more time critical. The priority arrangement is done by deliberately re-enabling the CPU interrupt at the very beginning of the dc-ac stage interrupt routine so that the dc-dc stage interrupt can be responded to by the CPU when it is busy executing the dc-ac stage interrupt routine. Fig. 7 illustrates the timing of the two interrupt routines and the ADC sampling periods. It can be seen that both stages can be controlled by the DSP. A third interrupt (not shown in Fig. 7) is also enabled for synchronizing the inverter output to the grid voltage, interrupting at 50 Hz only when the system is in the transition of synchronization with the grid voltage.

Fig. 8 shows the timing of the dc-dc stage and dc-ac stage interrupts measured from the experimental prototype. The dc-dc stage interrupt consumes around 50% of the CPU computational power at a sampling frequency of 100 kHz. In grid-connected mode of operation the execution time of the dc-ac stage interrupt routine is longer than in stand-alone mode of operation because of more calculations such as phase-locked loop (PLL), harmonic compensation, inverter current reference calculation, etc.
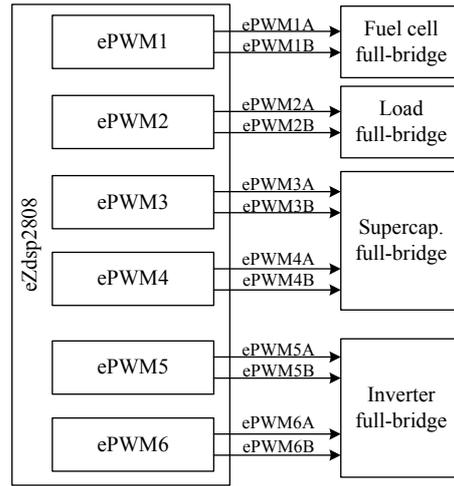
Figure 6: Assignment of the PWM outputs for the control of the whole system.
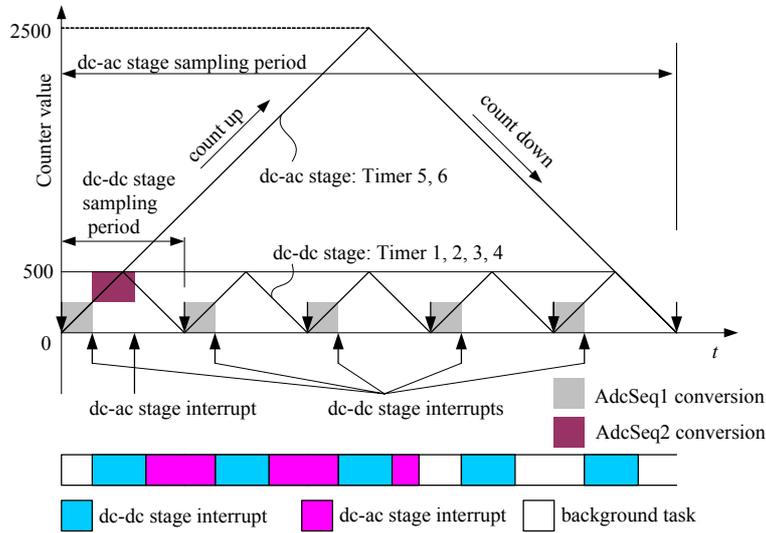

Figure 7: ADC sampling and timing of the two interrupts.

The control scheme for the dc-dc stage (see Fig. 9 [3]) aims at regulating the dc-link voltage V_{DL} and fuel cell power P_{FC} at the same time by controlling the two phase shifts. Two PI controllers are employed, which gives satisfactory dynamic performance [4]. Each controller is programmed with anti-windup protection. The controller is based on a digital approximation of an analog backward Euler scheme. However, the delay of the sample and hold has to be considered. The required phase margin has to be enlarged to cope with such a delay.

State-of-charge (SOC) management of the supercapacitor

Thanks to the direct coupling of the voltage and the SOC of the supercapacitor, the SOC manager can be implemented straightforwardly. Fig. 10 shows the flow chart of the DSP program procedure running as a background task. Since the supercapacitor voltage changes very slowly, the procedure runs about once every 3 second. The supercapacitor voltage is monitored so that it is kept within the allowed operating voltage range. When V_{SC} reaches the maximum or minimum limiting voltage, the fuel cell power P_{FC}^* is slightly adjusted in order to charge/discharge the supercapacitor. The average charging/discharging current can be simply written as

$$I_{SC} = \left(P_{FC}^{**} - P_{Load} - P_{Loss}\right)/V_{SC} \tag{5}$$

where P_{FC}^{**} is the power reference issued by the SOC manager; P_{Load} is the average power consumed by the load during the charging/discharging process; P_{Loss} is the total loss in the system. It should be noticed
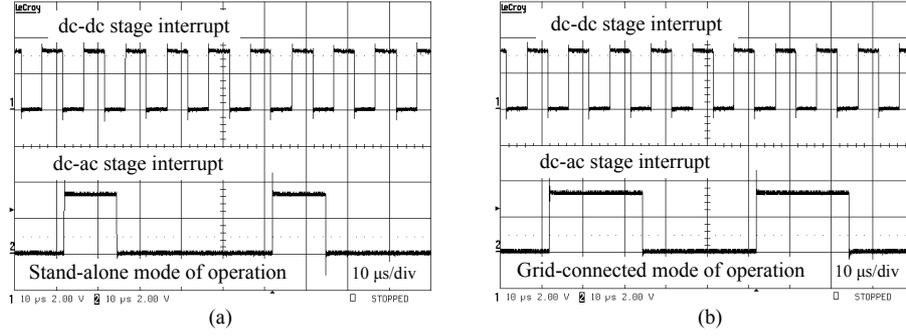
Figure 8: Measurement results of the timing of the dc-dc stage and dc-ac stage interrupts.
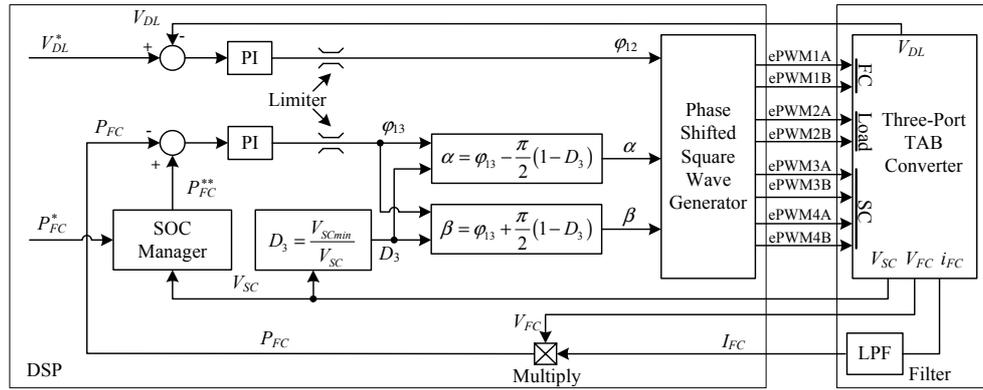

Figure 9: Control scheme for the dc-dc stage – the three-port TAB converter [3].

that a frequent adjustment of the fuel cell power should be avoid in order not to disturb the operation of the fuel cell power constantly. The history value of V_{SC} is stored and compared with the current measurement so that one can determine that the supercapacitor is being charged if V_{SC} increased in the last monitoring period and being discharged if it decreased. Accordingly, the increment/decrement of P_{FC}^{**} should be stopped if V_{SC} is rising/dropping. The step of increment/decrement should be a reasonable value that is sufficient for the requested charging/discharing power and is within the fuel cell limiting power. When P_{FC}^{**} reaches either the maximum or minimum, an error will be issued. The operation of the system will be stopped if V_{SC} reaches its protecting limits.

Prototyping and experimental results

The structure of the 3.5 kW laboratory prototype is illustrated in Fig. 11. As shown, the three full-bridges are linked through the three-winding transformer and inductors. The inverter is connected to the three-port TAB converter at the dc-link capacitor. The DSP based control system samples the operating parameters of both the dc-dc and dc-ac stages and delivers the gating signals to both of them after performing the routines for the closed-loop regulation. The total CPU load for both the dc-dc stage and dc-ac stage interrupts is around 70%.

One challenge in the design of the power stage is that both the fuel cell (54 V) and supercapacitor (42 V) are high-current and low-voltage. To deal with the high current, a novel method was used for the dc-dc stage circuit, as shown in Fig. 12. For each port, five paralleled full-bridge cells are connected together at the input point and are built on the same printed circuit board (PCB); however, the outputs of the bridges are kept separate from each other. The transformer also has five isolated windings in parallel and each of them is connected to a bridge cell. In this way, current is forced to flow through each cell; thereby a better distribution of the current over the five paralleled cells can be achieved.

The fuel cell used in the experiment is a polymer electrolyte membrane (PEM) fuel cell (54 V, 1 kW) from Avista Labs which was originally designed as a battery charger for a 48 V system. The fuel cell was connected in parallel with a 55 Ah 48 V battery bank to increase the total power rating. The supercapacitor from Maxwell has a rated voltage of 42 V and a capacitance of 145 F. The dc-dc stage – the three-port TAB converter – is rated at 3.5 kW (the maximum allowed power for single-phase) and
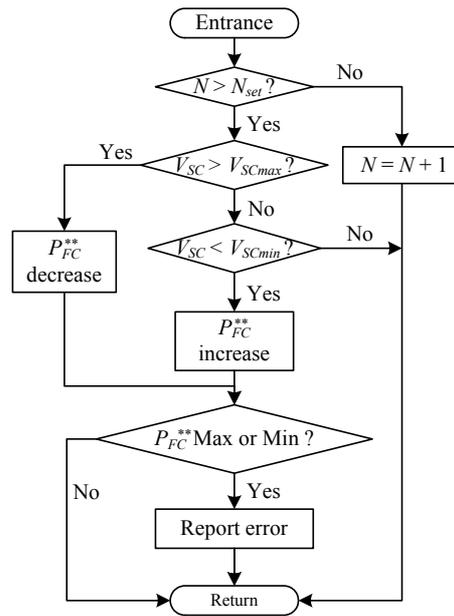
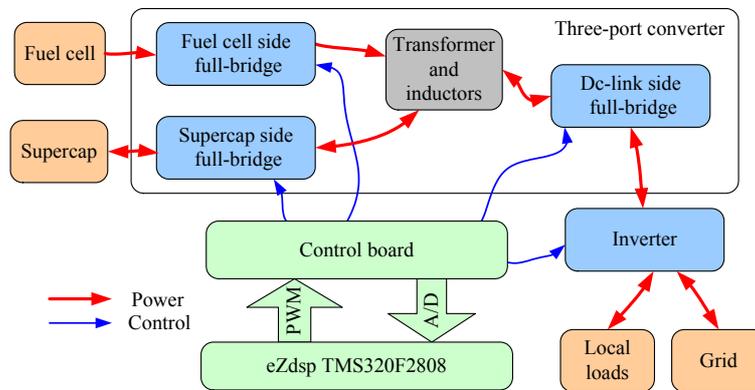Figure 10: DSP routine for the SOC management of the supercapacitor.
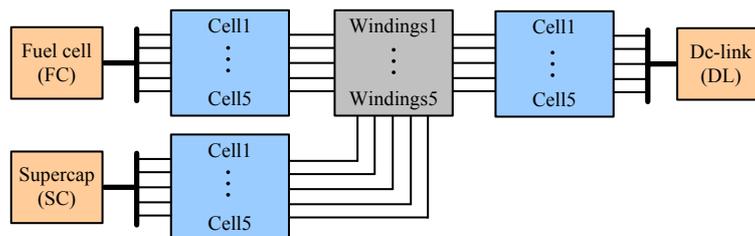

Figure 11: Structure of the 3.5 kW prototype.

Figure 12: Using separately paralleled cells for high-current applications.
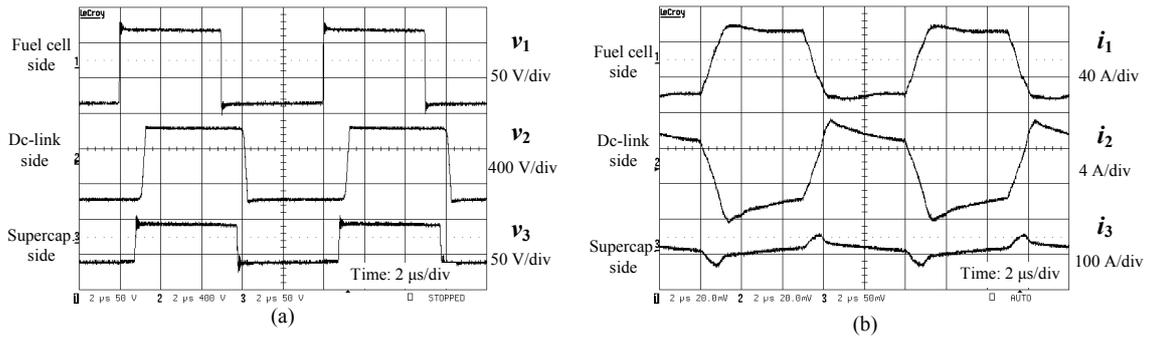
Figure 13: Measurement results of the three-port TAB converter at $\varphi_{12} = 0.2\pi$, $\varphi_{13} = 0.12\pi$, $D_3 = 1$, showing (a) voltages generated by the full-bridges, and (b) currents through the transformer windings.
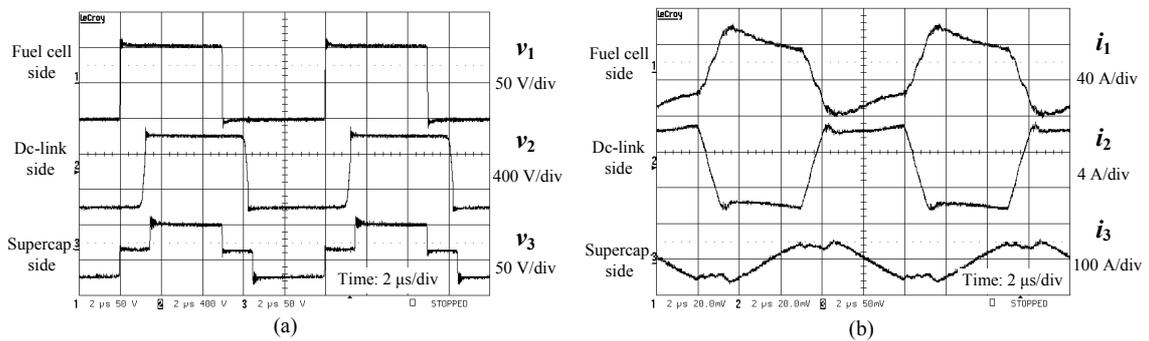

Figure 14: Measurement results of the three-port TAB converter at $\varphi_{12} = 0.2\pi$, $\varphi_{13} = 0.12\pi$, $D_3 = 0.7$, showing (a) voltages generated by the full-bridges, and (b) currents through the transformer windings.

switched at 100 kHz. Fig. 13 ($D_3 = 1$) and Fig. 14 ($D_3 = 0.7$) show the measured voltages generated by the full-bridges and the currents through the transformer windings at the different supercapacitor operating voltages (thus different duty ratios [3]). As shown, because of soft-switching the waveforms are free of oscillations.

The experimental results for grid-connected mode of operation are shown in Fig. 15(a), where a diode rectifier was used as the local load. As shown, the inverter compensates for the reactive and harmonic current of the local load and injects in-phase sinusoidal current into the grid [1]. With the same load, Fig. 15(b) presents the measurement results of the output voltage regulation in stand-alone mode of operation. As shown, the inverter output voltage v_O keeps low distortion.

Photographs of the prototype are shown in Fig. 16. Fig. 16(a) shows the full-bridge circuit with five separately paralleled modules. The two-layer PCB uses thick copper layers (140 μm) to reduce the conducting resistance. The three-port TAB converter is shown in Fig. 16(b), comprising a three-winding transformer, three inductors, and three full-bridge circuits shown in Fig. 16(a). The completely assembled system is shown in Fig. 16(c), where the three-port TAB converter is on the left side and the inverter is on the right side.

Conclusion

In this paper the digital implementation of a fuel cell powered single-phase UPS has been presented. The requirement for the resolution of the phase shift has been analyzed in detail. High-resolution phase shift is implemented with the TMS320F2808 DSP controller, which can achieve a maximum 150 ps resolution. It has been shown that with a proper design it is possible to use a single DSP controller to control and coordinate the dc-dc and dc-ac stages. In addition, a simple method for the SOC management of the supercapacitor by monitoring its terminal voltage was also presented. The digitally implemented 3.5 kW fuel cell UPS system was tested and the measurement results verified the effectiveness of the digitally implemented control system.
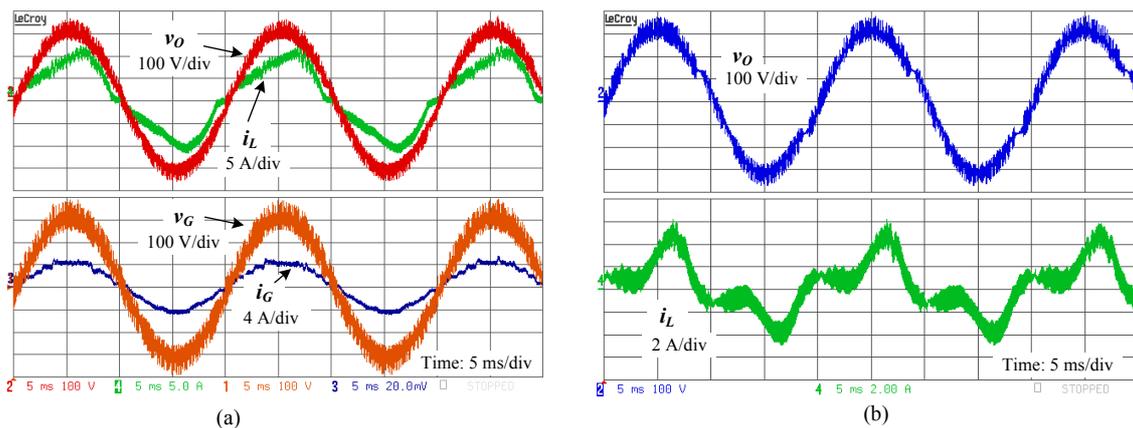
Figure 15: Measurement results of the inverter operation, showing: (a) compensation of the harmonics of the local load (a diode rectifier) and injection of active current to the grid in grid-connected mode of operation, and (b) the output voltage and inductor current in stand-alone mode of operation with a diode rectifier load.
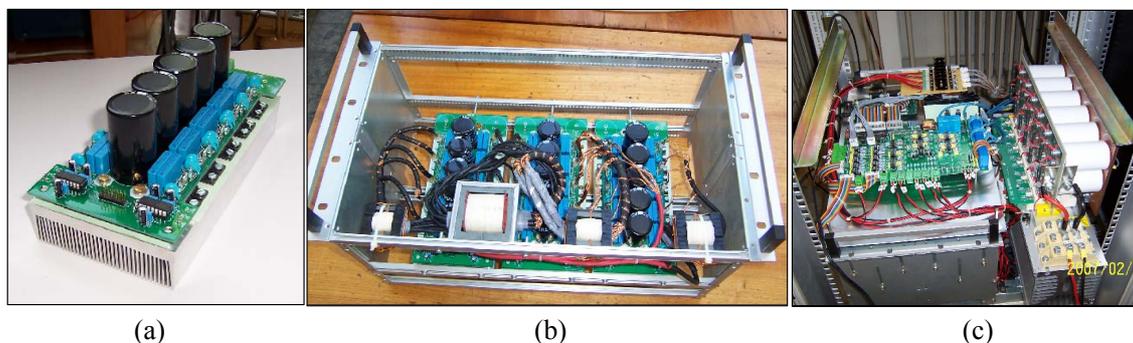

Figure 16: Photographs of the prototype, showing (a) the full-bridge module (3.5 kW, 100 kHz), (b) the dc-dc stage – the three-port TAB converter, and (c) the completely assembled power conversion system.

References

[1] Tao H., Duarte J. L., and Hendrix, M. A. M.: A distributed fuel cell based generation and compensation system to improve power quality, in *Proc. IEEE International Power Electronics and Motion Control Conference (IPEMC'06)*, Shanghai, China, Aug. 2006, pp. 1–5.

[2] Tao H., Kotsopoulos A., Duarte J. L., and Hendrix, M. A. M.: Family of multiport bidirectional DC-DC converters, *IEE Proceeding Electric Power Applications*, vol. 153, no. 3, pp. 451–458, May 2006.

[3] Tao H., Kotsopoulos A., Duarte J. L., and Hendrix, M. A. M.: A soft-switched three-port bidirectional converter for fuel cell and supercapacitor applications, in *Proc. IEEE Power Electronics Specialists Conference (PESC'05)*, Recife, Brazil, June 2005, pp. 2487–2493.

[4] Tao H., Duarte J. L., and Hendrix, M. A. M.: Transformer-coupled multiport ZVS bidirectional DC-DC converter with wide input range, *IEEE Transaction on Power Electronics*, to be published.

[5] Peterchev A. V. and Sanders S. R.: Quantization resolution and limit cycling in digitally controlled PWM converters, *IEEE Transaction on Power Electronics*, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[6] Peng H., Maksimovic D., Prodic A., and Alarcon E.: Modeling of quantization effects in digitally controlled DC-DC converters, in *Proc. IEEE Power Electronics Specialists Conference (PESC'04)*, Aachen, Germany, June 2004, pp. 4312–4318.

[7] Chen J., Ribeiro M., Payseo R., Zhou D., Smith J. R., and Kernahan K.: DPWM time resolution requirements for digitally controlled DC-DC converters, in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC'06)*, Dallas, TX, Mar. 2006, pp. 1127–1132.

[8] *High-resolution pulse width modulator (HRPWM) reference guide*, Literature Number: SPRU924, Texas Instruments, Apr. 2005.

[9] Tao H., Kotsopoulos A., Duarte J. L., and Hendrix, M. A. M.: Design of a soft-switched three-port converter with DSP control for power flow management in hybrid fuel cell systems," in *Proc. 11th European Conference on Power Electronics and Applications (EPE'05)*, Dresden, Germany, Sept. 2005, pp. 1–10.