An RX AFE With Programmable BP Filter and Digitization for Ultrasound Harmonic Imaging

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Abstract—This paper presents a front-end integrated circuit for ultrasound (US) harmonic imaging, interfacing to a one-dimensional capacitive micromachined ultrasonic transducer (CMUT). It contains a complete ultrasound receiving chain, from analog front-end (AFE) to gigabit/s data link. A two-stage self-biased inverter-based transimpedance amplifier (TIA) is proposed in this work to improve tradeoffs between power, noise, and linearity at the first stage. To improve harmonic imaging performance, the design is further equipped with a 4th-order highly programmable bandpass filter, which has a tunable bandwidth from 2 MHz to 15 MHz. An 8 b 80 MS/s SAR ADC digitizes the signal, which is further encoded and serialized into an LVDS data link, enabling a reduction in the number of output cables for future systems with multiple ADCs. The design is realized in a 40 nm CMOS technology. Electrical measurements show it consumes 2.9 mW for the AFE and 2.1 mW for the ADC and digital blocks. Its overall dynamic range varies from 61 dB to 69 dB, depending on the reception bandwidth. The imaging capability of this design is further demonstrated in a US transmission and reception imaging system. The acoustic measurements prove successful ultrasound harmonic acquisition, where the on-chip bandpass filter can improve the lateral resolution by more than 30%.

Index Terms—CMUT, front-end, inverter-based amplifier, RX, TIA, ultrasound harmonic imaging system.

I. INTRODUCTION

ULTRASOUND harmonic imaging (UHI) is becoming an essential medical modality in routine clinical diagnosis, especially for detecting the nonlinear responses from contrast agents in contrast-enhanced ultrasound imaging [1], [2]. Unlike conventional ultrasound fundamental imaging (UFI), the transmission (TX) and reception (RX) operate at a different frequency in this approach. In the TX, the transducer is usually excited by a pulse at the fundamental frequency ($f_0$). During wave propagation in a medium, nonlinear objects such as contrast agents will generate harmonic components. In the RX, multiple harmonic, sub-harmonic, or ultra-harmonic components $n \times f_0$ ($n = 0.5, 1.5, 2, 3,...$) can be received combined with the fundamental component ($f_0$). The harmonic signals can be further isolated from the fundamental component to make images. Compared to UFI, UHI can offer advantages such as better spatial resolution and contrast-to-tissue ratio [3], [4].

Fig. 1 shows a typical US RX system with digitization, which is widely adopted in UFI systems [5], [6]. Many transducer elements (e.g., $N = 128$) are often required to achieve sufficient image resolution. Compared to a typical UFI system, there are several significant differences in the design strategy for a UHI system:

(i) Dynamic range (DR) for harmonic signals. Typically, to improve the dynamic range of a US RX chain, variable gain stages are used to monitor small and large signals dynamically from different imaging depths [7]. This can help to relax the required dynamic range of the analog to digital converters (ADCs). However, in UHI, the fundamental signal usually has larger power and may limit the amplification of weak harmonic signals. To alleviate this issue, according to our previous study [8], medium order bandpass (BP) filtering can help to suppress the unwanted fundamental signal at an early stage, thereby enabling more gain at the harmonic frequencies, which should be realized in the hardware domain.

(ii) Linearity. In UFI systems, the linearity requirement of RX circuitry is often relaxed to around −45 dB HD2/HD3 or less, since the harmonic distortions are not of interest and can be filtered out later if they are out-of-band [6], [9], [10]. However, in UHI, the received harmonics are of primary interest. Therefore, distortion introduced by the electronics should be suppressed to a lower level compared to the received harmonic signals.

(iii) Flexibility. In UHI, the optimal TX frequency depends on the image objects. For example, in contrast-enhanced ultrasound imaging, the TX frequency should preferably match...
the resonance frequency of the microbubbles, which can be between 1 MHz and 10 MHz [11], [12] for different contrast agents in terms of size and shell. The optimal harmonic RX band, thus, depends on the TX frequency as well. In this respect, the RX electronics need to be versatile and thus should feature programmable bandwidth (BW).

In the signal processing domain, BP filtering has been known as one of the imaging techniques for UHI [14], but it involves inherent trade-off between contrast and axial resolution. Other imaging techniques are also known, such as pulse inversion [15], [16]. In this approach, two excitation pulses with inverted amplitudes are sent to the medium, enabling the extraction of even-order harmonics by summing the corresponding echoes, without loss of RX bandwidth. As an illustration for this comparison, an exemplary simulation based on a 128-element transducer is shown in Fig. 2(a). A plane-wave acoustic field is generated based on the k-Wave toolbox [17]. A point scatter is positioned at 25 mm depth in a homogeneous medium to analyze the spatial resolution. Spatial resolution are then compared based on the resulted images, as shown in Fig. 2(b). The BP filtering at the third harmonic gives the best lateral resolution (LR) in this case, while the pulse inversion technique maintains the best axial resolution (AR) compared to the original image. To the best of our knowledge, this paper shows BP filtering implemented in the AFE circuitry for the first time in literature. By this way, one can achieve the lateral resolution improvement provided by BP filtering. Furthermore, the dynamic range specifications for the backend electronic chain are relaxed when compared to a digital BP filter or a pulse inversion scheme [8].

The system in this work adopts a one-dimensional (1-D) capacitive micromachined ultrasonic transducer (CMUT) array. CMUT technology can provide a tunable center frequency by changing the DC bias voltage [18], thus offering adjustable bandwidth, which is preferred in UHI. However, the main physical limitation for this 1-D CMUT is its relatively large parasitic capacitance [19]–[21] due to the large element size, which tends to limit the bandwidth and noise performance of the RX electronics [22]. Therefore, the low noise amplifier (LNA) in the front-end that interfaces with the CMUT element needs to be optimized accordingly.

The design is implemented in a low-voltage (LV) 40 nm CMOS technology, since it offers better digital performance and efficiency, and enables in the future the integration of e.g. on-chip memory, digital beamforming, processing, and data reduction. By separating transducer elements into TX/RX subsets [5], [23], [24], the RX system can be fully implemented in a LV die with no need for a TX interface. As a prototype for demonstration, this work mainly focuses on a single-channel RX front-end design in LV technology. In terms of circuit implementation, a new two-stage self-biased inverter-based transimpedance amplifier (TIA) is adopted to enable an optimal balance between power, noise, and linearity. Besides, the front-end design includes a highly programmable BP filter for the purposes mentioned previously. Further, an 8-bit ENOB successive-approximation register ADC (SAR ADC) is adopted. It is followed by a serialization encoder and a gigabit/s LVDS data link [23] as a first step to reduce output cable count.

The rest of this paper is organized as follows. Section II describes the system overview, Section III shows the circuit optimization and implementation details, and Section IV provides the electrical and acoustic measurement results. Conclusions are drawn in Section V.

II. SYSTEM OVERVIEW

A. Transducer

The front-end circuits presented in this work are designed for a 1-D CMUT array with a pitch size of 102 μm. Each CMUT element is provided with an individual top electrode while sharing one common bottom electrode, as shown in Fig. 3(a). The CMUT element operates in collapse mode when a high voltage DC bias is applied between the two electrodes. The average collapse voltage of this CMUT is about 50-60 V. Its center frequency is roughly proportional to the DC bias voltage, as shown in Fig. 3(c). Therefore, by setting its DC bias at different levels, the CMUT can roughly cover a bandwidth from 3 MHz to 18 MHz.
To build a US TX/RX imaging system, the CMUT array is connected in an interleaved TX/RX configuration, as shown in Fig. 3(a). The odd elements are excited by high-voltage (HV) pulses (tens of volts) during TX. The even elements are used for reception only; thus, they can be connected to a LV chip with no TX interface. Thanks to the tunable bandwidth of the CMUT elements, it is in principle possible to use a lower bias voltage for TX, which enables low frequency excitation in UHI, while the DC bias voltage for the RX elements can be made higher, resulting in better reception of the high-frequency harmonic echoes. However, due to the shared bottom electrode (Fig. 3(a)), this implies that the different TX and RX biases should be applied at the top electrodes, and thus the AC signals should be read out via AC coupling capacitors ($C_{ac}$), as shown later. If an identical DC bias is always preferred, this can be applied via the bottom electrode, such that these coupling capacitors can be omitted.

The equivalent circuit model of a CMUT element is shown in Fig. 3(b). A Butterworth-van-Dyke (BvD) model is used to capture the main mechanical vibration response with the series RLC branch ($R_m$, $C_m$, $L_m$), and the electrical parasitic capacitance ($C_e$) between the transducer electrodes [25]. At the resonance frequency, the CMUT impedance model can be further simplified to $R_m = 4k\Omega \parallel C_e = 25pF$, where $R_m$ determines the intrinsic thermal noise added by the transducer. Due to the physical structure of the CMUT, the impedance is dominated by $C_e$ even inside the passband.

### B. Architecture Overview

Fig. 4 shows the implementation of the overall system. It consists of two main parts: analog blocks (TIA, filter/amplification stages, and a single-ended to differential converter or S2DC), and an ADC with digital backend blocks (serialization encoder, LVDS data link, and CLK divider).

Due to absorption and scattering, US signals will experience attenuation during propagation, which is proportional to the signal frequency and depth [13]. The attenuation in a round trip can be derived as (1):

$$\text{Attenuation in dB} \approx 2 \times \text{Frequency} \times \text{Depth} \times \alpha,$$

where $\alpha$ is the attenuation coefficient. For example, assuming a medium with $\alpha$ of 0.5 dB/cm/MHz and an image depth of 5 cm, the US signals at 3 MHz and 9 MHz would experience a different attenuation of 15 dB and 45 dB, respectively. The large fundamental component limits RX gain and thus makes recovery of the weak harmonic component difficult, but this can be alleviated by a filter. In this example, a 2nd-order HPF at 8 MHz can suppress the components at 3 MHz by about 17 dB relative to 9 MHz and enables further amplification of the 9-MHz component. Considering this, a 2nd-order high-pass filter (HPF) and a 2nd-order low-pass filter (LPF) are implemented in the analog front-end (AFE) after the TIA.

Two programmable gain amplifiers (PGAs) are implemented after each filter and are also used as a discrete-time gain compensation amplifier by suitably changing their gain. A SAR ADC is used to digitize the RX signals locally. Its sampling frequency ($F_s$) is 4× of the maximum RX bandwidth (about 20 MHz), to enable relaxed anti-aliasing and to provide sufficient time delay for beamforming [26]. The ADC output codes are serialized by an encoder and then transferred using a gigabit/s LVDS data link.

### III. CIRCUIT IMPLEMENTATION

#### A. TIA Design Methodology

The LNA is typically the most critical block in a US RX chain. In terms of performance, the LNA needs to provide good noise efficiency and enough gain to suppress the noise from the later stages. To represent the acoustic input, an input voltage source ($V_{in}$) can be added in series with the RLC branch, as shown in Fig. 5(a).

The optimization of the LNA strongly depends on the transducer characteristics. Three popular LNA architectures from literature are compared in Fig. 5(b): resistive-feedback TIAs (RF-TIAs) [5], [6], [9], [22], [27], [28] capacitive-feedback TIAs (CF-TIAs) [29], [30] and capacitive-feedback voltage amplifiers (CF-VAs) [10], [24]. In the following comparisons, the operational transconductance amplifiers (OTA) in the three LNAs are assumed to have sufficient bandwidth and open-loop gain to ensure accurate feedback. The closed-loop gain coefficients are determined such that the maximum in-band magnitudes of the frequency response are the same for the three LNAs.

Fig. 6 shows the normalized RX transfer function for the three LNAs, calculated from the input voltage source $V_{in}$ to the LNA outputs. Both CF-TIA and CF-VA provide low-pass responses.
Fig. 4. Implementation of the overall system: (a) AFE and (b) ADC + digital blocks.

Fig. 5. (a) CMUT model and (b) LNA architectures in literature.

Fig. 6. Normalized RX transfer function for three types of LNA.

with low corner frequencies due to either the feedback capacitor ($C_f$) in the CF-TIA or due to the large electrical capacitor ($C_e$) at the input of the CF-VA. The RF-TIA shows a bandpass frequency response centered at the transducer resonance frequency. Therefore, the RF-TIA yields an increased sensitivity at high frequencies compared to the CF-TIA and CF-VA, and it is preferred for high-frequency applications [30].

The noise performance of the three LNAs is evaluated based on the calculated noise figure (NF). The transducer impedance is approximated by $Z_s = R_m \| (sC_e)^{-1}$ to simplify the results. The input-referred voltage noise of the OTA is represented by $V_{n,amp}^2$. The NF of each LNA can be derived as:

$$NF_{RF-TIA} \cong \frac{4kT}{R_m} + \frac{4kT}{R_f} + \frac{V_{n,amp}^2}{Z_s (sC_e)^{-1}}$$

$$NF_{CF-TIA} \cong \frac{4kT}{R_m} + \frac{V_{n,amp}^2}{Z_s (sC_f)^{-1}}$$

$$NF_{CF-VA} \cong \frac{4kT}{R_m} + \frac{V_{n,amp}^2}{Z_s (sC_e)^{-1}}$$
Fig. 7. Calculated noise figure vs. $G_m$ for three types of LNA.

$$NF_{CF-V A} \approx \frac{4kT}{R_m} + \frac{V_{n,amp}^2}{|Z_S|^2} \left( 1 + \frac{C_f}{C_i} \right)^2,$$

for $(sC_i)^{-1} \gg Z_s$, \hfill (4)

where $k$ is Boltzmann’s constant and $T = 300$ K the absolute temperature. $V_{n,amp}^2$ can be further estimated by $4kT\gamma/G_m$, where $\gamma$ is a proportionality constant. Since the NF is frequency-dependent, to simplify calculations, we compare the NF at the resonance frequency (around 8 MHz) with $\gamma = 1.2$ for a differential-input design. Fig. 7 shows the calculated NF vs. $G_m$ for the three LNAs. The CF-TIA and CF-VA show similar results since $V_{n,amp}^2/|Z_S|^2$ dominates the input-referred current noise from the OTA, as shown in (3) and (4). With a high $G_m$, the RF-TIA has a slightly worse NF due to additional thermal noise from the feedback resistor ($R_f$). The plot in Fig. 7 can also be interpreted as NF vs. power since $G_m$ directly correlates to power consumption. When $G_m > 20$ mS, the NF only improves slowly with $G_m$, which is hence less power-efficient. Considering the tradeoff between power and noise, the design presented in this paper targets a $G_m$ of about 10 mS. As a result, the three LNAs show comparable NF performance. Thus, based on the higher sensitivity provided at high frequency, the RF-TIA is selected as the optimal choice for this design.

It is worth mentioning that: (i) the noise figure of the RF-TIA will further degrade when $R_f$ is reduced; (ii) the noise performance for all three LNAs can be remarkably improved if the electrical parasitic capacitance ($C_e$) is reduced; and (iii) any additional parasitic capacitance at the LNA input increases the current noise contribution from the OTA.

B. AFE

As discussed, a single-ended RF-TIA is chosen to sense the input current from the top electrode of this CMUT transducer. The TIA is designed with three feedback gain settings of 8 kΩ, 16 kΩ, and 32 kΩ. Suitable feedback capacitors are connected in parallel to each resistor to keep the TIA bandwidth around 20 MHz and ensure its stability [22]. Core amplifiers are typically implemented as single-stage amplifiers in most designs using HV processes [6], [10], [24], [30]. However, this approach is not suitable for the large DC gain and dynamic range required in this work. A two-stage amplifier (Fig. 8) is thus implemented here to enhance open-loop gain and improve linearity. In the first stage, an inverter-based differential pair $(M_1-M_4)$ is employed to boost the $G_m$ and save power. The input pair is biased in the sub-threshold region for best $G_m$ efficiency. With a tail current of around 500 $\mu$A, a total $G_m$ around 12 mS is achieved according to simulations. A cross-connected self-biased common-mode feedback (CMFB) is adopted ($M_{5,6}$) in the first stage. The output common mode of the inverter is determined by the gate-source voltage of PMOS transistors $M_{5,6}$ and thus by the biasing current. Compared to the multi-stage inverter-based amplifier used in [5], [29], this architecture requires no extra active CMFB.

The second stage of the TIA is based on a modified common-source amplifier with a current mirror load. The biasing current in this second stage is mirrored from transistors $M_{5,6}$, while at the same time, the AC output of the first stage is also provided to the gates of $M_7$ and $M_8$. Therefore, the second stage requires no extra tail transistor for current biasing, which maximizes the output swing. All PMOS transistors are dimensioned with the same width/length to ensure matching. One limitation of this architecture is that the self-biased PMOS transistors $M_{5,6}$ may be cut off under a large output swing, yielding poor linearity. When used in a feedback amplifier, this is overcome thanks to the gain provided by the second stage. The common mode at the output is set by applying a mid-supply voltage ($V_{cm}$) to the non-inverting input.

Simulated with the proposed transducer input model, the TIA maintains a typical phase/gain margin of 57°/27 dB at lowest gain. The expected output swing of this TIA is about 400 mVpp, which reaches $-1$ dBFS at the ADC input after an additional 6 dB gain by the S2DC. Over process corners and temperatures (0 °C to 85 °C), the post-layout simulations show that it can maintain a HD2/HD3 better than $-50/-54$ dB.

The BP filter is realized by implementing two separate 2nd-order active filters, based on the well-known multiple feedback topology [31], as shown in Fig. 4. The feedback architecture provides enough linearity performance. Both HPF/LPF are designed with a Q factor of 1, enabling a flat transfer function in-band. Each of them has an 8-bit control code that can set different capacitor values for bandwidth selection. The high-pass corner can be programmed from 3 MHz to 14 MHz, and the low-pass corner can be set from 6 MHz to 18 MHz. This enables large flexibility in the choice of bandwidth and center frequency according to the signals of interest.

The two capacitive-feedback PGAs have gain settings of 0 dB, 6 dB, and 12 dB, with a minimum bandwidth around 20 MHz at highest gain. A pseudo-S2DC is implemented to
Fig. 9. Circuit implementation of the core amplifier in the other blocks.

drive the differential ADC inputs, providing a fixed 6 dB gain. A traditional two-stage amplifier (Fig. 9) is used for the HPF, LPF, PGA1, PGA2, and S2DC.

C. ADC + Digital Blocks

A SAR ADC is implemented after the AFE. The ADC clock of 80 MHz is generated from a 1.28 GHz external clock by a 16 × clock (CLK) divider, as illustrated in Fig. 4. An asynchronous timing circuit and comparator are implemented, which eliminate the need for high speed internal clocks. The ADC has 8 b resolution plus 1 b redundancy and thus produces 9 output bits. The extra redundancy bit is placed after 5 most significant bits, and can compensate for dynamic errors before that bit decision [32]. The ADC is a modified version of our previous work [33]. Thanks to the custom-designed delta-capacitors, the total input sampling capacitor seen by the AFE is less than 150 fF with an effective LSB capacitor of 0.4 fF. The differential input range of the ADC is about 900 mVpp due to the DAC implementation, which relaxes the gain requirements of the AFE.

To reduce the number of digital output cables, a serialization encoder is implemented as shown in Fig. 4. The ADC’s 9 parallel bits are first encoded to make each individual code DC free (enabling AC-coupled transmission) and to enable clock and data recovery at the receiving side. For simplicity of implementation, a 9-to-16 b encoder was designed in this prototype, while the serialization is done by a multiplexer running at 1.28 GHz. In the future, a more efficient coding scheme such as 9-to-10 b could be used, reducing the data rate and potentially also the datalink power consumption. Flipflops are inserted after the ADC, the encoder, and the multiplexer, to pipeline the operation and avoid glitches. An LVDS data link then transmits the serial outputs. The bias current of the LVDS driver can be programmed for differential swings from 100 mVpp to 700 mVpp in a 100 Ω differential load.

IV. MEASUREMENT RESULTS

The design was fabricated in a standard 40 nm CMOS technology. Fig. 10 shows its die micrograph. In the floor plan, the AFE and the ADC (with decoupling caps) fit into a 100 μm height, which is compatible with the CMUT pitch size (102 μm), enabling a future array implementation.

Two setups are used to investigate the performance. Firstly, its electrical performance (Section IV.A) is characterized in terms of transfer function, noise, linearity, etc. An off-chip transducer equivalent capacitor (25 pF) is added at the TIA’s input for all electrical characterizations. Besides ADC digital outputs, the chip is also equipped with analog outputs from the S2DC such that the AFE performance can be measured stand-alone. For measurements that require an input signal, a test current is generated by applying a sinusoidal voltage to a 4 kΩ resistor, mimicking the transducer input current. Thus, the noise contribution from the 4 kΩ resistor is included, for example, in the SNR/SNDR/DR measurements.

In the second setup, an extensive acoustic characterization is carried out with a CMUT transducer (Section IV.B). A prototype US TX/RX system is built on a custom-designed PCB.

A. Electrical Measurements

Fig. 11 shows the measured AFE transfer function based on the AFE’s analog outputs. The BP filter is programmed at the full band (3-18 MHz). With different combinations of TIA/PGA gains, the overall AFE gain ranges from 84 dBΩ to 108 dBΩ. The BP filter can be programmed to different high-pass and low-pass corners. Several examples of this are shown in Fig. 12.

The AFE stand-alone noise performance is measured based on the analog outputs. Fig. 13 illustrates the result at highest TIA/PGA gain and full RX band. The integrated in-band input-referred noise (IRN) is 12.0 nArms, which gives a noise figure of 5.2 dB referred to the thermal noise level of a 4 kΩ resistor. When programmed at the lowest gain, the AFE has an in-band IRN of 26.1 nArms as shown in Table I.
Fig. 12. Measured AFE transfer function with different bandwidth settings at lowest gain.

Fig. 13. Measured AFE IRN spectrum at highest gain.

Fig. 14. Measured output spectrum of the RX chain based on AFE analog outputs after noise averaging at highest gain.

Fig. 15. Measured output spectrum of the RX chain based on ADC outputs with 65536 samples at highest gain.

The linearity performance of the RX chain is evaluated at full RX band, which is the most severe case in practical applications. A sinusoidal input signal of about 6 MHz is applied, introducing both second and third harmonic distortion (HD2 and HD3) inside the passband. The input signal amplitude is chosen to produce the maximum signal swing at the ADC input: it is thus set to $16.5 \mu A_{rms}$ and $1.04 \mu A_{rms}$ for lowest gain and highest gain, respectively. At highest gain setting, the output noise is dominated by the thermal noise from the AFE and the linearity performance is the most stringent for this design. Fig. 14 shows the output spectrum of the RX chain based on the AFE analog outputs at highest gain. It achieves an HD2/HD3 of $-60.7/-58.4 \text{ dB}$. Fig. 15 shows the output spectrum of the RX chain based on the ADC outputs at the highest gain. The entire RX chain achieves an in-band SNR/SNDR of $36.3/36.1 \text{ dB}$. The HD2/HD3 performance decreases to $-53.5/-53.1 \text{ dB}$. More disturbances are observed, which degrade the linearity performance. As the amplitude of these disturbances is related to the biasing current of the LVDS driver, they are most likely signal-dependent high-order harmonics caused by digital interference. It is also observed that the AFE becomes more sensitive to disturbances at higher gain settings, which indicates a coupling path from the LVDS driver to the AFE input, for instance caused by the pad ring or the measurement setup. Nonetheless, the SFDR is still better than 53 dB.

### TABLE I

**PERFORMANCE OVERVIEW**

| Supply | 1.1 V |
| Technology | 40 nm CMOS |

| AFE Power | 2.9 mW |
| Active area | $100 \times 230 \mathrm{ \mu m} \times \mathrm{ \mu m}$ |
| TIA gain range | 8/16/32 kΩ |
| PGA gain range | 0/6/12 dB |
| PSRR * | 25.4 dB @ 10 MHz |
| Noise figure | Highest gain 5.2 dB, Lowest gain 10.8 dB |
| ORN | $3.2 \mathrm{ mV}_{\text{rms}}$, $44.07 \mathrm{ mV}_{\text{rms}}$ |
| IRN | $12.0 \mathrm{ nA}_{\text{rms}}$, $26.1 \mathrm{ nA}_{\text{rms}}$ |
| HD2 | $-60.7 \text{ dB}$, $-66.6 \text{ dB}$ |
| HD3 | $-53.4 \text{ dB}$, $-60.7 \text{ dB}$ |

ADC + digital blocks

| Power | 2.1 mW |
| Active area | $40 \times 80 \mathrm{ \mu m} \times \mathrm{ \mu m}$ (ADC), $60 \times 160 \mathrm{ \mu m} \times \mathrm{ \mu m}$ (digital interface) |
| ADC Fs | 80 MHz |
| ADC ENOB | 8.0 bit in-band |

| Overall Power | 5.0 mW |
| Dynamic range | $60.5 \text{ dB} @ 3-18 \text{ MHz}$ |
| $69.3 \text{ dB} @ 11-13 \text{ MHz}$ |
| HD2 | $-53.5 \text{ dB}$, $-66.6 \text{ dB}$ |
| HD3 | $-53.1 \text{ dB}$, $-60.7 \text{ dB}$ |

*Referred to the AFE input.

*Measured based on AFE analog outputs.

*Measured based on ADC outputs.

Therefore, signals from each element can be entirely digitized for post-processing, while the overall output data rate can be reduced by a factor of 16. A commercial FPGA is programmed to control the TX/RX operation. The LVDS outputs are first received by the FPGA and then transferred to a PC. Image reconstruction is further realized offline based on the digitized data.

To perform US imaging, the CMUT is immersed in a water tank as shown in Fig. 19. A phantom with three copper wires (300 μm diameter) is placed at a depth around 23 mm, facing the transducer surface. The CMUT is biased at 120 V. In the TX, a two-cycle 30 Vpp pulse at 3 MHz ($f_0$) is used to excite the TX elements. The TX frequency deviates from the center frequency of the CMUT; thus, more nonlinear components are produced.

In the RX, two scenarios are compared based on two different RX settings. In scenario A, the RX AFE is programmed at full band, and thus the gain is limited by the fundamental signal component. In scenario B, the RX bandwidth is set to 8-10 MHz by the BP filter for better signal acquisition at the third harmonic frequency ($3f_0$). Since the BP filter suppresses the fundamental signal ($f_0$), more PGA gain is possible after filtering.

The reconstructed images after conventional delay-and-sum beamforming are provided in Fig. 19. The lateral resolution in scenario B is improved by about 32% in this case compared to scenario A, calculated based on the point spread function of the first wire phantom. The axial resolution is deteriorated by 6% after BP filtering, which is a mild loss compared to the lateral resolution improvement. The acoustic measurements show that moderate filtering will have little impact on the axial resolution while allowing better acquisition for harmonic components. We also observe more clutter in scenario B in this comparison. One potential reason is that, in scenario B, the filtered signal has less signal power than the full-bandwidth signals, thus degrading the relative difference between the main lobe and the side lobes.

### C. Benchmarking

Since most published systems are designed for conventional UFI and do not include a BP filter, a system-level benchmark is difficult. Instead, the TIA performance is compared with state-of-the-art as shown in Table II.

The noise and linearity performance listed for this work are based on the measured results of the AFE w/o ADC since we cannot measure the TIA alone. The TIA specs are very different depending on the transducer properties (size, impedance, frequency); therefore, a revised noise efficiency factor (NEF$'$) is commonly used for comparison [22], defined as

$$\text{NEF}' = P_{n,in} \cdot \sqrt{\text{Power}},$$

where $P_{n,in}$ is the input-referred acoustic pressure noise spectral density averaged inside the passband. The reported NEF$'$ in this work is calculated by referring the measured noise to an equivalent pressure noise using the estimated RX sensitivity. The proposed TIA achieves a NEF$'$ of 0.86 mPa·√mW/Hz, which is comparable to the prior works. Compared to the references, the reported TIA achieves a competitive noise figure despite the

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**Fig. 16.** Measured dynamic range based on ADC outputs @ full band.

**Fig. 17.** Power breakdown.
Fig. 18. Acoustic measurement setup.

Fig. 19. Acoustic measurement results.

TABLE II
COMPARISON OF PROPOSED TIA WITH STATE-OF-THE-ART

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<td>-</td>
<td>-</td>
<td>12/6</td>
<td>-</td>
<td>200/2</td>
</tr>
<tr>
<td>Gain control</td>
<td>Discrete</td>
<td>Continuous</td>
<td>Fixed</td>
<td>Fixed</td>
<td>Discrete</td>
<td>Fixed</td>
<td>Discrete</td>
</tr>
<tr>
<td>RX sensitivity [mV/kPa]</td>
<td>136 b</td>
<td>-</td>
<td>2.0</td>
<td>-</td>
<td>0.41</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IRN density [pA/Hz]</td>
<td>3.1 b</td>
<td>2.0</td>
<td>2.0</td>
<td>-</td>
<td>0.41</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>HD2 [dB]</td>
<td>-61 b</td>
<td>-</td>
<td>-37</td>
<td>-</td>
<td>46</td>
<td>-</td>
<td>&lt;64.3</td>
</tr>
<tr>
<td>HD3 [dB]</td>
<td>-58 b</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>46</td>
<td>-</td>
<td>&lt;64.3</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>1.4</td>
<td>4.9</td>
<td>0.42</td>
<td>1.4</td>
<td>14.3</td>
<td>0.66 d</td>
<td></td>
</tr>
<tr>
<td>Noise figure [dB]</td>
<td>5.2 b</td>
<td>-</td>
<td>3.4</td>
<td>8.9</td>
<td>13.5</td>
<td>10.3</td>
<td></td>
</tr>
<tr>
<td>NEF [mPa⋅√m/Hz]</td>
<td>0.86 b,c</td>
<td>0.96 c</td>
<td>0.55</td>
<td>2.7</td>
<td>2.1</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

a Estimated by measuring the pulse-echo from a US reflector.
b Measured with the entire AFE based on analog outputs.
c Calculated by referring the measured noise to an equivalent pressure noise using estimated transducer RX sensitivity.
d Averaged power per element.
large transducer capacitance. Moreover, the TIA has state-of-the-art linearity performance, which makes it suitable for UHI applications.

V. CONCLUSION

In this paper, an RX front-end for UHI systems is presented in a 40 nm CMOS process. A complete RX chain from AFE to digital data link is implemented. Thanks to the proposed two-stage self-biased inverter-based architecture, the TIA shows state-of-the-art performance in terms of noise, power, and linearity despite the large transducer input capacitance. As a second contribution, this work introduces flexible bandwidth selection in the AFE to improve RX dynamic range and lateral resolution in UHI, which is confirmed by acoustic measurements.

REFERENCES


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