A Closed-loop Reconfigurable Analog Baseband Circuitry with Open-loop Tunable Notch Filters to Improve Receiver Tx leakage and Close-in Blocker Tolerance

A Closed-Loop Reconfigurable Analog Baseband Circuitry With Open-Loop Tunable Notch Filters to Improve Receiver Tx Leakage and Close-in Blocker Tolerance

Xu Cheng, Feng-Jun Chen, Liang Zhang, Hao Gao, *Member, IEEE*, Jiang-An Han, Jing-Yu Han, Yang Yu, and Xian-Jin Deng

***Abstract*—This brief presents an analog baseband (ABB) circuit in a 0.13 μm SiGe technology for transmitter leakage cancellation and close-in blocker suppressions in fully duplex (FD) frequency-modulated continuous-wave (FMCW) radar. This ABB comprises a programmable gain amplifier (PGA) and a cascaded LPF/Notch hybrid, which incorporates a closed-loop (CL) reconfigurable low-pass filter (LPF) and an open-loop (OL) tunable notch filter. The adopted key topologies include active-R-C bi-quads and G_m-C ones. In an FD FMCW transceiver, Tx leakage and close-in blockers are difficult to be eliminated in the RF domain, especially when leakage/blockers are very close to desired signals or even in-band in the frequency domain. This LPF/notch hybrid is proposed to solve this issue. The LPF and PGA provide bandwidth (BW)/gain programmability, while the G_m-C bi-quad provides adaptable center frequency for a notch filter. With this adaption, the notch filter could be adjusted to match the leakage/blocker offset frequency. Thus, digitally discrete programmability and analog continuous tuning capability are combined in this solution for improving the overall front-end interference robustness without de-sensitizing the Rx. Furthermore, the order of LPF/notch hybrid is programmable from 2 to 10 with a step of 2 for different rejection levels of interferences. The measured chip achieves a −3dB bandwidth of 6 ∼ 21 MHz with 4-bit digital control and 1 MHz/step programmability, and a voltage gain of 0 ∼ 70 dB with 9-bit digital control (3-bit from pre-amplifier, and 6-bit from PGA with 1 dB/step). With the condition of 15 dB gain, output P_{-1dB} is 11.8 dBm@3MHz, and the output IP3 is 20.8 dBm@3MHz.**

***Index Terms*—Analog baseband, fully duplex, FMCW, notch filter, G_m-C filter, PGA.**

Manuscript received August 18, 2021; accepted October 31, 2021. Date of publication November 4, 2021; date of current version March 15, 2022. This brief was recommended by Associate Editor Y. Qin. *(Corresponding author: Xu Cheng.)*

Xu Cheng, Feng-Jun Chen, Liang Zhang, Jiang-An Han, Yang Yu, and Xian-Jin Deng are with the Institute of Electronic Engineering and the Microsystems and Terahertz Research Center, China Academy of Engineering Physics, Chengdu 610000, China (e-mail: chengxuthz@126.com).

Hao Gao is with the Department of Electrical Engineering, TU Eindhoven, 5600MB Eindhoven, The Netherlands.

Jing-Yu Han is with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, and also with the University of Chinese Academy of Sciences, Beijing, China.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2021.3125305.

Digital Object Identifier 10.1109/TCSII.2021.3125305

I. Introduction

THE TRENDS of higher data rates, lower latency, longer communication distance, and multi-functionality introduce new challenges in radio receivers. The most challenging issues could be concluded as in-band/near-band interference and insufficient RF/analog filtering induced by wideband receiver in Fig. 1. On one hand, when signal and interference are located far from each other in a narrowband ABB, pure RF/analog filter is sufficient to attenuate interference to a negligible level as depicted in the upper half of Fig. 1. On the other hand, when signal and interference are near to each other in a wideband ABB, traditional RF/analog filter is insuffient as depicted in the lower half of Fig. 1, especially when full-duplex (FD) or frequency devision duplex (FDD) standards are utilized [1]—[2]. Therefore, the burden of interference elimination is placed upon the ABB part in millimeter-wave Rx designs.

In a W-band FD FMCW system, the transceiver (TRx) transmits a signal in the order of 10 dBm, while the received signal is about −50 dBm. In this case, two most significant spurs near DC-frequency are Tx-to-Rx leakage and bumper reflection [3]. In the former scenario, a down-converted self-interference in the order of −30 dBm due to limited on-chip Tx-to-Rx isolation (∼ −40 dB), is located at several tens of KHz offset from DC. This self-interference signal is almost 20dB higher than the desired signal received. Considering Rx gain, including ABB, is typically higher than 50 dB, this down-converted self-interference could reach a hard-clipped level and result in Rx desensitization. Therefore, higher than 20dB interference suppression is demanded in ABB filter design. In the latter scenario, a reflection from bumpers could be down-converted to several KHz offset from DC, and this power would be in the order −40 dBm [3]. What is more, even order distortions induced by mismatches in mixer and ABB even complicate low frequency IF demodulations [1]–[2]. In short, suppression of in-band/near-band interference should be placed in a high priority in ABB designs of W-band FD FMCW systems.

Previous literature [1]–[2] and [10] proposed ABB notch filters to prove its merits in both Tx leakage/blocker suppression and Rx linearity improvement. However, 3 major

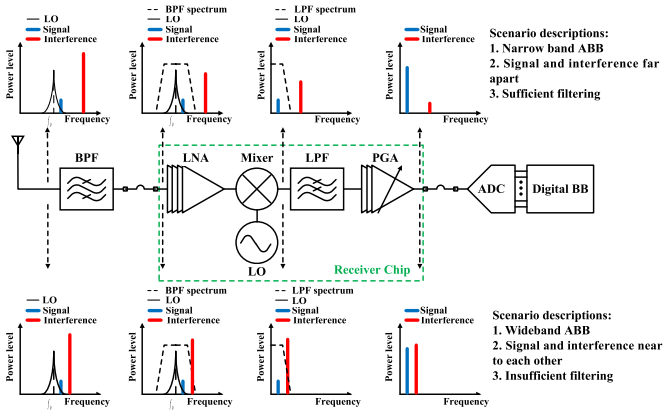

Fig. 1. Signal spectrum across the Rx chain.

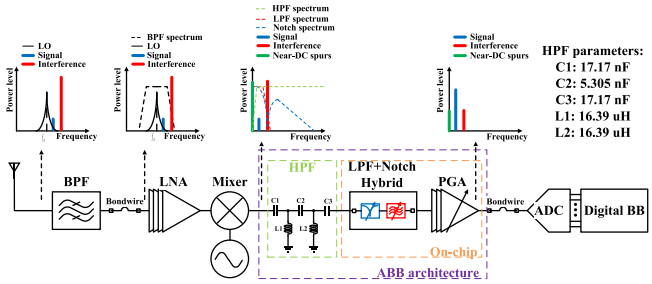

Fig. 2. Rx architecture with ABB LPF/Notch hybrid proposed.

problems remain unsettled: (1) blockers are assumed to be more than twice the −3dB bandwidth of ABB, which makes pure notch filtering suffice to meet ABB requirements. However, when blockers are located nearer between once and twice the −3dB bandwidth of ABB or even in-band, notch filters is not satisfactory and stricter filtering need including low pass filter (LPF) and high pass filter (HPF) emerges. (2) current-mode notch filters are adopted in [1] for potential higher linearity and thus, its power consumption quadruples across the notch tuning range. In addition, the linearity of a current-mode down-conversion Rx is a function of the input impedance of TIA (Trans-Impedance Amplifier), and therefore, high open-loop gain at blocker frequencies is required as well [2], which not only increases overall power consumption but also complicates design of notch filters. (3) when high quality off-chip HPF is inserted between mixer and LPF/Notch hybrid to suppress low frequency spurs as depicted in Fig. 2, active mixer eases the design of HPF and LPF/Notch hybrid. Although the idea presented here can also be applied to current-mode topology with Q-factor optimization, voltage-mode LPF/Notch hybrid is adopted in this work with a note on off-chip HPF designs. In a W-band FD FMCW TRx, a basic rejection requirement of −70dB@1KHz and −40dB@100KHz prefers a truly high performance HPF while the values of inductors and capacitors make a complete one-chip ABB solution impossible in Fig. 2.

On the basis of a high quality off-chip HPF, this work brings an open-loop G_m-C notch filter into traditional closed-loop ABB with the aim of larger than 20 dB interference rejections, at 5 MHz offset from the −3 dB bandwidth corner of a pass-band (20 MHz of 25 MHz). This novelty is based on the stable frequency response of closed-loop topology and the frequency tunability of open-loop one. In this idea, an architecture of

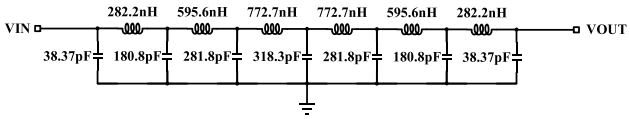

Fig. 3. 13th order Butterworth LPF prototype synthesis (single-ended).

on-chip LPF/Notch hybrids accompanied by PGA is proposed in this work, as described in orange in Fig. 2. In order to eliminate in-band/near-band interference, HPF and LPF/Notch hybrids are introduced to achieve adequate filtering. With the help of accurate notch location in this hybrid way, higher interference rejection is achieved than an LPF-only solution. Afterwards, PGA amplify both signals and interference without much nonlinearity, and the signal amplitude meets an ADC front-end's full swing requirement. In addition, the LPF/Notch hybrid improves both the intermodulation distortions and the overall ABB linearity. The structure of the rest of paper is organized as follows. Section II presents the analysis of an ABB architecture, including its concept and frequency behavior. Section III provides the implementation and measurement results of this ABB prototype. Conclusions and comparisons are drawn in Section IV.

II. ABB Architecture

In this ABB chipset, an LPF-first architecture with an embedded programmable 3-bit low noise pre-amplifier is applied [4]. There are two working modes: the first one is the low noise mode, and another is the high suppression one. In the former mode, the interference is less critical while receiver noise is the dominant issue. Thus, the pre-amplifier is turned on to improve the ABB NF. Meanwhile, in the latter mode, interference is the critical issue. Therefore, the pre-amplifier is turned off to avoid linearity degradation and potential signal saturation.

Considering of larger than 20 dB interference rejections at 25 MHz offset frequency, an LPF synthesis is conducted with a Butterworth prototype due to its maximum in-band flatness [9] as shown in Fig. 3. This on-chip programmable LPF can be realized via 4 major techniques: (a) switched-capacitor LPF; (b) passive R-L-C LPF; (c) active-R-C LPF; (d) G_m-C LPF. Switched-capacitor LPF is not adopted for its discrete-time characteristics, which needs an on-chip non-overlapping clock generator, and passive R-L-C is not applied due to its large area overhead. Active-R-C LPF has its advantage on stable frequency response over process, voltage, temperature (PVT) variations while G_m-C LPF has its advantage on wide tunability and high frequency potential. As is known, every active-R-C bi-quad needs 1 operational amplifiers (OPAMP) while every G_m-C one needs 2 operational transconductance amplifiers (OTA, or G_m cell) regardless of the automatic tuning circuitry [8]. When the synthesized 13th order Butterworth LPF prototype in Fig. 3 is transformed into active-R-C one and G_m-C one, 6 OPAMPs and 12 OTAs are needed respectively . Thus, the total chip area of active-R-C LPF is relatively smaller than that of G_m-C topology despite the actual topology of OPAMPs or OTAs. However, active-R-C LPFs could not support continuous frequency adjustability to respond to dynamic leakage/blockers. Therefore, active-R-C topology is adopted in the main signal path for stable frequency response over PVT corners while G_m-C one is utilized as an auxiliary path for adequate blocker's suppression,

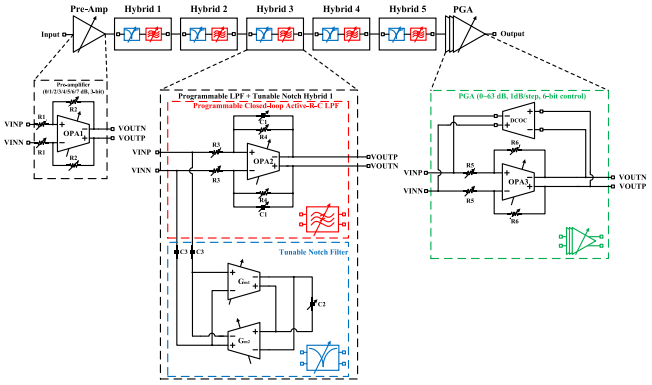

Fig. 4. ABB architecture with detailed sub-block schematics.

which not only meets various application scenarios but also saves area from a holistic view.

The simplified on-chip ABB architecture is plotted in the orange bracket of Fig. 2 and further expanded in Fig. 4 with detailed schematics of LPF/Notch hybrid and PGA. The LPF is composed of 5-stage bi-quads which includes a programmable 2^{nd}-order LPF and tunable 2^{nd}-order notch filter. The PGA is composed of 3 cascaded closed-loop OPAMPs with a maximum voltage gain of 63 dB and a minimum step of 1 dB. Low dropout regulator (LDO) and bandgap with electronic trimmers are incorporated to increase the PVT robustness of core circuits while register banks and I2C interface are brought in to facilitate the digital control.

A. Programmable LPF/Notch Hybrid

In Fig. 4, the pre-amplifier used the ratio of R_2/R_1 to set the voltage gain while the LPF used the ratio of R_4/R_3 to set the voltage gain and C_1 to set the bandwidth. From a transistor-level perspective, the introduction of notch filter worsens the input-referred NF by 1 $\sim$ 2 dB while the rejection at 25 MHz increases by 4 $\sim$ 5 dB for every notch bi-quad brought in. In addition, the ABB NF deterioration is relieved by previous Rx front-end circuitry (including LNA and mixer) power gain which is typically higher than 20 dB (voltage gain is typically 5 $\sim$ 10 dB higher). Therefore, the actual NF deteriorations is negligible from a systematic view [1]–[2].

The gyrator-based notch filter is drawn in the blue bracket of Fig. 4 and redrawn in Fig. 5 with LC resonating tank on the upper half and the trans-conductance (G_m) cell schematic (G_{m1}/G_{m2}) in the lower half. The active inductor is a gyrator which is shown in the upper right corner of Fig. 5. The notch tuning is achieved with the help of C_2 and trans-conductance G_{m1}/G_{m2} tuning. Assuming G_{m1}/G_{m2} has a trans-conductance G_{m1}/G_{m2} and output conductance G_{o1}/G_{o2}. The gyrator inductance L_{gyr}, series resistance R_{gyr}, notch frequency ω_{gyr} and input impedance Z_{in} in Fig. 5 are derived in (1)-(4).

$$L_{gyr} \approx C_2/(G_{m1} \cdot G_{m2}) \tag{1}$$

$$R_{gyr} \approx 2 \cdot (G_{o1} + G_{o2})/(G_{m1} \cdot G_{m2}) \tag{2}$$

$$\omega_{gyr} \approx \sqrt{(G_{m1} \cdot G_{m2})/(C_2 \cdot C_3)} \tag{3}$$

$$Z_{in} \approx 2/(\omega \cdot C_3) + (2\omega \cdot C_2)/(G_{m1} \cdot G_{m2}) + 2 \cdot (G_{o1} + G_{o2})/(G_{m1} \cdot G_{m2}). \tag{4}$$

Thus, the notch depth can be approximated [1] as:

$$Notch\ depth \approx R_3/Z_{in}. \tag{5}$$

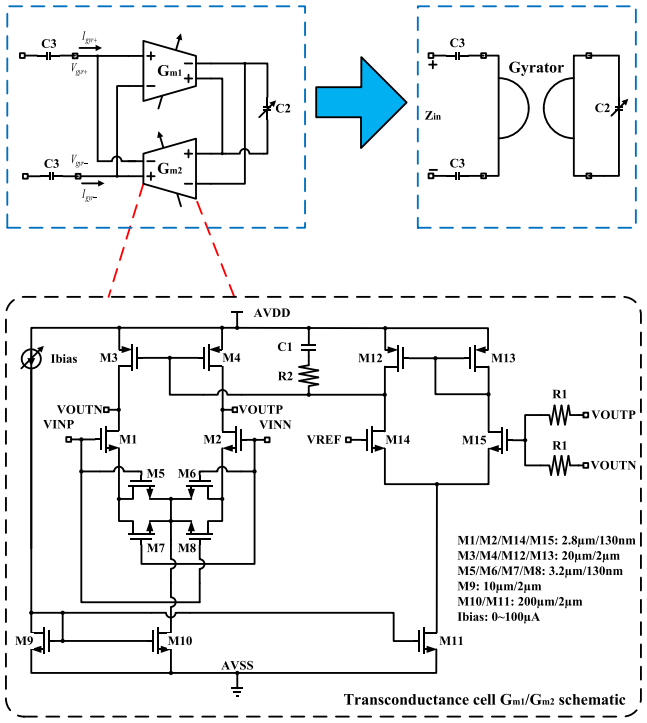

Fig. 5. Tunable active inductor realization.

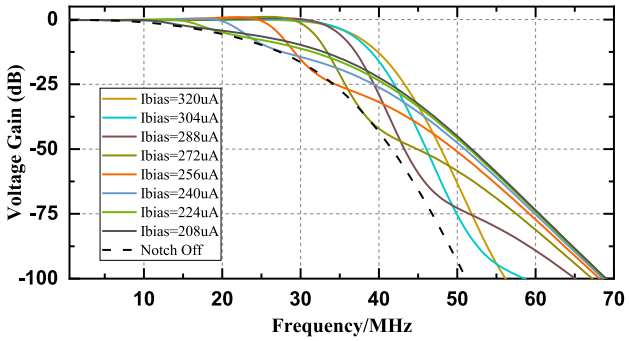

Fig. 6. Post-simulated LPF/Notch hybrid gain curves with notch frequency moving.

In notch filter designs, a fundamental tradeoff between filter impedance and power consumption exists and reduces the power efficiency. In order to sink most of the interference signal, the notch impedance should be much lower at the interference frequency, and thus, the G_m cells would consume more power. According to (3), (4), (5), a larger C_3 and smaller C_2 lead to lower Z_{in} and higher notch depth while C_2 and C_3 are inversely related to ω_{gyr}. Therefore, there exists a meticulous tradeoff between notch depth and notch frequency, which leads to a demand on both broad and fine tunability, as shown in Fig. 6. Since pure digital programmability or analog tuning is not enough to both accommodate tuning range and PVT robustness, a 10-bit DAC is utilized in the G_m tuning with its unit current reference tunable, which is described as I_{bias} in the lower half of Fig. 5, where a 4-bit programmability is adopted in C2 tuning. Thus, the notch filter frequency is designed to be broadly adaptable.

Previous literature adopted Nauta-cell or its modifications to implement the G_m cell for its simplicity and

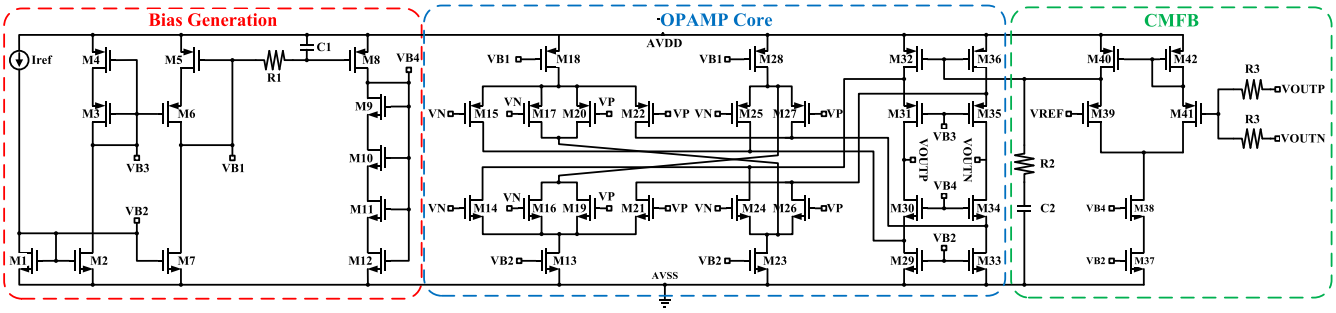

Fig. 7. Tunable active inductor realization.

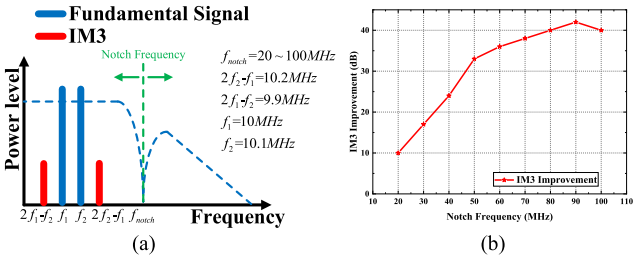

Fig. 8. ABB IM3 improvement with notch frequency tuning when ABB output power is set to be 0 dBm. (a) IM3 simulation condition; (b) IM3 improvement v.s. notch frequency.

modularity [1]–[2]. However, its voltage tuning port is limited to the power supply. Therefore, the power supply rejection ratio (PSRR) is low, and power consumption varies a lot across the tuning range. In addition, sufficient power supply filtering is a prerequisite in Nauta-cell based G_m-C filter designs. In this design, adaptive source degeneration topology is utilized in G_m cell designs for its high linearity, acceptable power supply rejection ratio and PVT robustness as shown in the lower half of Fig. 5. The common-mode feedback (CMFB) is implemented in every G_m cell for the overall filter stability. The post-simulated LPF/Notch hybrid gain curves with notch tuning are shown in Fig. 6. The hybrids consume 5 ~ 10 mA@1.8 V supply from the post-simulation and provides a programmable bandwidth from 6 to 21 MHz with 1 MHz step. The input-referred root-mean-squared (RMS) noise voltage is 110.3 nV/$\sqrt{}$Hz, the OP_{1dB} is 15 dBm@5 MHz, and the OIP3 is 23.5 dBm@5 MHz with intermodulation offset frequency at 100 kHz.

B. PGA Design

PGA utilized a 3-stage closed-loop cascaded topology as shown in Fig. 4. The first stage is with a 1-bit control of 32/0 dB gain. The second one is with a 2-bit control of 24/16/8/0 dB voltage gain. The third one is with a 3-bit control of 7/6/5/4/3/2/1/0 dB voltage gain. Considering the interference robustness issue, the OPA is a rail-to-rail fully differential amplifier with CMFB for its large signal handling ability, as shown in Fig. 7. A simplified schematic of the fully differential amplifier is shown in Fig. 7 with bias generation, OPAMP core and CMFB. The input and output common-mode voltages of this amplifier are set at half of the supply voltage. The sizes of the main amplifying transistors are optimized for DC offset and noise figure. With a voltage gain of 63dB, a 20mV DC offset is added to differential signals of 10μV to be input to the PGA with less than 5mV DC offset at

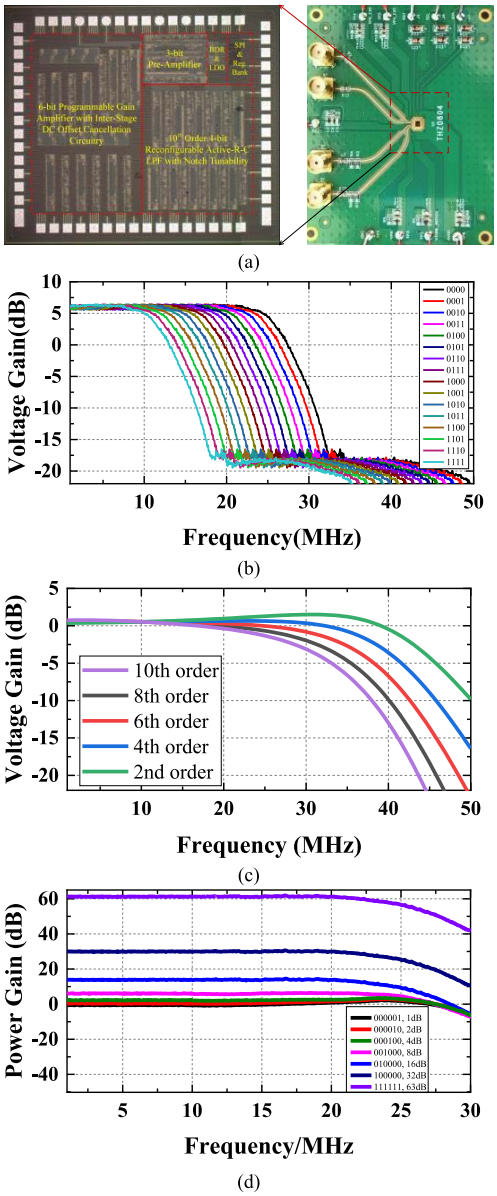

Fig. 9. ABB IC photograph and measurement results. (a) ABB IC photograph; (b) LPF gain curves with 4-bit digital codes when notch is on with Ibias = 272 μA; (c) ABB gain curves with filter order 2/4/6/8/10 when notch/PGA is off; (d) ABB gain curves with 6-bit digital codes when notch is off, LPF control codes are 0001 and pre-amplifier control codes are 0000.

the PGA output ports. The PGA consumes 6.5 mA@1.8 V supply and provides a programmable voltage gain from 0 to 63 dB in 1 dB step. The input-referred RMS noise voltage is

TABLE I
STATE OF THE ART COMPARISON

Ref.	[1] TCASI 2019	[2] TCASI 2019	[4] TCASII 2015	[5] JSSC 2011	[6] TVLSI 2012	[7] TCASI 2013	This work
Process	65-nm CMOS	65-nm CMOS	65-nm CMOS	90-nm CMOS	65-nm CMOS	90-nm CMOS	130-nm BiCMOS
Architect	OL G_m-C + CL PGA	OL G_m-C + CL PGA	CL Active-R-C + CL PGA	OL G_m-C (No PGA)	CL Active-R-C + CL PGA	OL G_m-C (No PGA)	CL Active-R-C + OL G_m-C + CL PGA
P_{dc} (mW)	9~36@1.2V	5.5@1.2V	1.72~9.6@1.2V	4.35@1.2V	10.78@1.2V	3@1.2V	20.7~29.7 (PGA 11.7, Filter 9~18) @1.8V
Gain range (dB)	49.5	28~42	0~72	N/A	-6~53	N/A	0~70
Gain step (dB)	N/A	N/A	18	N/A	6	N/A	1
BW range (MHz)	10	20	0.2~20	8.1~13.5	0.09~14.2	7.1~20.3	6~21
BW step (MHz)	N/A	N/A	0.1	Analog tuning	N/A	N/A	1
Filter order	2	2	2/4/6/8	6	N/A	6	2/4/6/8/10
IRN ($nV/\sqrt{Hz}$)	N/A	N/A	87.2	75	N/A	66.2	135.6
OIP3 (dBm)	N/A	N/A	17.8	22.1	22.43	-8.7	20.8
Area (mm^2)	0.15	0.078	0.8	0.239	1.57	0.23	2.16

131.1 nV/$\sqrt{}$Hz, the OP_{1dB} is 16 dBm@5 MHz, and the OIP3 is 24.1 dBm@5 MHz with an intermodulation offset frequency of 100 kHz.

C. Linearity Improvement

In order to verify linearity improvement of the ABB chip, a two-tone simulation was performed with the IM3 frequency at 9.9/10.2 MHz. The simulation shows an improvement of 10 $\sim$ 41 dB over the frequency range of 20 $\sim$ 100 MHz (see Fig. 8), which is in accordance with the OIP3 improvement of the ABB IC. When notch movers close to the signal, IM3 improvement drops since the input impedance drops in (4) [1]–[2].

III. IMPLEMENTATIONS OF THE ABB

The ABB chip is implemented in an in-house 130-nm SiGe BiCMOS technology with a core area of 1.2 × 1.8 mm^2 (as shown in Fig. 9 (a)). A 6-bit PGA with DCOC, a 10^{th} order 4-bit LPF/Notch hybrid, a 3-bit pre-amplifier, power supply management, register bank and SPI are integrated on chip to facilitate the practicality of the whole chip. The measurement results with the help of FR-4 PCB wire-bonding are shown in Fig. 9 and listed in Table I. More than 20 samples were fully tested with similar results. A notch bias current of 272 μA is selected to ensure the close-in blocker suppression and the LPF gain curves are programmable with 4-bit control as shown in Fig. 9 (b). A suppression of around 22 dB is clearly observed when notch frequency is at 25 MHz. The LPF order programmability is illustrated in Fig. 9 (c) while the PGA gain curves with 6-bit control are given in Fig. 9 (d) with notch off.

IV. CONCLUSION

Targeting at adaptable and acceptable in-band/near-band interference suppression, this briefing proposed an ABB circuitry with traditional closed loop LPF/PGA and novel open loop notch filter. In this chipset, a LPF and a PGA provide bandwidth (BW)/gain programmability, and the G_m-C filter provides adaptable center frequency for a notch filter. With the adaption, the notch filter could be adjusted to match the leakage/blocker offset frequency. Thus, digitally discrete programmability and analog continuous tuning capability are combined for improving the overall front-end interference robustness without de-sensitive the Rx. Furthermore, the LPF and notch filter order is programmable for different rejection levels. After a complete implementation in an in-house SiGe process, programmability in bandwidth, gain, filter order, and continuous tunability in notch frequency are simultaneously validated with increased flexibility, adaptability, and reconfigurability in various multi-standard Rx.

REFERENCES

[1] M. Abdulaziz, E. A. M. Klumperink, B. Nauta, and H. Sjöland, "Improving receiver close-in blocker tolerance by baseband G_m—C notch filtering," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 885–896, Mar. 2019, doi: 10.1109/TCSI.2018.2872469.

[2] M. T. Ozgun, A. Abdelhamid, and H. Dogan, "A low power receiver front-end design with tunable notch filter for TX leakage and blocker suppression," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1180–1191, Mar. 2019, doi: 10.1109/TCSI.2018.2879040.

[3] D. Sahu *et al.*, "A 45nm 76-81GHz CMOS radar receiver for automotive applications," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2019, pp. 9–12, doi: 10.1109/A-SSCC47793.2019.9056907.

[4] Y. Wang, L. Ye, H. Liao, R. Huang, and Y. Wang, "Highly reconfigurable analog baseband for multistandard wireless receivers in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 3, pp. 296–300, Mar. 2015, doi: 10.1109/TCSII.2014.2368975.

[5] M. S. S. Oskooei, N. Masoumi, M. Kamarei, and H. Sjoland, "A CMOS 4.35-mW +22-dBm IIP3 continuously tunable channel select filter for WLAN/WiMAX receivers," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1382–1391, Jun. 2011, doi: 10.1109/JSSC.2011.2120670.

[6] R. Kulkarni, J. Kim, H. Jeon, J. Xiao, and J. Silva-Martinez, "UHF receiver front-end: Implementation and analog baseband design considerations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 197–210, Feb. 2012, doi: 10.1109/TVLSI.2010.2096438.

[7] L. Ye, C. Shi, H. Liao, R. Huang, and Y. Wang, "Highly power-efficient active-rc filters with wide bandwidth-range using low-gain push-pull opamps," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 95–107, Jan. 2013, doi: 10.1109/TCSI.2012.2215700.

[8] T.-Y. Lo and C.-C. Hung, *1V CMOS Gm-C Filters Design and Applications*. Dordrecht, The Netherlands: Springer, 2009.

[9] C. Kai, *Microstrip Filters for RF/Microwave Applications*. New York, NY, USA: Wiley, 2001.

[10] H. Liu, X. Zhu, M. Lu, Y. Sun, and K. S. Yeo, "Design of reconfigurable dB-linear variable-gain amplifier and switchable-order g_m-c filter in 65-nm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5148–5158, Dec. 2019, doi: 10.1109/TMTT.2019.2947668.