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# Short Polarization Converter Optimized for Active–Passive Integration in InGaAsP–InP

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**Abstract**—An improved design for an integrated polarization converter is presented. The device is designed for monolithic integration with active and passive components on InP–InGaAsP. A novel simplified fabrication process is demonstrated. Measured polarization conversion >97% over a wavelength range of >35 nm agrees well with simulations.

**Index Terms**—Indium phosphide, integrated devices, polarization converter (PC).

## I. INTRODUCTION

**P**OLARIZATION handling is of ever greater importance in modern telecommunications networks. First of all, a lot of components in the network are highly polarization-dependent; furthermore, polarization-mode dispersion can degrade the transmission in an optical fiber. On the other hand, the polarization can be employed in, e.g., polarization multiplexing, polarization-based filtering, and polarization diversity [1]. In all these cases, polarization converters (PCs) are key elements.

Passive PCs that are able to be integrated with both active and passive components are preferred. Polarization conversion can be obtained by periodically loaded waveguide sections [2]–[4], by using integrated bends [5], or by using a single waveguide section with a vertical and a slanted sidewall either by etching a slope [6]–[8] or by creating a slope effect by etching trenches [9], [10].

One problem with these designs is the difficulty to integrate them with passive and specifically with active components. The PCs and active components (such as semiconductor optical amplifiers (SOAs) and phase shifters [11]) can be made in the same layerstack, but the optimal thickness of the top-cladding differs by more than 1  $\mu\text{m}$ . For PCs, a large birefringence, and more important, a critical width definition close to the waveguide layer is needed: hence, a thin top cladding is preferred (typically smaller than 300 nm); for SOAs and electrooptic phaseshifters, a thick top cladding (typically 1.5  $\mu\text{m}$ ) is needed below the contact to avoid optical losses due to the contact layer.

This is clarified in Fig. 1: an SOA, phaseshifter, and a conventional PC are shown. Critical lithographical definition is not possible with these height differences as the photoresist thickness varies over the different heights and the depth of focus is

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Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

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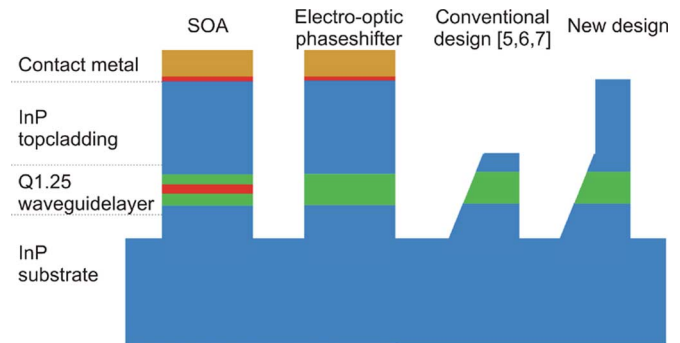


Fig. 1. Cross section of active devices (SOA, phaseshifter), a conventional PC, and the new design.

limited for critical definitions. This complicates processing and integration of these devices.

The new design [12] is shown in the right-most picture in Fig. 1. This new proposed design uses the same top cladding as an active device and can be integrated with the other components. The birefringence with the thicker cladding is only slightly reduced with respect to the thinner cladding. Hence, the increase in length for this design is less than 40  $\mu\text{m}$ .

## II. PRINCIPLE

The PC is the integrated optical analogue of the half wave plate in bulk optics. The device consists of a ridge waveguide with a straight and a slanted sidewall. Because of the narrow width, this slanted sidewall causes the two modes to tilt, ideally for  $+45^\circ$ , respectively,  $-45^\circ$ . If light in a straight waveguide is coupled to the PC waveguide, both modes are excited. After a half beat length  $L_{\lambda/2}$  ( $L_{\lambda/2} = \pi/(\beta_1 - \beta_2)$ , where  $\beta_n$  is the propagation constant of mode  $n$ ), the modes are completely out of phase and recombine into the orthogonal polarization in a straight output waveguide.

## III. DESIGN

The layer stack consists of an InP substrate, a 500-nm InGaAsP [ $Q$  (1.25  $\mu\text{m}$ )] waveguide layer and a 1500-nm InP top cladding. Simulations with the commercial waveguide solver FIMMWAVE predict an optimal conversion of TE to TM and *vice versa* larger than 99% for a width of 0.94  $\mu\text{m}$  and a length of 141  $\mu\text{m}$ . A conversion above 95% is expected for a width deviation of 100 nm.

Deviations from the calculated width and length can be expected, because the refractive indexes used in the simulations are not accurately known for these materials.

The total device contains an asymmetric waveguide as the converter section, 1.2- $\mu\text{m}$ -wide deep input and output waveguides, coupled to 3- $\mu\text{m}$ -wide shallow waveguides via 75- $\mu\text{m}$ -long tapers. At the interface of the input waveguides

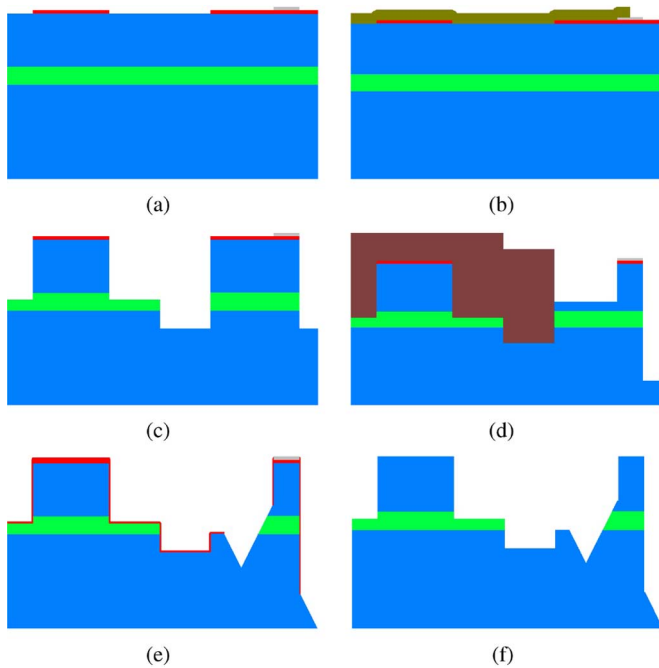


Fig. 2. Processing of the integrated PC (see text).

and the PC section, a small ridge is present, perpendicular to the waveguide. This is needed to prevent etching of the input waveguide in the wet etch for the slanted sidewall. However, this does not influence the propagation of the waveguide modes.

#### IV. FABRICATION

The PCs have strict tolerances, so the converter sections will be defined using electron beam lithography (EBL). EBL is not suited to write large circuits, therefore, all other waveguides will be defined using standard optical lithography. The EBL written parts are aligned to the optical waveguides.

The processing of the PC, shown in Fig. 2, is as follows.

- First the waveguides and write fields for the EBL, including alignment marks, are defined optically into a silicon nitride ( $\text{SiN}_x$ ) mask. Next the PCs are defined in Ti on top of the  $\text{SiN}_x$  using EBL and a lift-off process.
- Before etching any waveguide, the second EBL step is done to open the straight side of the PC.
- Next the nitride at the straight side of PC is opened. The shallow waveguides and the straight side of the PC are etched with  $\text{CH}_4/\text{H}_2$  reactive ion etching (RIE) in a double etch process [13].
- All shallow waveguides are covered with resist, and the PC area is opened with a noncritical optical lithography step. The  $\text{SiN}_x$  at the sloped side of the PC is opened and the InP top cladding is RIE etched until 300 nm above the waveguide layer. In this step, the critical dimensions are kept, because the Ti mask does not erode during the etch and thus the sidewalls are perfectly vertical. While etching this side, the straight side of the PC is etched even deeper, well below the waveguide layer.
- Silicon nitride is deposited on the whole sample and the shallow waveguides are again covered with resist. The  $\text{SiN}_x$  on the PC area is etched back using  $\text{CHF}_3$  RIE.

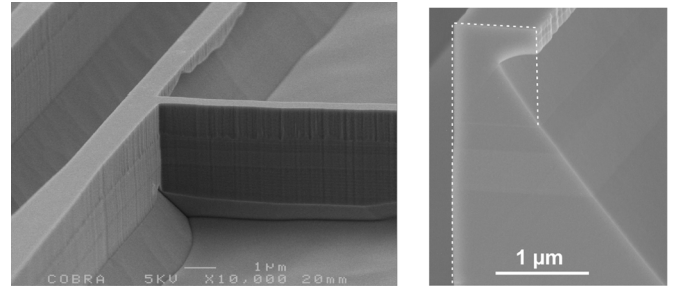


Fig. 3. SEM photographs of the integrated PC. Left: transition of a straight waveguide to the PC. Right: cross section through the converter.

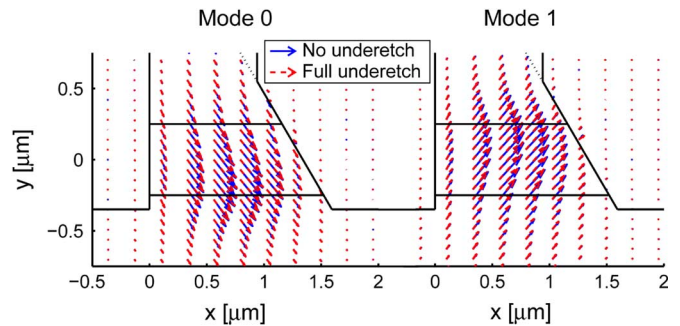


Fig. 4. E-field of the tilted modes in the PC.

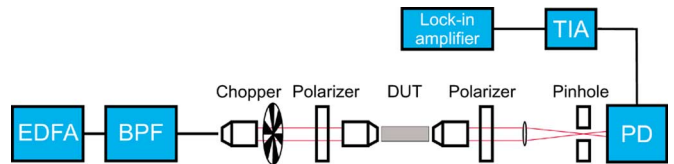


Fig. 5. Setup used for characterization of the PC. BPF: Bandpass filter, PD: Photodiode, TIA: Transimpedance amplifier.

Because of the directional etching, the etched sidewalls stay covered with  $\text{SiN}_x$ , which serves as a mask for the wet etching.

$\text{Br}_2$ -methanol is used to etch the slope. This etchant etches both InP and InGaAsP with an angle of  $54.7^\circ$  with respect to the surface.

- Finally, all the nitride is removed using an HF solution.
- The fabricated converters are shown in Fig. 3. From these figures, it is clear that there is an underetch at the shallow side (the sloped side). There is, however, no underetch at the deep side. This indicates that the underetch can be caused by stress in the masking material during the wet-etching.

The influence of this additional underetch on the conversion performance of the device will be negligible. The width definition at the InGaAsP layer is not affected by this underetch: the slope starts at the desired point, fixed by the silicon nitride, and stops on the crystal plane. The resulting difference in the tilt angle of the modes is smaller than  $1^\circ$ . Fig. 4 shows the tilted modes for both cases (with and without underetch).

#### V. MEASUREMENTS

The PCs are measured using a setup as shown in Fig. 5. The device is excited using an EDFA with a bandpass filter set to 1555 nm as a source. The filter has a 2-nm bandwidth, large

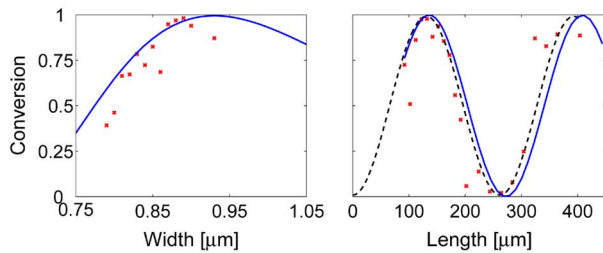


Fig. 6. Simulated conversion (solid), measured values ( $x$ ), and fit (dashed) as a function of width (left) and length (right).

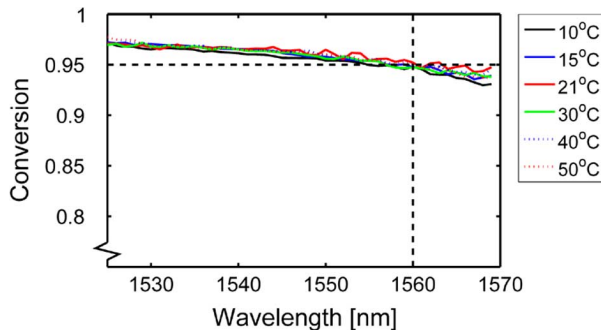


Fig. 7. Measured conversion as a function of temperature and wavelength.

enough to prevent Fabry–Pérot resonances. A polarizer at the input of the chip is used to select the input polarization. At the output another polarizer selects the polarization that is measured using the photodiode and the lock-in amplifier.

The power in both polarizations at the output is measured for both TE and TM polarized light at the input. The conversion is defined as the fraction of the converted polarization in the output power. This conversion is plotted as a function of width and length in Fig. 6.

The maximum conversion from TE to TM and *vice versa* occurs at 131- $\mu\text{m}$  length, corresponding to the half beat length between the modes of the converter section. The conversion is back to zero at the full beat length (262  $\mu\text{m}$ ). The maximum conversion for this device is 97%.

The scattered values for the measured conversion are caused by nonuniformities in the width along the device, caused in part by deviations in the etch depth, the underetch and the layer thicknesses. A width variation of 30 nm can explain the observed behavior.

Fig. 7 shows both the wavelength and the temperature dependence of the PC. A conversion larger than 95% is obtained over a wavelength range larger than 35 nm (limited by the available equipment). The device is insensitive to temperature in the range from 10 °C to 50 °C.

The total excess losses of the PC, including input and output tapers, are measured to be  $2.4 \pm 0.3$  dB for TE and  $2.6 \pm 0.3$  dB for TM, with respect to a shallow waveguide. The losses can be separated in scattering loss, caused by sidewall roughness of waveguides, which has a big influence on the narrow deeply etched waveguides, and overlap losses at the junctions (simulated to be well below 0.5 dB), most probably caused by the

nonoptimal coupling of the waveguide and the converter because of the underetch of the access waveguides in the propagation direction. This can be avoided by using a more controlled wet etch.

## VI. CONCLUSION

A new type of PC is shown, specially suited for easy integration with active and other passive devices. The device is fabricated and measured. The PC shows a maximum conversion of 97%. A conversion larger than 95% is obtained over a wavelength range larger than 35 nm and a temperature range  $>40$  °C.

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