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Ultrafast Asynchronous Multioutput All-Optical Header Processor

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Abstract—We present a novel all-optical header processing technique that can be utilized in all-optical packet switches. The header processor consists of a terahertz optical asymmetric demultiplexer in combination with a header preprocessor that separates the packet header from the packet payload. Experimental results show asynchronous operation of the header processor at a header bit rate of 10 Gb/s in the case of two output ports. This concept can, however, be extended to a larger number of output ports, operates at low power, and allows photonic integration.

Index Terms—Header recognition, optical packet switch, optical signal processing, polarization switching, semiconductor optical amplifier (SOA), terahertz optical asymmetric demultiplexer (TOAD).

A LL-OPTICAL header processing plays an important role in all-optical packet switching [1]–[3]. In [2], ultrafast all-optical header processing using a terahertz optical asymmetric demultiplexer (TOAD) is demonstrated at a bit rate of 250 Gb/s. This TOAD-based header recognizer operates at low energy and allows photonic integration, but a disadvantage is that the control pulse should be synchronous with the header bits. Also, since this header recognition concept is based on the binary value of a single bit, the header recognizer can only distinguish between two header patterns. In [3], an asynchronous multioutput all-optical header processing technique based on the two-pulse correlation principle in a semiconductor laser amplifier in a loop optical mirror (SLALOM) configuration is presented. This concept was employed in an all-optical packet switch [4]. This header processing technique does not require a synchronous control pulse, but the processing speed of the SLALOM-based header processor is determined by the semiconductor optical amplifier (SOA) recovery time $\tau_r(\sim 1$ ns) [5]. Moreover, the SOA has to be placed offset to the center of the loop with a distance that is larger than $\tau_r \cdot v_g (\sim 10$ cm), where v_g is the group velocity of light (~ 100 μm/ps). Thus, a disadvantage of the header processing method presented in [3] is that the SLALOM configuration is too large to allow photonic integration.

In this letter, we present a novel header processing technique that can distinguish a large number of header patterns and which allows asynchronous operation and photonic integration. The concept is based on combining the header preprocessor (HPP) that is presented in [6] with a TOAD that acts as a header rec-
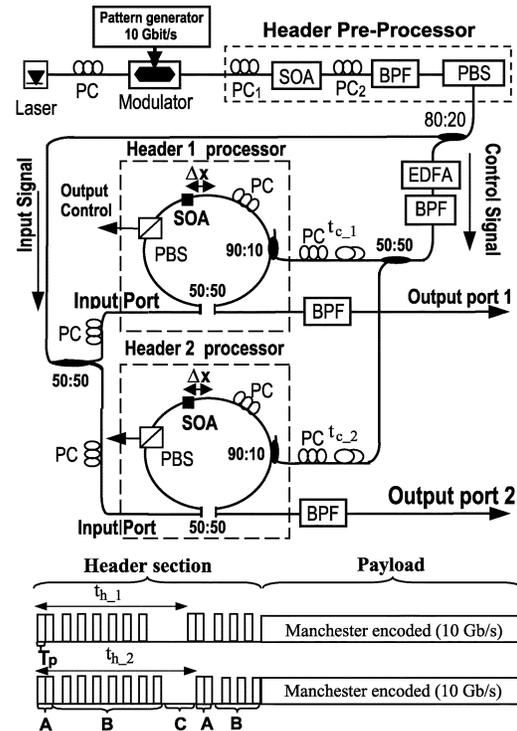
Fig. 1. Experimental setup to demonstrate the header processing system and packet structure are presented. PC: Polarization controller. EDFA: Erbium-doped fiber amplifier. BPF: Bandpass filter. (A) Header pulses. (B) Alternating "1" and "0" bits. (C) Sequence of "0s."

ognizer. The function of the HPP is twofold; it separates the packet header from the packet payload, but it also creates the control signal that is required for TOAD operation. The HPP output is fed into the TOAD for header recognition. Essential for TOAD operation is the employment of a control pulse for optical switching [7]. Whereas, for header recognition based on two-pulse correlation in a SLALOM configuration, the SOA recovery time plays a critical role, for header recognition based on TOAD operation, the timing of a control pulse is essential. As a direct consequence of this, a header recognizing system based on TOAD operation allows photonic integration. Moreover, TOAD operation guarantees ultrafast header processing at low power. Finally, the header processing system as a whole operates asynchronously and the system can be extended to have multiple output ports.

The optical header processing system is schematically presented in Fig. 1. It consists of an HPP and two TOADs that are placed in parallel. Each of the TOADs is designed to recognize a specific header pattern. An essential point of the header processing concept, as proposed in this letter, is that the address information is encoded by the difference in time between the

leading edges of two header pulses. The function of the HPP is to extract the header information from the data packet. It is shown in [6] that this can done by employing self polarization rotation in a nonlinear polarization switch. The nonlinear polarization switch is shown in the dashed box of Fig. 1. In brief, in the nonlinear polarization switch, an optical bit with a polarization angle of approximately 45° in injected into the SOA. As the bit propagates through the SOA, the polarization angle rotates due to the polarization-dependent gain and index saturation [6]. Essential, however, is that the rotation of the polarization angle of the leading edge of the header bit differs from the rotation of the polarization angle of the trailing edge due to self gain saturation. By aligning the polarization of the SOA output carefully with the polarizing beam splitter (PBS), only the leading edge of the header bit outputs the nonlinear polarization switch [6]. The space between the header pulses is filled with a sequence of alternating nonreturn-to-zero "0" and "1" bits at the same bit rate as the data payload, which ensures that the SOA remains saturated while the packet header passes through [6]. Also, a series of "0" with a duration that is longer than the SOA recovery time τ_r is placed before the second header bit, to allow the amplifier to recover before the second header pulse arrives at the SOA. Similarly, the guard time in between the header section and the payload section is filled with a sequence of alternating "0" and "1" bits to keep the amplifier saturated when the packet passes by. Finally, the packet payload is Manchester encoded to avoid repetition of the header pattern in the packet payload. Manchester encoding also guarantees that the average signal power of the payload is constant, regardless of the specific bit pattern [6].

The operation of the TOAD has been described in [7]. As shown in the dashed box of Fig. 1, a TOAD consists of an optical loop that contains an SOA, which acts as a nonlinear element. The SOA is placed with an offset Δx with respect to the center of the loop. When an optical input pulse enters the TOAD, the pulse power is split by a 50 : 50 coupler into a clockwise (CW) propagating pulse and counterclockwise (CCW) propagating pulse. The optical power of the CW and CCW propagating pulses should be lower than the SOA saturation power, thus, both pulses experience the same gain and phase shift when passing through the SOA. Hence, if no control pulse is present, the recombined CW and CCW propagating pulses reflect back at the TOAD input port. The role of the control pulse that is coupled into the loop via a 90 : 10 coupler is to create a refractive index change in the SOA. If the control pulse arrives at the SOA after the CW propagating pulse has passed through but before the CCW propagating pulse arrives at the SOA, the CW and CCW propagating pulses no longer experience the same gain and refractive index. This leads to the creation of a pulse at the TOAD output [7]. The polarization of the control light that is orthogonal with respect to the polarization of the input pulses. Thus, the control light can be removed by using a PBS.

The TOAD can function as a header processor as follows. The HPP output pulses form the TOAD input signal and are split by an 80 : 20 coupler in a low-power CW and CCW propagating data signal and a high-power control signal. The CCW propagating pulses arrive at the SOA a time $\tau_{sw} = 2\Delta x/v_g$ later with respect to the CW propagating pulses. If no control is present the data signal is reflected back to the TOAD input. The first pulse of high power control signal is used to saturate the SOA.
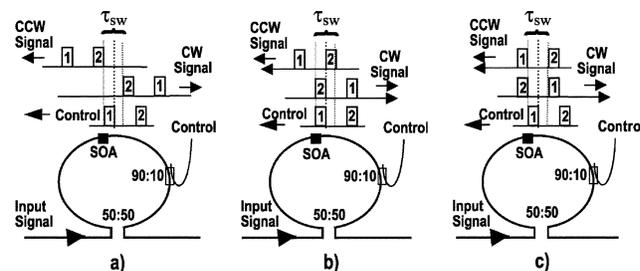

Fig. 2. Timing of the control pulses for the three relevant cases for the operation of the header processor. (a) The control arrives at the SOA after all the pulses have passed the SOA. (b) The control arrives at the SOA after the second CW pulse has passed the SOA but before that the second CCW arrives at the SOA. (c) The control arrives at the SOA before both the CW and CCW second pulses arrive at the SOA.

Header recognition can be implemented by accurately timing of the control pulses. There are three interesting cases that are shown in Fig. 2. In the first case [see Fig. 2(a)], the first control pulse arrives at the SOA after the second CCW propagating data pulse. Thus, the control pulse arrives too late at the SOA to create a pulse at the TOAD output. In the second case [see Fig. 2(b)], the control light arrives at the SOA after the second CW propagating data pulse has passed through the SOA, but before the second CCW propagating data pulse arrives at the SOA. Hence, the control light creates a refractive index change in the SOA that is only experienced by the second CCW propagating pulse, so a pulse is created at the TOAD output. In the third case [see Fig. 2(c)], the control light arrives at the SOA before the second CW and CCW pulses. In this case, the SOA refractive index change is experienced by both the second CW and CCW pulses. Thus, no pulse is formed at the TOAD output. The separation of the two pulses should be large enough to ensure that the control light cannot switch the first header pulse.

We conclude that a pulse outputs the TOAD if the time between the two header pulses matches with the timing of the control pulse. The TOAD output pulse can be used to set/reset an optical flip-flop that controls the optical wavelength routing switch, as described in [4]. It is important to notice that in contrast to header recognition based on two-pulse correlation in a SLALOM configuration, this header recognition concept does not critically depend on the SOA recovery time. Hence, the offset of the SOA with respect to the center of the loop and the delays for the control pulses can be made sufficiently small in order for this header processing concept to allow photonic integration.

The concepts described above were demonstrated by using the experimental setup shown in Fig. 1. The laser source had a wavelength of 1550.91 nm and was modulated by a 10-Gb/s Mach–Zehnder modulator, which was driven by a pattern generator. The packet format is also shown in Fig. 1. The duration of the sequence of "0s" that were placed in front of the second header pulse was 0.9 ns. The payload section consisted of Manchester-encoded pseudorandom binary sequence data at a bit rate of 10 Gb/s.

Sequential optical packets with header sections consisting of a hexadecimal "D555 5555 5500 3555" pattern (Header 1) and a hexadecimal "D555 5555 5540 1C55" pattern (Header 2) were used in the experiments [see Fig. 3(a)]. This means that the time between the header pulses are 5 and 5.1 ns for Header 1 and
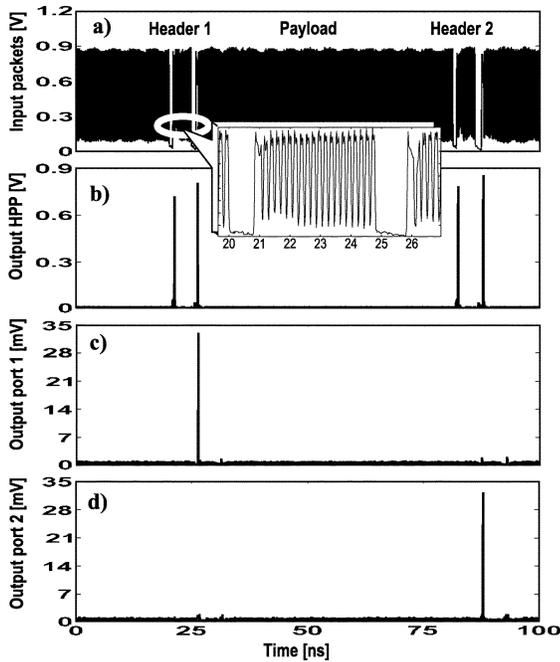
Fig. 3. Measured oscilloscope traces. (a) The optical data packets that input the header processor. Packets with two different headers are shown. The inset shows details of the packet header. (b) The output of the HPP. It is clearly visible that only pulses synchronized with the leading edge of the header bits output the HPP. (c) Output at Port 1. It is visible that only Packet 1 is recognized. (d) Similar to (c), but now for Packet 2.

Header 2, respectively. The packets are first preprocessed by the HPP. The average optical power of the packets at the input of the HPP was 2.3 dBm. The extinction ratio of the input optical data packet was 12 dB. The SOA in the HPP was pumped with 123.5 mA of current. The PBS has an extinction ratio of 30 dB. The oscilloscope trace of the signal that outputs the HPP is presented in Fig. 3(b). It is clearly visible in Fig. 3(b) that the HPP generates a pulse at the leading edges of the header bits. The pulses have a duration of 50 ps each. The average payload suppression is 18.4 dB. The HPP output is than split by an $80:20$ coupler to create the input and control signals of the TOADs. The input and control signal are split by $50:50$ couplers before being distributed over the TOADs. For both TOADs, τ_{sw} is 50 ps. The control signals were delayed by 4.95 and 5.05 ns before being fed in TOAD 1 and TOAD 2, respectively. The SOAs in TOAD 1 and TOAD 2 were pumped with 116 and 121 mA of current, respectively. The energy of the input pulses was 50 fJ while the energy of the control pulses was 0.8 pJ. According to the design of the TOADs and the header patterns, we expect that a pulse is formed at output Port 1 only for packets with Header 1 and a pulse is formed at output Port 2 only for packets with Header 2. The traces of the output Port 1 and output Port 2 are shown in Fig. 3(c) and (d), respectively. It is clearly visible that indeed a pulse is formed at output Port 1 only for packets with Header 1 while no pulse is formed for packets with Header 2. We can observe that a pulse is formed at output Port 2 only for packets with Header 2 while no pulse is formed for packet with Header 1. The contrast ratio between the pulse and the suppressed payload is higher than 14.4 dB.

These experiments indicate that the setup presented in Fig. 1 is indeed capable of recognizing two different headers but the concept is scalable so that a larger number of packet headers can be processed. A limitation of this approach is that a packet header only contains two bits of information. The length of the packet header grows linearly with the number of packet header times the header processor's speed ($\sim$100 ps). It should be noted, however, that the processing speed of the header processor can be decreased to 4 ps [7]. This means that the length of header patterns can be reduced with more than a factor 25.

We have shown that the header processing system can distinguish between two different packet headers and the output is sent to two distinct output ports. We believe that this principle can be extended to recognize more header patterns by constructing packet headers that are made out of a sequence of two header bits as shown in this letter.

The design of the header processing system provides several advantages over alternative techniques. The HPP operates asynchronously which means that the header processing system as a whole can be operated in an asynchronous fashion. Also, the system operates at low power. In this letter, the bit rate was 10 Gb/s and τ_{sw} was 50 ps, but optical switching of a 250-Gb/s signal has been demonstrated using a TOAD for which τ_{sw} was 4 ps [2], [7]. Thus, we believe that the header processor can operate at higher bit rates than 10 Gb/s. Moreover, a shorter offset time in the order of few picoseconds allows photonic integration of the header processor. Finally, a header processing system that can recognize a large number of header patterns can be utilized in devising an all-optical packet switch.

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