# A CMOS V-I converter with 75dB SFDR and 360uW power consumption

# A CMOS *V–I* Converter With 75-dB SFDR and 360-$\mu$W Power Consumption

Sotir Ouzounov, *Student Member, IEEE*, Engel Roza, Johannes A. (Hans) Hegt, *Senior Member, IEEE*, Gerard van der Weide, and Arthur H. M. van Roermund, *Member, IEEE*

***Abstract*—This work describes a method for analysis of voltage-to-current converters (*V–I* converters or transconductors) and a novel *V–I* converter circuit with significantly improved linearity. The new circuit utilizes a combination of cross-coupling and local resistive feedback for a significant, simultaneous suppression of the third- and fifth-order harmonic distortion components in the transconductor characteristics. An evaluation of the optimal circuit dimensioning is shown. Simple and robust design rules are derived for the chosen operation conditions. The transistor implementation is presented and a prototype *V–I* converter is realized in a digital 0.18-$\mu$m CMOS technology. The measured spurious-free dynamic range is 75 dB in a frequency band of 10 MHz. The circuit occupies less than 0.02 mm$^2$ and dissipates 360 $\mu$W.**

***Index Terms*—CMOS transconductors, harmonic balancing, linearization.**

## I. Introduction

CIRCUITS that convert the voltage applied to their input terminals into output current are generally referred to as transconductors or *V–I* converters. These circuits are basic building blocks in many applications. The precision of the *V–I* conversion, with respect to the introduced distortion and noise, can be a limiting factor for the precision of the overall signal processing. There are numerous works that treat the improvement of the *V–I* conversion, in different application contexts and via different techniques [1]–[6]. In some recent, high performance designs [7], [8] a combination of linearization techniques is used. In this paper, first, an approach for a generalized mathematical treatment of the *V–I* function is suggested. It explains and confirms the potential of the combined linearization techniques to achieve better linearity. Second, a new circuit solution based on MOS differential pairs is described as an example of the implementation of that approach. Then the realization of this circuit is shown and the performance-limiting factors are discussed.

Manuscript received November 12, 2004; revised January 27, 2005. This work was supported in part by the Dutch Technology Foundation STW under Project ECS.5455.

S. Ouzounov is with the Department of Electrical Engineering, Mixed-Signal Microelectronics Group, Technical University of Eindhoven, EH 5.15 Eindhoven, The Netherlands (e-mail: S.Ouzounov@tue.nl).

E. Roza was with Philips Research Laboratories, 5656AA Eindhoven, The Netherlands (e-mail: e.roza@philips.com).

J. A. Hegt and A. H. M. van Roermund are with the Department of Electrical Engineering, Mixed-Signal Microelectronics Group, Technical University of Eindhoven, The Netherlands (e-mail: J.A.Hegt@ele.tue.nl; A.H.M.v.Roermund@tue.nl).

G. van der Weide is with Philips Research Laboratories, 5656AA Eindhoven, The Netherlands (e-mail: gerard.van.der.weide@philips.com).

Digital Object Identifier 10.1109/JSSC.2005.847496

## II. Linearization of the *V–I* Function

The operation of the *V–I* converter is described by the function $i_o = f(v_i)$, where $v_i$ and $i_o$ are, respectively, the applied input voltage and the output current. For a differential circuit in equilibrium (symmetric biasing and lack of excitation signal) the function $f_{v_i}$ reduces to a constant: the static transconductance value $G_m$. The transconductor circuit is linear for a certain input voltage range: $\Delta v_i$, if for that range $G_m$ is equal to the equilibrium value. The influence of the circuit parameters on the linearity of $G_m$ can be investigated via a Taylor expansion of the $i_o = f(v_i)$ function around the equilibrium point. For a fully differential circuit this expansion is given in the form

$$i_o(t) = \alpha_1 v_i(t) + \alpha_3 v_i^3(t) + \alpha_5 v_i^5(t) + \alpha_7 v_i^7(t) + \dots \quad (1)$$

where the $\alpha_i$ parameters are determined from the particular circuit implementation. For a harmonic input of the type $v_i(t) = v_m \cos \mu t$, and after grouping of the frequency components, (1) can be rewritten in the form

$$\begin{aligned} i_o(t) = {} & (\alpha_1 v_m + \dots)\cos \mu t \\ & + \left(\frac{1}{4}\alpha_3 v_m^3 + \frac{5}{16}\alpha_5 v_m^5 + \frac{21}{64}\alpha_7 v_m^7 + \dots\right)\cos 3\mu t \\ & + \left(\frac{1}{16}\alpha_5 v_m^5 + \frac{7}{64}\alpha_7 v_m^7 + \dots\right)\cos 5\mu t \\ & + \frac{1}{64}\alpha_7 v_m^7 \cos 7\mu t + \dots . \end{aligned} \quad (2)$$

From (1) and (2), the goal of the linearization would be to design and parameterize a circuit solution in a way that the harmonic content is significantly suppressed. For example, a simultaneous minimization of the parameters $\alpha_3$ and $\alpha_5$ in (1) and (2) would lead to a major suppression of the third harmonic and a simultaneous reduction of the fifth. That would require a circuit with enough degrees of freedom—a combination of parameters that would allow cancellation or significant suppression of $\alpha_3$ and $\alpha_5$. As it will be shown, such a circuit can be implemented via a combination of two cross-coupled resistor-degenerated CMOS pairs (Fig. 1).

## III. *V–I* Converter Analysis and Design

In Fig. 1, the proposed circuit solution is shown. The basic transconductor core consists of two input pairs $\mathrm{M_1}$–$\mathrm{M_2}$ and $\mathrm{M_3}$–$\mathrm{M_4}$. Each of these pairs has a local resistive feedback and a split tail current source implemented, respectively, via $\mathrm{R_1}$ and $\mathrm{R_2}$, and $\mathrm{I_1}$, and $\mathrm{I_2}$. The two input pairs are cross-coupled at their drains.

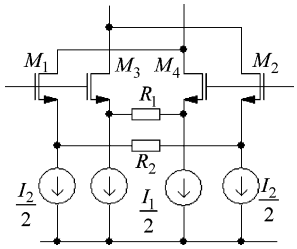



Fig. 1. Basic transconductor circuit.

### A. Initial Assumptions

The circuit is analyzed according to the approach described above with the following initial assumptions.

- The circuit solution is regarded as fully balanced (differential). In such a case, all even-order distortion components can be neglected. In a practical situation, the device matching and the bandwidth of the common-mode operation are limiting factors. Those will be discussed in Section IV-B.
- The basic quadratic dependence [9] for a CMOS differential pair in saturation, with tail current $I$ and $\beta = \mu_n C_{\rm ox} W/L$ is used in the formula

$$i_o = \frac{1}{2} v_i \sqrt{I\beta} \sqrt{1 - \frac{\beta v_i^2}{4I}}. \tag{3}$$

  The channel length modulation is initially neglected. For the submicron process that was used for prototyping, this assumption might be an oversimplification. This will be discussed further in Section IV-A.
- The reactive effects in the circuit are not included in the mathematical evaluation. The static and the dynamic linearity (the response of the system to dc and harmonic input excitations) are assumed equal for low frequencies. The actual bandwidth and the reactive effects are discussed in Section IV.

The $i_o = f(v_i)$ relation for the circuit of Fig. 1 can be derived in the following steps. First, the $v_i = g(i_{o,k})$ relation (4) for the two input pairs is derived. This inverse expression of the input-output function is used due to the simplicity of the derivation

$$v_{i,1} = v_{i,2} = v_i = i_{o,k} R_k + \sqrt{\frac{I_k + 2i_{o,k}}{\beta_k}} - \sqrt{\frac{I_k - 2i_{o,k}}{\beta_k}} \tag{4}$$

where the index $k = 1, 2$ refers to pair one and pair two. Second, the two equations (4) are Taylor expanded and represented in the inverse form: $i_{o,k} = f(v_i)$, and finally the cross-coupling is taken into account via a subtraction of the output currents: $i_{o,tot} = i_{o,1} - i_{o,2}$. The resulting expressions for the $\alpha_i$ coefficients in representation (1) are as follows:

$$\alpha_1 = \left( \frac{1}{R_1 + \sqrt{\frac{4}{I_1\beta_1}}} - \frac{1}{R_2 + \sqrt{\frac{4}{I_2\beta_2}}} \right) \tag{5.1}$$

$$\alpha_3 = \left( \frac{1}{I_1^2 \sqrt{I_1\beta_1} \left( R_1 + \sqrt{\frac{4}{I_1\beta_1}} \right)^4} - \frac{1}{I_2^2 \sqrt{I_2\beta_2} \left( R_2 + \sqrt{\frac{4}{I_2\beta_2}} \right)^4} \right) \tag{5.2}$$

$$\alpha_5 = \left( \frac{7I_1\beta_1 \left( R_1 + \sqrt{\frac{4}{I_1\beta_1}} \right) - 12\sqrt{I_1\beta_1}}{4I_1^5 \beta_1 \sqrt{I_1\beta_1} \left( R_1 + \sqrt{\frac{4}{I_1\beta_1}} \right)^7} - \frac{7I_2\beta_2 \left( R_2 + \sqrt{\frac{4}{I_2\beta_2}} \right) - 12\sqrt{I_2\beta_2}}{4I_2^5 \beta_2 \sqrt{I_2\beta_2} \left( R_2 + \sqrt{\frac{4}{I_2\beta_2}} \right)^7} \right) \tag{5.3}$$

Equations (5.$x$) give the relation between the circuit parameters that can ideally fully eliminate the unwanted harmonic content. However, they are rather cumbersome and at the same time create a multidimensional design space. In order to derive implementable design rules from the above relations they are further simplified, as follows.

### B. Parameterization and Optimization Procedure

A simple approach that gives more insight in the circuit operation and reflects its structure is to represent the parameters of the two transistor pairs as ratios, i.e., as a relation between the dimensioning of the two pairs

$$\frac{I_1}{I_2} = p \quad \frac{\beta_1}{\beta_2} = q \quad \frac{R_1}{R_2} = x. \tag{6}$$

Then using (5) and (6), (1) is rewritten in the form

$$i_o = \rho[p,q,x] v_i - \psi[p,q,x] v_i^3 - \zeta[p,q,x] v_i^5 - \omega[p,q,x] v_i^7 - \ldots \tag{7}$$

where $\alpha_3 = \psi[p,q,x]$ and $\alpha = \zeta[p,q,x]$. The ratios (6) were determined after an optimization procedure of (7). The goal of the optimization was to find a global optimum that would lead to a cancellation or significant suppression of the harmonic content and would not greatly deteriorate the signal component. The optimization range was bounded for practically implementable ratios (good matching for a reasonable chip area). Several observations have to be pointed out:

- The linearization mechanism is to a great extent independent of the absolute values of the design parameters (current consumption, resistors and transistor sizes). As argued later, when those are increased, the linear input range also increases.
- Primary concerns for the choice of absolute parameter values are the application specifications for noise and bandwidth.
- The impact of the technology with respect to the available voltage room has to be taken into account.

The optimization procedure showed that the third- and fifth-order harmonic components are minimized, for

$$p = 8 \quad q = 2 \quad x = 0.25. \tag{8}$$

Moreover, the functions $\psi[p,q,x]$, $\zeta[p,q,x]$ have rather flat minima (see Figs. 2 and 3), so the minimization of the harmonics is not very much dependent on the absolute accuracy (matching) of the ratios (8). Due to this flat optimum, the linearization is also robust to technology spread and temperature variations. By substitution of dependencies (8) into (5.1), it is estimated that the transconductance value $G_m$ of this circuit is decreased by 25% with respect to that of a single differential pair with the same size and current settings, while $\alpha_3$ and $\alpha_5$ are ideally fully cancelled. This small reduction of the intrinsic transconductance

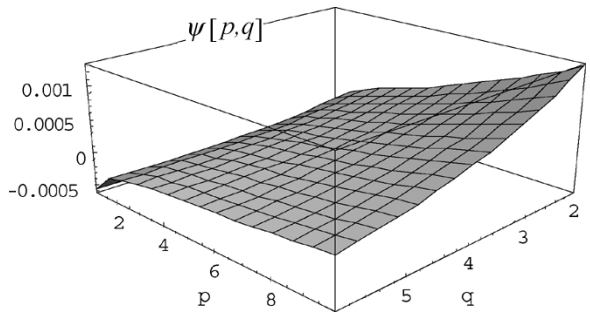



Fig. 2. Graphical evaluation of the optimal parameterization for the $v_i^3$ harmonic component.

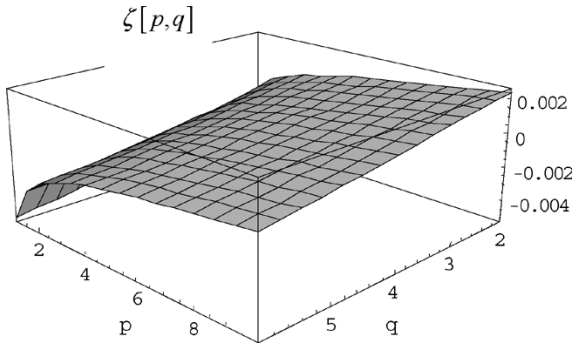



Fig. 3. Graphical evaluation of the optimal parameterization for the $v_i^5$ harmonic component.

makes possible the realization of the required linearity and noise specification with relatively low power consumption.

Up to now, we established optimal ratios between the two parts of the proposed *V–I* converter that would lead to minimal harmonic content. The actual circuit dimensioning is done in the context of a particular application that sets the requirements toward the current consumption, signal-to-noise-and-distortion ratio (SNDR), and bandwidth. The proposed circuit was used as a building block in a $G_m$-$C$ filter for a continuous-time sigma-delta modulator. The specifications are defined as a SNDR of 75 dB, a maximal differential input signal of 400 mV peak-to-peak, and a bandwidth of 10 MHz.

The input dynamic range is estimated by solving (4) for the boundary condition $2i_o = I$, when only one transistor in the input pairs carries the entire tail current, ideally assuming the other is fully off. That corresponds to

$$\Delta v_i = \frac{I_k R_k}{2} + \sqrt{\frac{4I_k}{\beta_k}} = \frac{I_k R_k}{2} + \sqrt{\frac{2}{(V_{GS,k} - V_{t,k})}} \quad (9)$$

where $V_{t,k}$ are threshold voltages of the input transistors. From (6) and (9), the two input pairs have different dynamic ranges due to the different dimensioning. The dynamic range with maximal linearity for the whole *V–I* converter is then determined by the dynamic range of the smaller pair [pair 2, according to (6)]. After the overload of the smaller pair the stage operates close to a single, resistor-degenerated pair. This behavior is illustrated in Fig. 4.

Formula (9) gives an indication for the required currents, biasing, and resistor values. An important note is that the resistors $R_k$ are just modifying the transconductance characteristics and

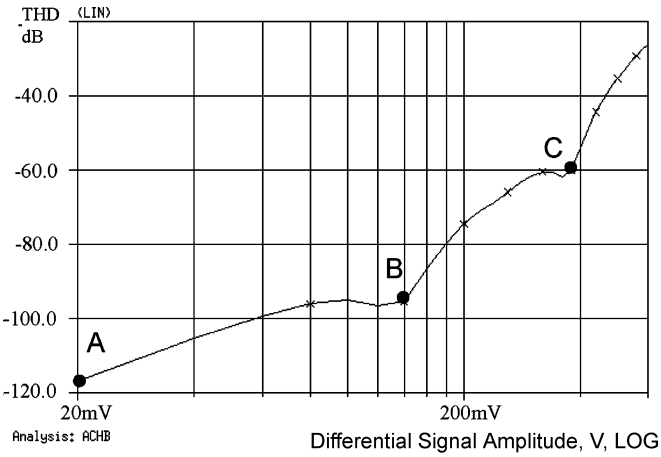



Fig. 4. Simulated THD, 5–MHz input, A-B region with maximal linearity, B-C region single degenerated pair operation.

can be quite small with respect to the reciprocal of the transconductance of the complete stage. For the final transistor sizing, the following nonidealities are taken into account.

## IV. Nonidealities in the Transconductor Implementation

### A. Thermal and Flicker Noise

The thermal output noise current of the *V–I* converter is a combination of the noise generated in the input pairs, the tail current sources, the active load, and the degeneration resistors. An analysis of the influence of the combination of the two pairs on the noise and the signal-to-noise ratio (SNR) shows that the noise increases due to the cross-coupling of two pairs with different sizes to a much less extent than the linear input dynamic range. That leads to an improvement of the overall SNR.

In the submicron process that was used for prototyping, the flicker noise also has a significant impact in the frequency range of interest. In the current design, a simple increase of the device sizes was used to decrease the flicker noise. A transistor length of $L \approx 10L_{\min}$ ($L_{\min} = 0.18\ \mu$m) was used for the transistors that determine the noise performance. The width (the W/L ratio) is determined from the requirements discussed up to now. The increased transistor sizes lead to two additional benefits:

- the effect of the channel length modulation is significantly decreased;
- the larger size of the devices assures better matching.

### B. Mismatch and Reactive Effects

As already stated, the linearization mechanism is rather insensitive to mismatch. Moreover, the target bandwidth specification of 10 MHz is relatively modest for the chosen technology for prototyping. That allows a significant increase of the device sizes and additionally alleviates a possible matching problem. The evaluation of mismatch showed that the even-order harmonics remain significantly lower (at least 5 dB) than the odd-order terms. However, in the layout special care was taken for a very good symmetry between the two differential branches and equal electrical and mechanical environment.

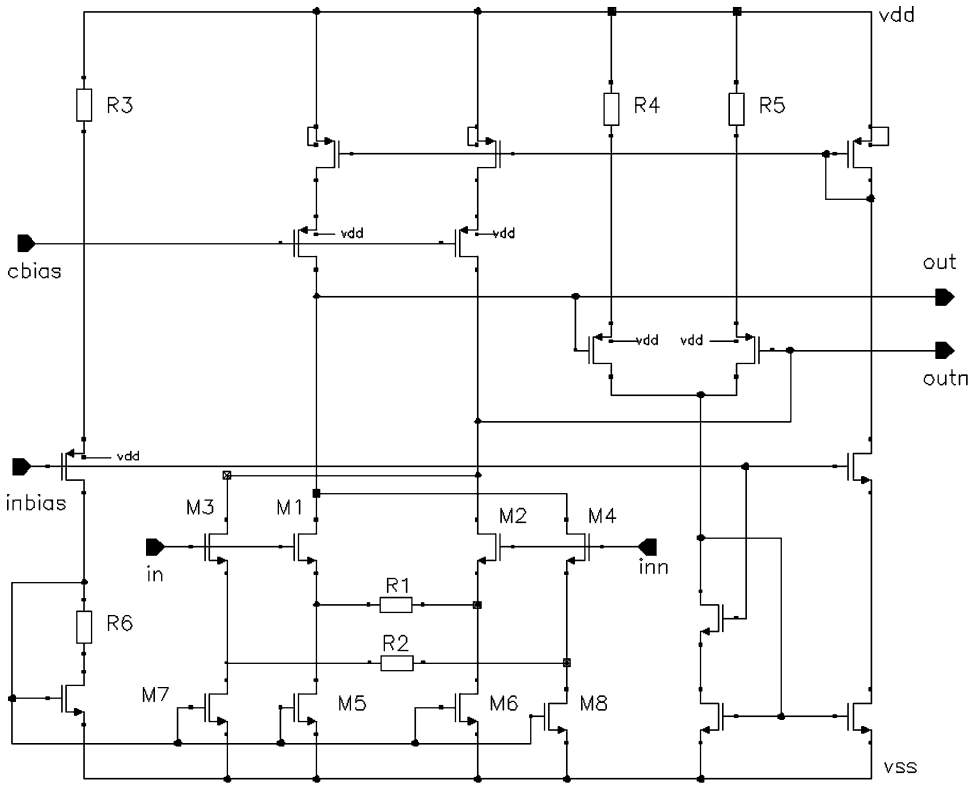



Fig. 5. Circuit schematic of the proposed *V–I* converter.

The full circuit schematic including the common-mode feedback is shown in Fig. 5.

In the design of the stage, care is taken that the following reactive effects do not decrease the performance in the specified band of operation:

- the decrease of the common-mode rejection ratio at high frequencies due to the source capacitances of the differential pairs;
- the bandwidth of the common-mode feedback;
- the different frequency responses of the two input pairs due to their different sizes (8).

## V. Experimental Results

The *V–I* converter was fabricated in a standard 0.18-$\mu$m five-metal digital CMOS process. The resistors are implemented in the n+ poly layer. The occupied area is less than 0.02 mm$^2$ and 200 $\mu$A are consumed from a 1.8-V power supply.

The evaluation of a standalone *V–I* converter is very complicated because of the very low level of the output signal. The difference between the two output currents is converted into a voltage across an external resistor and this voltage is then measured. For a correct evaluation, this resistor should be small with respect to the output impedance of the stage, so that the operation of the circuit is not influenced. A 10-k$\Omega$ resistor was used whereas the output impedance the *V–I* converter is approximately 1.5 M$\Omega$. A second limitation is the limited bandwidth of the setup due to the capacitive load built-up by the internal protection ring and the packaging. This load was estimated to be in the order of 2 pF.

TABLE I
Maximal Measured INL, % Full Scale ($\Delta V_i$)

| $\Delta V_i$, peak-to-peak | INL, %FS |
|---|---|
| 200mV | 0.08 |
| 400mV | 0.1 |
| 600mV | 0.6 |

Fifteen ICs from a single batch were evaluated via static and dynamic measurements.

### A. Static Measurements

Via a static measurement, the output signal as a function of a dc sweep of the input voltage was established. The measurement was done with a digital multimeter in differential mode. For a quantitative evaluation, the integral nonlinearity (INL) was calculated. The measured characteristic was subtracted from an ideal straight line generated via a least mean square (LMS) fit. The results are summarized in Table I.

### B. Dynamic Measurements

The dynamic performance of the *V–I* converter was evaluated with the measurement setup shown in Fig. 6. The output of the signal generator (SG) was low-pass filtered in order to assure spectral purity of the input signal. At the input and at the output, respectively, single-ended-to-differential and differential-to-single-ended conversion of the signals was done via

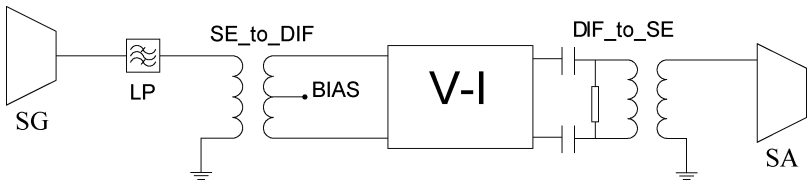



Fig. 6. Dynamic measurements setup.

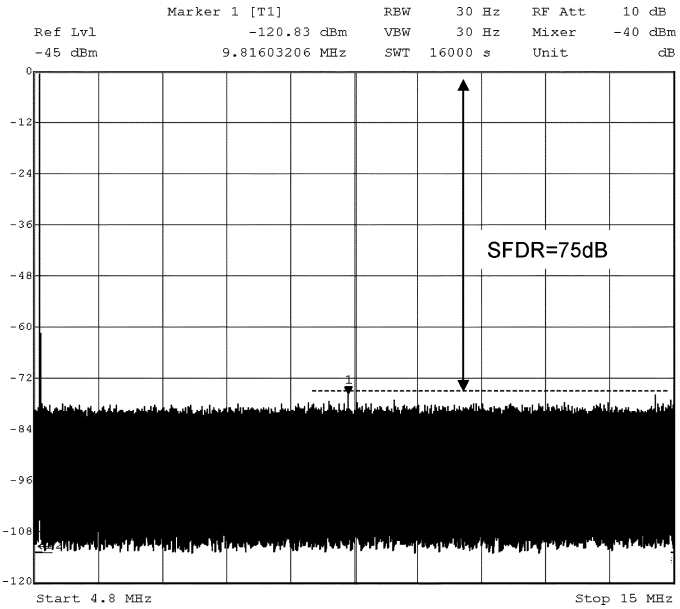



Fig. 7. Measured SFDR with 4.9-MHz sine input signal in a frequency band between 4.8 and 15 MHz.

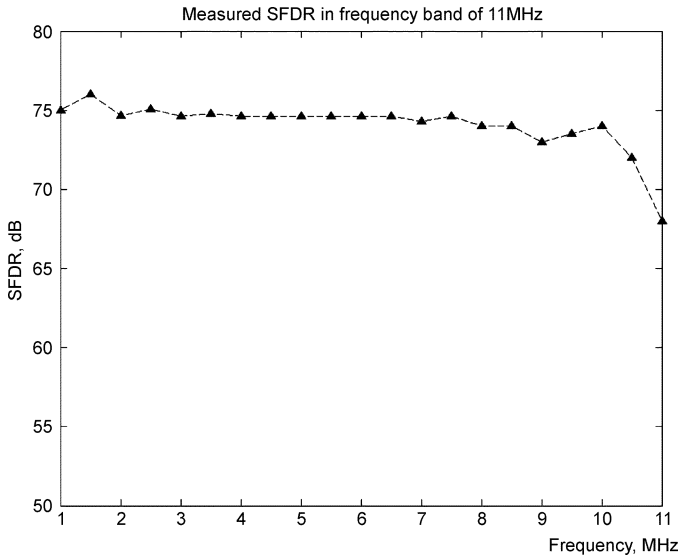



Fig. 8. SFDR with respect to the frequency of the input signal.

TABLE II
SUMMARY OF MEASURED PERFORMANCE OF THE *V–I* CONVERTER

| | |
|---|---|
| Technology | 0.18 $\mu$m, CMOS |
| Supply Voltage | 1.8V |
| Area | <0.02 mm$^2$ |
| Vin,$_{PP}$ | 400mV |
| SFDR [0-10MHz] | 75dB |
| SNR [1k-8MHz] | 70dB |
| Current Consumption | 200 $\mu$A |

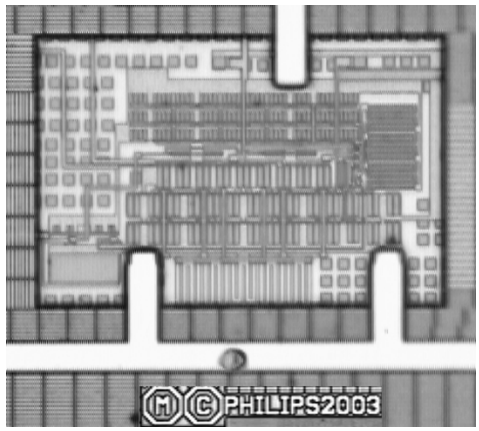



Fig. 9. Chip photograph.

transformers. The output signal was measured with a spectrum analyzer (SA) in a low-distortion mode. Due to the very small levels of the measured signal, the resolution of the measurement setup was limited to 78 dB. A second harmonic at $-75$ dBFS that originates from the limited dynamic range of the spectrum analyzer in a low-distortion mode is limiting the measurable SFDR.

For a full-scale 4.9-MHz input signal, a SFDR of 75 dB was measured (Fig. 7).

This SFDR is determined from the second harmonic distortion component as stated above. The third harmonic is 1–3 dB lower than the second harmonic in all measured samples. The distortion behavior with respect to the frequency of the input signal is plotted in Fig. 8. The measured SFDR is almost flat up to approximately 10 MHz. For higher frequencies, the SFDR starts to decrease, mainly due to the attenuation of the signal component. In turn, both even- and odd-order harmonics start to increase, mainly due to the different frequency behavior of the larger main differential pair and the smaller supplementary pair. That deteriorates the effectiveness of the harmonic suppression.

The IC specifications are summarized in Table II, and in Fig. 9, a die photograph is shown.

## VI. CONCLUSION

The possibility to design transconductors with improved linearity via a combined application of linearization techniques was investigated. An integrated CMOS *V–I* converter has been presented that achieves an SFDR of 75 dB for a differential input signal of 400 mV peak-to-peak in 1.8-V technology. The low

power consumption of 360 $\mu$W is due to the utilized linearization principle that allows simultaneous suppression of third- and fifth-order harmonic components in the *V–I* characteristic with only 25% decrease of the transconductance of the basic differential pair. Due to the flat optimal parameterization, the circuit is relatively robust to process spread and temperature variations.

A boosting of the output current is recommended in order to facilitate the measurement of the standalone *V–I* converter and show the full potential of the presented technique.

## REFERENCES


[1] A. T. van Zanten, "An accurate integrated voltage-to-current converter," *IEEE J. Solid-State Circuits*, vol. 10, no. 6, pp. 432–436, Dec. 1975.

[2] H. Tanimoto, M. Koyama, and Y. Yoshida, "Realization of a 1-V active filter using a linearization technique employing plurality of emitter-coupled pairs," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 388–397, Jul. 1991.

[3] H. Voorman and H. Veenstra, "Tunable high-frequency Gm-C filter," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1097–1108, Aug. 2000.

[4] K. Kimura, "A linear transconductance amplifier obtained by realizing a floating resistor," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 45, no. 1, pp. 108–113, Jan. 1998.

[5] E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *IEE Proc. Circuits, Devices Syst.*, vol. 147, no. 1, pp. 3–12, Feb. 2000.

[6] R. H. Zele and D. J. Allstot, "Low-power CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 157–168, Feb. 1996.

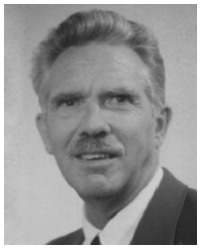
[7] K.-C. Kuo and A. Leuciuc, "A linear MOS transconductor using source degeneration and adaptive biasing," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 10, pp. 937–943, Oct. 2001.

[8] U. Chilakapati, T. S. Fiez, and A. Eshraghi, "A CMOS transconductor with 80 dB SFDR up to 10 MHz," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 365–370, Mar. 2002.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001, pp. 107–118.


**Sotir Ouzounov** (S'95) was born in Pazardjik, Bulgaria, in 1973. He received the M.Sc. degree in electrical engineering from Sofia Technical University, Sofia, Bulgaria, in 1997. Since 2000, he has been working toward the Ph.D. degree in the Mixed-Signal Microelectronics group, Technical University Eindhoven, The Netherlands.

His current research interests are in high-speed sigma-delta A/D converters and associated circuits.



**Engel Roza** joined Philips Electronics in 1965 and has been with the Philips Research Laboratories, Eindhoven, The Netherlands, since 1970. From 1985 to 1999, he headed the Digital VLSI Group in Philips Research. The group's program covered programmable architectures, architectural synthesis, embedded memories, circuit innovation and applied DSPs. Currently, he has a special assignment as Management Team Advisor for Systems on Silicon. As a researcher, he has been active in radio and television receivers, optical character recognition, and digital and optical communications. He holds over 25 U.S. patents and has written many publications in international journals. His research interest is in theory, applications and implementations of nonlinear feedback loops in signal processing, e.g., phase-lock loops for synchronization, decision feedback equalization, synchronous and asynchronous sigma-delta modulation, and recursive bitstream conversion.

**Johannes A. (Hans) Hegt** (M'97–SM'01) was born on June 30, 1952, in Amsterdam, The Netherlands. He studied Electrical Engineering at the Eindhoven University of Technology (TU/e), where he graduated with honors in 1982. In 1988, he received the Ph.D. degree from TU/e on synthesis of switched-capacitor filters.

From 1983 to 1986, he was an Assistant at the TU/e. Since 1987, he has been a Lecturer at this University, where he gives courses in the areas of switched-capacitor filter engineering, switched current filters, digital electronics, microprocessors, digital signal processing, neural networks, nonlinear systems and mixed-signal systems. Since 1994, he has been an Associate Professor on mixed analog/digital circuit design. He is currently especially involved in the hardware realization of ADCs and DACs.

**Gerard van der Weide** was born in 't Harde, The Netherlands, on November 23, 1971. He received the M.Sc. degree in electrical engineering from Twente University of Technology, Enschede, The Netherlands, in 1995.

In 1995, he joined the Mixed-Signal Circuits and Systems group of Philips Research Laboratories, Eindhoven, The Netherlands, where he has been working on high-speed A/D converters and associated circuits. Currently, he is involved in the design of mixed-signal and RF circuits for wireless connectivity systems.

**Arthur H. M. van Roermund** was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in electrical engineering from the Delft University of Technology in 1975 and the Ph.D. degree in applied sciences from the K.U.Leuven, Belgium, in 1987.

From 1975 to 1992, he was with Philips Research Laboratories in Eindhoven, The Netherlands. From 1992 to 1999, he was a full Professor in the Electrical Engineering Department of Delft University of Technology, where he was Chairman of the Electronics Research Group and member of the management team of DIMES. From 1992 to 1999, he was Chairman of a two-year post-graduate school for "chartered designer". From 1992 to 1997, he was a consultant for Philips. In October 1999, he joined Eindhoven University of Technology as a full Professor, chairing the Mixed-Signal Microelectronics Group. Since September 2002, he has also been Director of Research of the Department of Electrical Engineering. He is Chairman of the board of ProRISC, a nationwide microelectronics platform. He is a member of the supervisory board of the Cobra research school.

Dr. van Roermund has been one of the three organizers of the yearly workshop on Advanced Analog Circuit Design (AACD) since 2001. In 2004, he received the Simon Stevin Meester Award for his scientific and technological achievements.