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The development of today's complex electronic products (e.g. mobile phones, Bluetooth) requires accurate computer simulations. For radio frequency (RF) designs in particular, many parts of the physical system, such as IC (integrated circuit) packages, PCBs (printed circuit boards) and printed components (and also the coupling between them) can only be simulated accurately using numerical electromagnetic field analysis [1,2]. In general, this results in very large matrix systems to be solved, which can be virtually impossible.

For the electromagnetic analysis of complex interconnect structures, the layout simulation tool Fasterix was developed. In Fasterix the interconnect structure is discretized and a boundary element method is used to model the structure as a lumped RLC circuit. In the current implementation, the sometimes very large RLC circuit is represented in a compact way by making use of the so-called 'supernode algorithm' [3], which generates a compact equivalent circuit model for use in circuit simulation. However, since the stability of these models is not guaranteed, transient circuit simulations often result in convergence problems.

In order to remedy these instabilities, a number of Reduced Order Modelling (ROM) methods, preserving stability and passivity, have been investigated. ROM replaces large systems by smaller, computationally more flexible ones, with approximately the same behaviour. An important issue in reducing the size of models is the preservation of passivity. In order to be able to use the model in circuit simulation, the realization of an equivalent circuit is essential. In this paper the results of a comparison between a special implementation of the SVD-Laguerre ROM method [4] and the original 'supernode' method, is shown.

The results show that the reduced systems, although much smaller, have the ability to approximate the behaviour of the original system to arbitrary accuracy. Furthermore, the reduced systems are provably stable and passive, and take less evaluation time with a circuit simulator. The main advantage is that transient analysis can now be performed on the layout structures, which was not possible with the original method.

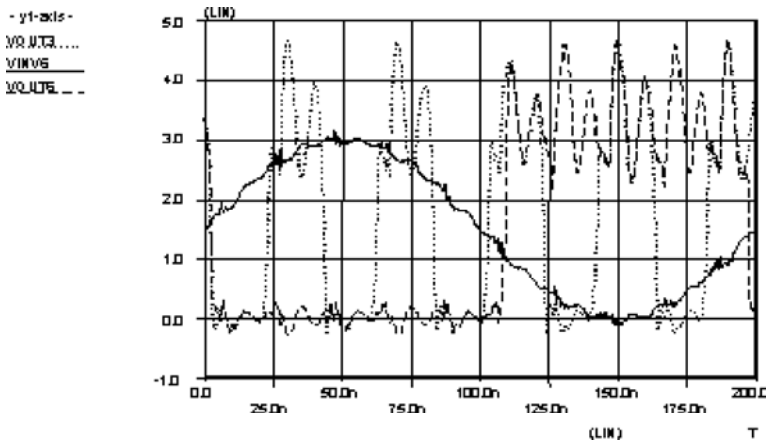

Figure 1. New ROM method allows transient simulation of interconnect structures.

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