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A 34 to 36 GHz Active Transmitarray for Ka-band Tracking Radar Using 5G Tx/Rx Beamforming ICs: Design and 64-Element Demonstrator

Martijn de Kok, Graduate Student Member, IEEE, Cornelis J.C. Vertegaal, Graduate Student Member, IEEE, A. Bart Smolders, Senior Member, IEEE, and Ulf Johannsen, Member, IEEE

Abstract—An active transmitarray antenna is presented for Ka-band monopulse tracking radar in the 34 to 36 GHz range. A novel contribution is the application of commercial SiGe-based 5G beamforming chips in a large-scale naval radar array, demonstrating how developments in Ka-band communications can benefit radar technology. Three arrays of 0.77 m diameter each with 24368, 19424 and 7824 radiating elements are presented to compare amplitude-tapered, space-tapered and hybrid-tapered designs. All designs achieve a sub-1° half-power beamwidth (HPBW), peak side-lobe levels (SLL) below –26 dB and effective isotropic radiated power (EIRP) of 100 dBm at broadside with a ±60° grating-lobe-free scanning range. Furthermore, a small-scale demonstrator is realized and presented that consists of an eight-layer printed circuit board with 8 × 8 patch antennas on one side, and a 4 × 4 open-ended waveguide feed-array with beamforming chips and integrated liquid cooling channels on the other. After over-the-air calibration, the realized array achieves a peak EIRP of 56 dBm, a 12° HPBW and the ability to scan to ±60° in the H-plane with cos θ scan loss and no grating lobes. E-plane scanning is achieved up to ±45° with cos θ1.1 scan loss.

Index Terms—Ka-band, transmitarray, phased array, beamforming, SiGe, tracking radar, monopulse, space tapering

I. INTRODUCTION

RADAR and mobile communications share several challenges in the pursuit of improved performance. The increasingly limited availability of the required radio frequency (RF) bandwidth for sensing resolution and data throughput is driving developments towards millimeter-wave (mm-wave) operating frequencies: the fifth generation mobile network (5G) spectrum allocation includes sections of the Ka-band (26.5-40 GHz), which is already used for satellite communication (SATCOM) uplinks and short-range radars with better resolution and compactness than S- and X-band systems [1]–[3]. Moreover, a trend can be observed towards even smaller and more wide-band devices operating beyond 100 GHz [4].

The significant path losses at mm-wave, particularly due to rain and atmospheric attenuation losses at Ka-band, impose high effective isotropic radiated power (EIRP) requirements leading to a demand for high antenna gain and transmit power [5]. As a result, active electronically scanned phased arrays (AESAs) have been receiving notable attention for a wide range of mm-wave applications: with rapidly steerable high-gain beams they can enable low inter-user interference in 5G, uninterrupted links with fast-moving satellites, and tracking of multiple radar targets [6]–[8]. Recent advances in off-the-shelf silicon and silicon germanium (SiGe)-based beamforming integrated circuits (BFICs) has enabled the mass-production of low-cost mm-wave AESAs for commercial SATCOM systems and 5G base stations [9]. These advances are expected to benefit radar technology as well.

Ka-band monopulse sensors as presented in [10]–[14] commonly use high-gain reflectors or lenses, which must be steered mechanically to scan a wide sector [15]. This is too slow for multi-target and track-while-scan functionalities and defense against hypersonic missiles. This paper presents the design of an active Ka-band transmitarray, demonstrating the novel application of commercial SiGe-based 5G BFICs in a large-scale and high-power naval monopulse tracking radar system. This is the first demonstration of beamsteering with a BFIC-based reconfigurable transmitarray in published literature. The combination of lens-like focusing with per-element 8-bit phase shifting and power amplification results in a rapidly steerable high-EIRP pencil beam to track fast-moving targets.

The remainder of this paper is structured as follows. Section II lists the system requirements and provides an overview of the active transmitarray design. In Section III, three full-scale array designs are presented to compare amplitude- and space-tapered designs. Whilst both tapering techniques improve peak-sidelobe level (SLL) performance at the cost of increased half-power beamwidth (HPBW), space tapering may also alleviate thermal and size, weight, power, and cost (SWaP-C) constraints with fewer, wide-spaced elements [16]–[18].

Furthermore, this article presents a small-scale demonstrator array consisting of a printed circuit board (PCB) with a patch antenna array, an open-ended waveguide (OWEG) feed array with integrated liquid cooling and analog BFICs. The design is presented in Section IV, and measurement results are discussed in Section V. Section VI concludes this paper.

II. TRANSMITARRAY OVERVIEW & REQUIREMENTS

The operating principle of the proposed active transmitarray is depicted in Fig. 1. The complete system, including antenna
Arrays, electronics and circuitry for power supply and digital control, is designed to be implemented in PCB technology to outperform traditional lenses and reflectors in volume, mass and production costs. Compared to conventional PCB-based arrays, a transmitarray offers a higher degree of scalability due to the absence of lossy on-board distribution networks.

A list of system requirements, based on a naval monopulse tracking radar application, is presented in Table I. In this section, a brief state-of-the-art overview on active transmitarrays is provided. Furthermore, the transmitarray subsystems including the beamforming electronics, space feed, antenna array and cooling, are described and linked to these specifications.

A. Active Transmitarrays: State-of-the-art

Whilst passive transmitarrays can be steered by moving the feed position, a range of electronic-scanning implementations with a clear advantage in speed can be found in state-of-the-art overviews such as [19]–[21]. Several strategies to reconfigure the element-level phase shifts can be identified.

PIN-diode-reconfigurable elements are relatively simple to implement, only requiring a single bias line. However, most designs only provide 1-bit phase shifts, leading to severe limitations including sub-optimal EIRP and SLL performance, beam-pointing errors and even spurious lobes [22].

Analog phase shifts can be achieved with varactor diodes or through displacement of conductive fluid in a microfluidic structure. The former method may be subject to varying transmission bands due to capacitance changes whilst scanning, and whilst the latter uses zero power in static conditions it is slow to reconfigure. For both techniques, the designs listed in [19]–[21] generally have insertion losses of several decibels.

Of the aforementioned methods, no examples beyond 30 GHz are listed in the overviews. This is likely due to the limited area and tolerances for component placement. Ka-band designs with switching micro-electromechanical systems (MEMS) have been presented, but have low-resolution phase shifts similar to PIN-diodes and high insertion losses.

Implementing multi-bit electronic phase shifts, particularly at high frequencies, has been identified as a significant research gap in [21] due to biasing network complexity. Moreover, most of the listed designs are lossy structures without an amplification stage, resulting in high feed power requirements. Commercial Ka-band BFICs can tackle both problems with daisy-chained digital control and element-level power amplifiers (PAs), and feature high-resolution phase shifters.

The only published active transmitarray with BFICs to date is presented in [23]. This design consists of a SiGe-based SATCOM BFIC encapsulated between PCBs with K- and Ka-band patch antennas. As only a single submodule was realized, no beamforming performance or active impedance was presented. The submodule dimensions prevent a regular element spacing, limiting the expected grating-lobe free scan range. Moreover, no attention is given to cooling due to the low transmit power of 8 dBm per channel.

The system presented in this contribution is the first demonstration of beam-scanning with a BFIC-based reconfigurable transmitarray in published literature. The mm-wave design achieves a wide grating-lobe-free scan-range with fast, multi-bit phase shifters, and features element-level power amplification. Integrated active cooling enables a high degree of scalability, which is not limited by submodule size. The assembly is simple compared to most stack-ups shown in [19]–[21], allowing for conventional manufacturing techniques.

B. Beamforming ICs

At the core of the proposed transmitarray are SiGe-based quad-channel mm-wave BFICs from NXP Semiconductors. Specifications are listed in Table II, and a functional diagram is shown in Fig. 2. Each channel consists of a transmit (Tx) and a receive (Rx) chain, each with a vector modulator (VM) which can control amplitude and phase with 8-bit resolution through a high-speed digital serial peripheral interface (SPI) bus [24]. A similar BFIC designed for 28 GHz has been used in previous work on AESAs for 5G applications [25]–[27].

The chips considered in this work are early-production prototypes from 2019 designed for the 5G n260 frequency

![Fig. 1: Schematic cross-section depicting the principle of operation and components of the monopulse-transmitarray.](image-url)
band (37-40 GHz). As such, it should be noted that efficiency, manufacturing variations and 1-dB compression output power ($P_{1\text{dB}}$) have been improved in more recent versions of the product line [24]. Although 34-36 GHz is entirely outside of the designed operating band, the amplifiers and VMs of the BFIC still function well throughout this frequency range.

### C. Array diameter, grid & element spacing

The array diameter $d_{ap}$ as specified in Table I was based on the specified HPBW, which can be estimated for a uniformly excited circular aperture and wavelength $\lambda$ using [28]

$$\text{HPBW} \approx 58.9 \frac{\lambda}{d_{ap}} \approx 0.66^\circ,$$

leaving ample margin for SLL reduction.

A symmetric rectangular array lattice was chosen to achieve a low null-depth for the monopulse application [13] and to simplify the division of the array in four symmetric quadrants for ease of manufacture. To maximize the space available for the BFICs, signal routing and cooling, the largest allowed inter-element spacing $d$ is preferred whilst avoiding the appearance of grating lobes. For a rectangular-grid array with a maximum steering angle from broadside $\theta_{0,max}$ and with $\lambda_h$ being the free-space wavelength of the highest operating frequency as specified in Table I, this criterion becomes [28]

$$d \leq \frac{\lambda_h}{1 + \sin \theta_{0,max}} \approx 4.463 \text{ mm},$$

which was rounded down to 4.40 mm for ease of design and robustness. This spacing allows 6092 four-channel BFICs to fit within the specified array aperture as shown in Fig. 3. This results in a total of 24368 antenna elements ($N_{ant}$), each with a directivity that can be estimated from the grid size as

$$D_e = 10 \log_{10} \left( \frac{4\pi d^2}{\lambda^2} \right) = 5.2 \text{ dBi},$$

If the array is excited uniformly at the $P_{1\text{dB}}$ level of the BFICs, the peak achievable broadside EIRP under ideal conditions (i.e. ideal phase settings, no losses) is

$$EIRP_{pk} = D_{array}|dB| + P_{\text{radiated, total}}|dBm$$
$$= [D_e + 10 \log_{10} (24368)] + [P_{1\text{dB}} + 10 \log_{10} (24368)]$$
$$= 108.9 \text{ dBM},$$

leaving nearly 10 dB margin over the specified 99 dBm to account for losses, mismatches, and SLL reduction techniques.

### D. Monopulse horns and space-feeding

The active transmittarray is designed for a pre-existing monopulse horn array as shown in Fig. 1. However, for the sake of brevity and simplicity, the feed source is modeled as a single 12 dBi gain horn as illustrated in Fig. 3. This horn illuminates a planar antenna array, and the BFICs compensate for the non-uniform phase front indicated as $\Delta V$ in Fig. 1.

Due to the four-way split in the BFICs, the space-feed side of the array has an approximate full-wavelength element spacing. This sparse lattice is acceptable due to the lack of a wide-scanning requirement on the feed side, but it limits the aperture efficiency. This could be compensated for with larger, higher-gain elements, leading to an area trade-off as the feed-side should also accommodate the BFICs and cooling solution.

### E. Cooling system

Radar systems differ from 5G and SATCOM arrays in terms of linearity and power requirements. Whilst the 5G BFICs are designed mainly for back-off conditions, in pulsed radars the output-stage PA.s are frequently pushed into compression. This may result in thermal power output beyond the BFIC package capability, and decrease chip lifetime and performance. In the full-scale array where thousands of BFICs in compression may dissipate kilowatts of combined thermal power, a highly scalable cooling solution is called for. Particular attention is directed at co-designing the feed array and cooling and integrating both functionalities in a single subsystem.

### III. FULL-SCALE SYSTEM MODELING AND DESIGN

A model was built in MATLAB to rapidly generate and assess the performance of preliminary full-scale array designs. This section describes this model and presents three design concepts to meet the requirements of Table I.

#### A. Space-feed model

The feed horn is aligned with the feed array center at a distance of $D_{ap}/2$ as shown in Fig. 3, ensuring all elements are within 45° from boresight. The power received by each BFIC-connected feed element, $P_{IC}$, is determined from a given feed power $P_{fd}$ using the Friis transmission equation, given by [29]

$$\frac{P_{IC}}{P_{fd}} = G_{fd}(\theta)G_{sf}(\theta) \left( \frac{\lambda}{4\pi R(\theta)} \right)^2$$

where $G_{fd}(\theta)$ and $G_{sf}(\theta)$ denote the realized gain patterns of the feed-horn and space-feed array elements, respectively, and $R(\theta)$ denotes the distance from the feed horn to an array element at angle $\theta$ from boresight.

The sparse feed array could accommodate high-gain elements up to 11.2 dBi according to an analysis similar to (3). However, a more conservative 6 dBi element was modeled to leave room for the BFICs and cooling. The resulting power distribution shown in Fig. 3 rolls off by around 15 dB from the array center to the edge. In this case, 28.3% of $P_{fd}$ is received by the feed array. For comparison, the 11.2 dBi elements achieve a power transfer of 62% with a 22.4 dB roll-off.
Fig. 3: Space-feed model side-view showing the gain horn and feed array (left) and the input power distribution (right).

B. BFIC model

The BFICs feature non-idealities which are taken into account in the array model. The complex responses of sample chips were characterized with measurements in compression and in back-off, to determine the discretized gain and phase increments. These measurements were performed both on a single-chip evaluation board and through over-the-air (OTA) measurements with an integrated antenna. A subset of the OTA-measured responses for a single channel is shown in Fig. 4. In back-off operation the amplitude and phase settings are not fully isolated from each other. When the output-stage amplifier reaches compression, the amplitude variations between phase settings are reduced significantly.

The variances in complex responses between the measured samples were modeled as normal distributions in the MATLAB-model. The discretized gain and phase steps as shown in Fig. 4 were modeled as well, but steering-angle dependent load-pull effects due to coupling were not.

C. Beamforming array model

The free-space side array consists of low-gain linearly polarized antennas. In the model, the embedded element realized-gain pattern for large arrays is modeled as a cosine

\[ G(\theta, \phi) = 10 \log_{10} \left( D_e \cos \theta \left[ 1 - |\Gamma_a(\theta_0, \phi_0)^2 | \right] \right) \text{[dBi]}, \]  

where \( D_e \) can be found in (3), and \( \Gamma_a(\theta_0, \phi_0) \) denotes the scan angle-dependent active reflection coefficient which is simplified to zero in the model. For array elements where \( \Gamma_a \) remains below -10 dB throughout the scan range, which has been demonstrated at 30 GHz in [7], the additional scan loss would remain limited to 0.5 dB which matches the specification in Table I. This simplification enables the model to produce first-order performance estimates of large-scale arrays with individual element excitations in minutes, allowing a fast comparison of array design strategies.

The element excitations resulting from the space-feed and BFIC models are used to calculate the array factor and the resulting farfield pattern for any given scanning angle \((\theta_0, \phi_0)\).

D. Amplitude taper

Due to the tapered input power across the array as shown in Fig. 3, relatively little chip gain tapering is required to achieve a low SLL. This allows the majority of chips to operate at or close to their maximum gain setting, benefiting their power- and cost-efficiency. A -30 dB Taylor taper, shown in Fig. 5, was modeled to achieve the SLL

\[ P_{\text{pk-to-avg}} \]  

requirement with margin. With a \( P_{\text{fd}} \) of 33 dBm, a BFIC gain variation of up to 4.5 dB from maximum and all chips operating in back-off, the excitation depicted in Fig. 6a was achieved.

Table IIIa lists the modeled array performance for scan angles up to 60° in the H-plane, meeting all performance requirements listed in Table I. H-plane cuts of the modeled EIRP-patterns are depicted in Fig. 7a, showing the pencil beam, grating-lobe-free scanning and low SLLs. Due to the assumption of a cosine-pattern and array symmetry, scanning results in the E-plane are similar and not listed for brevity.

E. Space taper

Alternatively to amplitude tapering, space tapering can achieve SLL-reduction by reducing the total number of elements, along with the power requirement and heat generation,
TABLE III
MODELED PERFORMANCE OF AMPLITUDE- AND SPACE-TAPERED COSINE-ELEMENT ARRAYS ARRAY FOR BEAMSTEERING IN THE H-PLANE ($\phi = 0^\circ$)

<table>
<thead>
<tr>
<th>$\theta_0$, $\phi_0$</th>
<th>[0.0]</th>
<th>[45.0]</th>
<th>[60.0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIRP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HPBW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLL$_{pk}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLL$_{av}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(a) -30 dB Taylor amplitude taper $P_{fd} = 33$ dBm, $N_{ant} = 24368$ (100%)

(b) -30 dB Taylor space taper $P_{fd} = 45$ dBm, $N_{ant} = 7824$ (32.1%)

(c) -30 dB Taylor hybrid taper $P_{fd} = 33$ dBm, $N_{ant} = 19424$ (79.7%)

whilst optimizing per-chip power output and cost efficiency [16]. Although the requirement set in (2) is not met throughout the resulting sparse array, grating lobes are prevented due to the non-regular spacings and density in the linear projection of elements [16], [17]. Examples of space-tapered transmitarrays are absent in open literature, as removed elements directly reduce the aperture efficiency. In the proposed system, the active power amplification of the BFICs compensates for this.

The space tapering process is adapted from [16]. In co-centric rings, chips are removed at irregular intervals so the total excited power approximates an amplitude taper as depicted in Fig. 5. The number of remaining BFICs is rounded up for gain margin to fine-tune the taper.

Fig. 6b shows a 67.9% space-tapered array design with a –30 dB Taylor taper and 7824 remaining uniformly excited elements. In this case, $P_{fd}$ is increased to 45 dBm so each BFIC can reach the maximum output power. As listed in Table IIIb, this array sacrifices on EIRP, HPBW and SLL compared to the amplitude-tapered array, although the potential reduction in total cost, power and thermal output is significant. Only the SLL$_{av}$ barely misses the broadside requirement of –45 dB, as it is fundamentally limited by the number of remaining antennas [17]. Fig. 7b shows the array patterns scanning in the H-plane. E-plane scan-results differs with less than one dB in EIRP and SLL$_{pk}$, and were omitted for brevity.

F. Hybrid amplitude/space taper

If not all BFICs operate in compression, the natural amplitude taper resulting from the space feed can be used in conjunction with space-tapering. Fig. 6c shows the resulting hybrid-space-tapered array for a –30 dB Taylor taper and $P_{fd} = 33$ dBm. The results in Table IIIc show that this space-tapered array with 20% fewer elements matches the EIRP and HPBW of the dense array. SLL performance has worsened somewhat compared to the amplitude-taper, but still meets the requirements. The modeled array patterns are shown in Fig. 7c. A trade study indicated that all performance requirements could be met for a $P_{fd}$ of 38 dBm and a total of around 10,000 elements. 

Fig. 6: Element positions and excitation power in [dBm] corresponding to the arrays listed in Table III.

Fig. 7: Modeled H-plane EIRP cuts in [dBm] at $f_c$ for given steering angles $\theta_0$, corresponding to the arrays in Table III.
radiating elements, which is a reduction of 60% from dense array design. This would leave one dB of margin in EIRP and $N_{ant}$ to allow for graceful performance degradation as elements fail over time. Moreover, the additional EIRP-margin would allow the hybrid-taper to be fine-tuned by adjusting the channel gain settings.

On the non-scanning feed-array side, the element sparsity presents opportunities for further optimization. The available surface area near the array edges enables the design of larger, higher-gain feed-array elements there to alleviate the $P_{fd}$-requirement for array-wide compression. Alternatively, the space could be allocated to additional pre-amplifiers on the feed-array side to achieve a similar result.

IV. 64-ELEMENT DEMONSTRATOR DESIGN

A small-scale technology demonstrator was designed to showcase the combination of an active beamforming array, BFICs and space feeding on a single PCB and to explore the practical design features of such a system.

The demonstrator array is non-sparse, to represent the most challenging design case for antenna coupling, thermal management, component placement and signal routing. An 8×8 array was chosen to limit the size and cost, leading to a total of 4×4 BFICs and feed-array elements. This section describes the subsystem designs, including the feed- and beamforming arrays, cooling and integration on the PCB shown in Fig. 8.

A. PCB technology & design

The layer stackup and via connections of the demonstrator PCB are depicted in Fig. 9. The substrate is Isola Astra MT77, a low-loss ceramic with a stable $\varepsilon_r = 3.0$ and $\tan \delta = 0.0017$ that has been characterized up to 100 GHz.

The outer metal layers accommodate the antenna arrays, and all surface-mount components including BFICs and connectors are placed on the top layer as shown in Fig. 8. The digital lines are routed between the dual-voltage power planes and the antenna ground planes to minimize the risk of crosstalk. The PCB stack-up was designed to maintain symmetry in each lamination step to reduce the risk of warping.

![Fig. 10: (a): Patch antenna unit cell design with BFIC alignment shown. The dimensions are given in Table IV. (b): Simulated active reflection coefficient at $f_c$ in [dB] in an infinite array for scanning within 75° from broadside.](image)

**TABLE IV

<table>
<thead>
<tr>
<th>PATCH ANTENNA DIMENSIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
</tr>
<tr>
<td>Patch width $W_p$</td>
</tr>
<tr>
<td>Patch length $L_p$</td>
</tr>
<tr>
<td>Inset width $x_{pi}$</td>
</tr>
<tr>
<td>Inset depth $h_{pi}$</td>
</tr>
<tr>
<td>Feedline width $w_{pf}d$</td>
</tr>
<tr>
<td>Feedline length $l_{pf}d$</td>
</tr>
<tr>
<td>Substrate height $h_{sub}$</td>
</tr>
</tbody>
</table>

Fig. 11: Simulated S-parameters of a patch antenna near the center of the 8×8 array. The $S_{11}$-range due to PCB etching tolerances is shown in red. The range of mutual coupling with other elements is depicted in yellow as $S_{\pm1}$.
The unit cell of the linear-polarized microstrip patch antennas for the active beamforming array is presented in Fig. 10a. Although single-layer patch antennas generally have narrow bandwidths, the specified 6% around center frequency $f_c$ is achievable with a relatively thick substrate layer [32].

The elements are placed in an alternating orientation to improve symmetry in BFIC-connections and the array radiation pattern. As a result, a phase shift of 180° is required between each row of patch antennas to account for the physical rotation.

A probe-feed design would have been preferred to an inset-fed design for fewer mode transitions in the feed network. However, such a probe position would coincide with BFIC ground pads, making a direct probe-fed design impractical. Consequently, an inset-fed design was chosen, which was connected directly to the BFIC pin on the other PCB side. The resulting dimensions of the active array elements are listed in Table IV.

Table V lists the dimensions of the open-ended waveguide and quarter-wave patch antennas. The dimensions of the waveguide and patch antennas are shown and listed in Fig. 12 and Table V, respectively [31].

<table>
<thead>
<tr>
<th>Dimension</th>
<th>[mm]</th>
<th>Dimension</th>
<th>[mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Waveguide width $W_w$</td>
<td>5.35</td>
<td>Patch width $W_{wp}$</td>
<td>3.50</td>
</tr>
<tr>
<td>Waveguide height $H_w$</td>
<td>1.90</td>
<td>Patch length $L_{wp}$</td>
<td>1.13</td>
</tr>
<tr>
<td>Waveguide length $L_w$</td>
<td>10.0</td>
<td>Inset width $x_{wp}$</td>
<td>0.55</td>
</tr>
<tr>
<td>Corner radius $r_w$</td>
<td>0.50</td>
<td>Inset depth $y_{wp}$</td>
<td>0.35</td>
</tr>
<tr>
<td>Aperture width $H_{wa}$</td>
<td>2.00</td>
<td>Feedline width $w_{fd}$</td>
<td>0.30</td>
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<tr>
<td>Aperture height $H_{wa}$</td>
<td>2.00</td>
<td>Feedline length $l_{wd}$</td>
<td>2.62</td>
</tr>
<tr>
<td>Channel diameter $d_{cc}$</td>
<td>2.00</td>
<td>Feedline gap $g_{wd}$</td>
<td>0.10</td>
</tr>
</tbody>
</table>

C. Demonstrator feed array

OEWG elements were chosen for the 4×4 feed array as they can be implemented closely alongside cooling channels in a single machined metal block. The design and dimensions are shown and listed in Fig. 12 and Table V, respectively [31].

An inset-fed quarter-wavelength patch antenna, also depicted in Fig. 12, provides the microstrip to waveguide transition. The launchers are connected to the BFICs pads through microstrip lines passing through 1×1 mm² apertures. The substrate thickness of 762 µm was set to ensure symmetry in the PCB stack-up, and helped achieve a wide resonance bandwidth in this antenna design as well. Whilst OEWG apertures are typically badly matched to free space, the short length $L_w$ of 10 mm allows the planar structure to help compensate for the aperture mismatch.

The simulated S-parameters of an OEWG-element are shown in Fig. 13. The design has been validated for robustness against PCB etching tolerances and misalignments of up to ±45°, which can also be recognised from Fig. 10b. Although considered acceptable for the small-scale design to demonstrate the system operating principle, the bandwidth margin and scan range should be improved to meet the full-scale system requirements. The wide-band and wide-scanning elements presented in [7] are considered a promising starting point for a next design iteration.
In/output fittings
Horn alignment slot
Mounting holes
Cooling channels
OEWGs
BFIC Inserts
Cooling channel
Plugs

D. Integrated cooling system

Although the total dissipated power of the 16-chip array is only in the order of tens of watts, heat removal through another means besides the PCB copper would improve BFIC performance and lifetime. Liquid-cooling was chosen for the high achievable thermal performance and scaleability: a design for a large Ka-band antenna array was presented earlier in [33]. Moreover, a low-profile heatsink with liquid channels is less bulky and more feasible to integrate with a sparse antenna array than an air-cooled alternative as used in [34].

For the demonstrator, liquid-cooling channels and inserts for the BFICs were machined in a brass block alongside the 4×4 feed array of OEWG radiators as depicted in Fig. 14, resulting in a highly-integrated co-design with thermal and mm-wave functions. A good thermal connection with the heatsink is ensured through TGA-A1660 soft thermal pads from T-Global.

V. Demonstrator Measurements

As the subsystems of the realized demonstrator are highly integrated, OTA measurement setups based on [35] were used to verify their performance. The methods, results and deductions from each setup are presented in this section.

A. Calibration

The space-feed results in an unequal distribution of power amongst the BFIC. Although this distribution can be modeled as discussed in Section II.C, real-world phenomena such as imperfect feed alignment and manufacturing tolerances result in the need for calibration in order to optimize performance.

The BFICs performance should be known to accurately take quantization effects, non-linearities and production tolerances into account. A typical normalized amplitude and phase response of a single channel in Tx mode, determined using OTA measurements, was already depicted in Fig. 4.

Fig. 15 shows the demonstrator positioned before a near-field OEWG probe in the anechoic measurement chamber at Eindhoven University of Technology (TU/e) [36]. A 25 dBi gain horn was used as feed. The probe is moved with a planar scanner to face each element at a distance of just under 5 wavelengths. The gain and phase settings of the corresponding BFIC channel are swept and measured whilst all other channels are active and at zero gain settings.

Measuring all 256² combinations of gain and phase settings, in two modes (Tx & Rx) for 64 channels per array at various frequency points would take an impractical amount of time. Instead, a subset of 17 gain and 32 phase settings has been measured and spline-interpolated to create a normalized table of all possible element settings. Assuming low variations between BFICs, a practical calibration of a full-scale array could be achieved with only a single amplitude and phase reference measurement for each element.

Note that when array elements start to reach compression, phase errors start to occur with respect to the back-off calibration which lead to beam deformation, EIRP decrease and SLL deterioration. As a result, re-calibration would be required for optimal performance at various levels of compression.
B. Radiation patterns

The patch antenna embedded element patterns (EEPs) shown in Fig. 16 were determined using a planar near-field scanner from NSI-MI Technologies, using the setup illustrated in Fig. 17a. All EEPs have been simulated in a finite-array, and depicted alongside the measurements of two corner and two center elements resulting from a near-field scan. A considerable amount of ripple is observed in the patterns, the cause of which was determined to be scattering at the PCB edge based on experimental simulations. This effect will be diminished in a sufficiently large-scale array. The near-field scans are truncated at ±60°, leading to a decrease in accuracy and overlap with simulations beyond that angular range.

The farfield patterns of the full 8×8 array have also been determined with the near-field scan setup depicted in Fig. 17a, with the scan range expanded to ±75° to account for steering. The array scans well without any nulls or grating lobes up to ±45° and ±60° in the E- and H-planes respectively: Fig. 18 depicts planar cuts for steering with saturated and tapered excitations in Tx, and uniform gains in Rx. The array approximates scan-loss patterns of \( \cos(\theta) \) and \( \cos(\theta) \) in the E- and H-planes, respectively. At peak broadside EIRP, the SLL is 13.3 dB and the HPBW is 12°.

For the measurements in saturation, a \( P_{fd} \) of 22 dBm was provided through a driver-amplifier to reach each output power compression with each BFIC channel at \( f_c \). In this case, only the element phases were calibrated as shown in Fig. 4.
Fig. 20: Measured demonstrator-array farfields normalized to peak broadside EIRP, for (a) broadside and (b-d) scanning.

The results depicted in Figs. 18-20 are achieved with calibrations at 35 GHz. Fig. 19 shows the pointing error due to frequency squinting, which is limited to ±2° and ±3° when scanning to 45° in the H- and E-planes, respectively. As expected from the EEPs, H-plane scanning results in a significantly higher cross-polarization (X-pol) than E-plane, albeit still around 30 dB below the co-polarization (Co-pol). Fig. 20 shows the normalized patterns for broadside and beam-scanning with all BFICs in compression.

C. EIRP and gain measurement

The method to determine the EIRP in Tx has been adapted from [35]. After calibration, the transmitarray is placed in the farfield of a reference 20 dBi gain horn characterized in [35], as shown in Fig. 17b. Using a power meter, the received power at the reference 20 dBi gain horn was measured from a distance of 1.10 m to ensure farfield conditions. As the only unknown, the EIRP was determined from the Friis transmission equation. This process was repeated for three different calibration points, at 34, 35 and 36 GHz, and the results are shown in Fig. 21. A range of ±0.5 dB was included to reflect the measurement uncertainties such as the power and distance measurement accuracies, and the reference horn gain.

The Rx-mode gain, being a combination of array gain, amplifier gain, and combiner losses, was determined similarly but with the power meter at the feed-horn port. The Rx-mode results are shown in Fig. 21 as well. In both operating modes, the results of the three calibrations are generally within 1 dB from each other. The variation with frequency of several dBs is due to the direct-mounting of the feed-horn to the array, which is not the case in the full-scale system.

D. Feed power transfer

To maximize the achievable power transfer and prevent spillover, the array was directly attached to the feed horn as shown in Fig. 15. Robust alignment is ensured with a slot in the cooling block. To reduce the apparition of standing waves in the resulting metal cavity, the surface around the OEWG-apertures is covered by MAST MR11 tuned RF-absorbers achieving a reflectivity of around –29 dB at $f_c$.

There remains an expected frequency dependence in the transmission of power from the feed horn to the feed-array elements, which was characterized using OTA-measurements as shown in Fig. 22. For each element the corresponding BFIC operates at back-off and maximum gain setting, and the variations between EEPs and BFICs are also included in the results. The observed power variations between elements range from 5 to over 25 dB, which makes achieving a reflectivity of around –29 dB at $f_c$.

The measurement setup in Fig. 17c was used to verify the power transfer with the array separated from the feed as in the full-scale system. Although in this configuration the compressed power level could not be reached with the maximum available feed power in the lab, the power transfer is significantly more predictable and the spread between elements is limited to around 5 dB. This is expected to reduce the EIRP and Rx gain variations throughout the operating band.
E. Element excitation and thermal performance

In Fig. 23, the OTA-measured individual element power and phase variations are shown for a broadside beam setting at compressed output power. The power variations result from combined variations in $\Gamma$, BFIC $P_{dB}$-level, and EEP directivity in the broadside direction due to ripples seen in Fig. 16. Moreover, since input power variations between elements can exceed 8 dB at $f_c$ as discussed in the previous section, some BFICs are pushed further towards saturation than others.

As shown in Fig. 23, the steady state temperatures read from the BFIC on-die temperature sensor did not exceed 57°C even for operation in compression, with a maximum variation of 4°C. With all chips in Tx back-off conditions, the temperature sensor readings did not exceed 50°C. This is 15°C lower than the peak temperatures of an array with $4 \times 8$ similar chips in Tx mode using forced air cooling as reported in [35], and up to 36°C and 54°C lower than the passively-cooled arrays with $4 \times 4$ similar BFICs in [34]. The observed temperature uniformity also compares well to the variations of 7°C in [35] and 15-24°C in [34]. Considering the thousands of elements used, a total power dissipation in the order of 4 and 12 kW is expected for the full-scale sparse and amplitude-tapered arrays, respectively. The excellent and uniform performance of the integrated liquid cooling solution in the demonstrator array indicates promise for scalability, especially considering that low-cost commercial components were used.

VI. CONCLUSIONS

This article has presented the system concept of an active transmittarray antenna, designed to interface with an existing Ka-band monopulse feed. Two large-aperture array design strategies have been implemented in a model: A dense array design achieved high-EIRP pencil beams with low side-lobes using amplitude tapering, whereas space-tapered designs can reach sufficient performance results as well with a significantly reduced number of radiating elements and BFICs.

Furthermore, the design of a small-scale demonstrator transmittarray has been presented, realized, and characterized through OTA measurements. The demonstrator achieves a broadside EIRP of 56 dBm and electronic scanning up to ±45° and ±60° in the E- and H-planes, respectively. The integrated liquid cooling system provides a scalable solution to keep the BFICs at a cool temperature.

As mm-wave communication and sensing applications share many challenges, mass-produced electronics that were initially designed for 5G and SATCOM applications may increasingly find their way into the radar industry. This paper has demonstrated the novel use of SiGe-based 5G-BFICs in a radar transmitarray, and such cross-pollination may eventually trickle back to expand next-generation communication networks with sensing capabilities.

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