

A wideband RF mixing-DAC achieving $\text{IMD} < -82$ dBc up to 1.9 GHz

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A highly linear wideband RF Mixing-DAC

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Abstract

This paper presents a highly linear wideband Mixing-DAC architecture. A current-steering DAC core and a mixer are co-integrated at a unit current-cell level. A 1-bit DAC output stage is cascoded by a 1-bit mixer to form the Mixing-DAC current cell. An array of such current cells and a system front-end construct the Mixing-DAC. The system front-end includes digital signal processing and data synchronization, global LO driver and sort-and-combine calibration hardware. To reach high linearity, various techniques are used: digital dither, self measurement and calibration of amplitude and timing errors, local advanced cascoding scheme, bleeding currents, segmentation and accurate scaling of the LSB binary current cells. The proposed approach is validated by a 65nm CMOS test-chip of a dual 16-bit 2GS/s 4GHz Mixing-DAC with $\text{IMD} < -82\text{dBc}$ up to 1.9GHz and output noise lower than -165dBm/Hz .

Index Terms

Mixing-DAC, current-steering DAC, RF DAC, multicarrier GSM, LTE, WCDMA, multi-standard, high linearity.

I. INTRODUCTION

Bandwidth and spectral purity are two crucial performance specifications of transmitters. High spectral purity enables complex modulation schemes and results in the maximum use of the available bandwidth (BW). Hence, increasing both transmitter spectral purity and its (clean) BW leads to high throughput and relaxed filter requirements, enabling new applications.

Traditional transmitters contain a cascaded DAC and mixer, with a I-V and V-I conversion in between. However, the V-I conversion is a major source of distortion [1], limiting the spectral purity. An alternative approach is co-integration of both functions as a single component - the RF Mixing-DAC [2]. Fig. 1 shows a standard Cartesian transmitter architecture based on

Mixing-DACs. This architecture realizes a direct step from digital to analog RF modulated signal. As a single unit, the Mixing-DAC features much more architecture choices, compared to just combining a separate DAC and mixer [3]. Potential advantages of these new architecture choices include higher linearity and larger clean bandwidth, as demonstrated in this article. For efficiently generating a large output power, typically a dedicated (non-CMOS) PA is used. The total system efficiency is therefore dominated by this PA, hence the Mixing-DAC efficiency is a secondary concern, only after spectral purity and bandwidth.

Fig. 2 shows the IMD performance data points of the current state-of-the-art DACs, mixers and Mixing-DACs for an output RF range up to 10GHz. The requirements of multicarrier GSM, WCDMA and LTE are shown in the grey areas. Note that typical transmitters operate at a certain output-power back-off, where these linearity requirements should still be satisfied. None of the published DACs, mixers, or Mixing-DACs can meet the requirements for a multi-standard transmitter covering all these standards.

The high-performance state-of-the-art DACs usually sacrifice noise performance or lose linearity at high frequencies due to dynamic errors, e.g. finite output impedance, mismatch and ISI (inter-symbol-interference). Publications [4], [5] are notable for achieving high linearity and large signal BW at baseband frequency. Thanks to its sort-and-combine calibration method, the work of [4] achieves $\text{IMD}_3 < -80\text{dBc}$ up to $f_{out}=610\text{MHz}$ while also having an excellent noise performance of -168dBm/Hz . However, the output signal still needs to be modulated with an RF carrier without losing linearity, which is a major challenge. Hence, co-integration of the mixer and DAC is an interesting solution, as demonstrated in our original publication [14].

This paper elaborates further on [14] - a 5.3GHz 16bit 1.75GSps wideband RF Mixing-DAC achieving $\text{IMD} < -82\text{dBc}$ up to 1.9GHz. The additional contributions of this paper are in the analysis of the dominant errors and the description of the resulting design choices with implementation details, extra measurement results and the demonstration of the digital dither as

a technique for further performance improvement of the Mixing-DAC.

Section II proposes a Mixing-DAC architecture and an approach for managing its complexity. Section III discusses its output stage, errors and design trade-offs. Section IV considers the whole Mixing-DAC system. Section V validates it by two types of measurements: fundamental and application-related measurements. Comparison with literature is discussed in section VI.

II. ARCHITECTURE

The proposed Mixing-DAC architecture is shown in Fig. 3. It is based on the current-steering principle, which is well established for high-linearity at high-speeds [4], [6]. As demonstrated in this paper, the current-steering architecture is advantageous for spectral purity and wide BW over the main alternatives: switched currents [15] and $\Sigma\Delta$ Digital RF modulation [8], [16]. The switched-currents approach lacks the very high spectral purity due to the disturbances associated with turning on/off big currents. The $\Sigma\Delta$ Digital RF modulation approach sacrifices signal BW for acceptable spectral purity.

The segmentation is 6 MSB unary and 10 LSB binary, based on the balance between target linearity, power consumption, chip area and matching requirements for the binary current cells [17]. A calibration engine, used as an IP block from [4], measures the amplitude and timing errors of the unary current cells and applies the sort-and-combine method. In this paper, only its effectiveness at RF frequencies is shown. For its full characterization and theoretical foundations, the reader is referred to [4], [18], [19].

The architecture has two main parts: the output stage core and the system front-end. The output stage core sets the output signal power and realizes the two co-integrated functions: D/A conversion and mixing, while the system front-end processes and conditions the necessary signals for these. The system front-end includes LO mixing-signal driver with a regulator, serial interface, digital-signal processing unit, a programmable decoder, synchronization latches and drivers (data path), and a reference generator (elevated bulk generation).

A. Output-stage core

The core of the Mixing-DAC is the output stage which dominantly determines the output signal purity, and hence has been specifically optimized for spectral purity. To achieve a high spectral purity, it is necessary that all current cells in the output stage shown in Fig. 4 are: independent and identical (in the case of the unary current cells) or ideally scaled (in the case of the binary current cells). These goals require accurate transistor level design and optimization and careful chip layout. A single current cell of this array implements a 1-bit signal processing: signal-current generation, 1-bit D/A conversion and local mixing [20]. Because of the 1-bit nature, there are no linearity concerns at the current-cell level. At the array level, the main linearity concerns are: output impedance modulation of the current cells, coupling of the output voltage to internal nodes, (amplitude and timing) mismatch between the current cells and inter-symbol-interference (ISI) within the current cells.

The function of a single current cell is as follows. M_0 generates the current for the output signal. A large transistor area guarantees amplitude matching of the current cells. Its output impedance is increased by the cascode M_1 , thereby reducing ISI and improving the matching of current cells. M_2 and M_3 are the data switches. These four transistors form the DAC core. Furthermore, M_4 - M_7 are the mixing switches, implementing a local mixer per current cells, which yields higher linearity than global mixing, as argued in [20]. M_8 and M_9 are local thick oxide transistor cascodes per current cell, which are needed to shield the output stage core from the large output signal. The transistors M_{8m} and M_{9m} are measurement probes, which are used instead of M_8 and M_9 for calibration measurements. Bleeding currents $I_{bleed,mix}$ and $I_{bleed,oc}$ are used to limit the voltage swing on the nodes mix,cs and $OutCasc,s$, and increase the high frequency output impedance of a current cell [21]. Besides the explicit cascodes M_1, M_8 - M_9 , the switches M_2 - M_7 also act as cascodes. This multi-level cascoding strategy ensures that each function of the current cell is isolated from the other functions. The local biasing of the current-

source cascode and output cascodes is implemented to avoid crosstalk between the current cells. The fully-differential structure is chosen because of its isolation to common-mode disturbances.

The output stage needs to stack 4 thin-oxide transistors which is a design challenge in modern low-voltage CMOS technologies. Typically high W/L ratios are required, which increases the parasitic capacitances and hampers the matching and noise of the current source. Both effects lead to a decrease in linearity. In the presented architecture, a triple-well technology is used to define two voltage domains for the thin-oxide transistors: grounded-bulk transistors and elevated-bulk transistors. The DAC core (M_0 - M_3) and its associated bleeding current transistors operate within the grounded-bulk domain, where the voltages do not exceed 1.2V. The local mixer transistors and $M_{4a,d}$ utilize the elevated-bulk domain. Its voltage range is between 0.6V and V_{loHigh} (about 1.8V). These transistors are implemented in a p-well, which is biased with V_{b1} (about 0.6V). This p-well also accommodates the thick oxide transistors M_8 - M_9 and M_{8m} - M_{9m} .

B. System front-end

The system front-end provides conditioned signals for the proper operation of the output-stage core. The required functions are: digital data processing, synchronization and driving the Data switches, and distribution and conditioning of the LO signal. A programmable decoder converts the 6 MSB into 63 unary bits, the digital bits are synchronized by CML latches to minimize their timing errors, and CML drivers condition the signal levels and transition slopes for fast D/A switching with minimal glitches in the $Data,cs$ node, see [19].

A global, single driver for the LO signal is used to minimize the timing errors between the local mixers of the current cells. An internal regulator provides the LO -driver power supply from the 3.3V power supply.

C. Design approach

The next part of this paper describes the design optimization process. The design approach considers all errors, isolates and analyzes their influence, and finds optimal design solutions.

The various elements of the output stage (output cascode, mixer, data switches, current source) are separately optimized by isolating their error sources from the rest of the output stage. The scaling of the binary current cells is done at the end.

Ultimately, the remaining errors that determine the output spectral purity are finite output impedance, coupling of the output voltage to internal nodes and matching of the current cells.

III. OUTPUT-STAGE CORE

The numbered error sources of this section are annotated on the output-stage schematic of Fig. 4. The floorplan of the output stage consists of an array of parallel slices. The floorplan of one slice, which is the implementation of one current cell, is shown in Fig. 5. The binary cells are positioned at the center of the current-cell array, while the unary current cells are positioned on either side of the array, to be insensitive to linear gradients.

A. Output cascode

The output cascodes (M_8, M_9 in Fig. 4) isolate the sensitive internal nodes of the output stage from the large output voltage swing. At the output cascode, three error-sources introduce non-linear distortion:

- 1) non-linear drain impedance,
- 2) data-dependent switching of the output impedance,
- 3) ISI due to incomplete settling of the source node.

Error source 1, the non-linear drain-impedance, mainly comes from the gate-source and gate-drain capacitance (C_{gs} and C_{gd}), which both originate from the transistor channel. The magnitude of this non-linear distortion depends on the size of the capacitances and on the non-linearity of the capacitance.

The size of these capacitances is minimized by reducing the area of the transistor, while respecting the required mixer operating voltage. However, reducing the length of the output

cascode (L_{oc}) increases the non-linearity of the C_{gs} and C_{gd} capacitance values. Hence, there is a trade-off between capacitance value and capacitance non-linearity.

The non-linearity of C_{gs} and C_{gd} also depends on the output common-mode voltage (V_{out_cm}), which is illustrated in Fig. 6. In this simulation, the non-linearity of the output cascodes are isolated (see [20]). The total non-linearity is a combination of the individual non-linearities of C_{gs} and C_{gd} . The optimum V_{out_cm} (2.8V for the example of Fig. 6) is due to partial cancellation of the non-linearity of the two capacitances.

The data-dependent switching of the output cascode impedance (error source 2) is due to the data-dependent current through the local output cascodes [22], which can be reduced by adding bleed current $I_{cascBias}$ ($=I_{bleed,mix}+I_{bleed,oc}$). However, a higher bleed current increases the size of the output cascode (for identical operating voltages) and hence increases the impact of error source 1.

The ISI of error source 3 is caused by incomplete settling of the source nodes of the output cascode ($OutCasc, s$) at *Data* transitions. Incomplete settling after *LO* signal transitions do not cause ISI since the *LO* signal switches in each current cell, and hence there is no cell-dependent behavior. The ISI can be reduced by increasing $I_{cascBias}$, which is illustrated in Fig. 7. In this simulation, the operating voltages are kept constant by changing the width of the output cascode transistors. The optimal $I_{cascBias}$ is a trade-off between ISI and error source 1, which for this design is approximately 40 μ A ($\pm 13\%$ of the signal current).

B. Mixer

Next to the error sources in the output cascode, there are three error sources in the local mixer which generate non-linear distortion:

- 4) timing mismatch between mixers,
- 5) disturbance on $V_{mix,cs}$, caused by LO transition,
- 6) ISI at the source node.

The impact of timing errors (error source 4), is extensively discussed in [17]. This Mixing-DAC architecture is more sensitive to delay timing errors than to duty-cycle timing errors. Assuming a Gaussian distribution, the required timing-error standard-deviation is $\sigma_{delay} < 36\text{fs}$ and $\sigma_{duty-cycle} < 0.85\text{ps}$. Timing errors in the mixer are mainly caused by a limited LO transition speed in combination with the mixer threshold-voltage mismatch. Note that this effect mainly causes duty-cycle timing errors, which are more favorable than delay timing errors. The transition speed can be improved by increasing the strength of the LO driver or decreasing the capacitive load of the LO driver (LO distribution tree and mixer transistors). Decreasing the mixer transistor area (and hence gate capacitance) also increases the threshold-voltage mismatch. However, the resulting timing-errors improve for decreasing mixer area, since the advantages of faster switching overcome the disadvantages of the increasing threshold-voltage mismatch. Therefore, the area of the mixer is minimized, while keeping the voltage potential at the source of the mixing transistor at acceptable levels. The length of the mixer (L_{mix}) is near minimum length. Minimizing W_{mix} is limited by the available voltage headroom and by the minimum width of the technology. For binary scaling, a mixer transistor consists of 8 unit elements. Choosing less unit elements will hamper the matching of the binary cells and degrade the SFDR.

LO signal transitions generate a disturbance at the common-source node of the mixer $V_{mix,cs}$ (error source 5). The size of this disturbance depends on the settling level of $V_{mix,cs}$, which depends on the output voltage swing due to the limited output impedance. The parasitic capacitance $C_{mix,cs}$ consumes this signal-dependent charge and hence introduces non-linear distortion. Minimizing the mixer area also reduces the impact of this error source.

Error source 6 is caused by the incomplete settling of $V_{mix,cs}$ when the $Data$ signal switches. This causes ISI, which results in non-linear distortion. Increasing $I_{bleed,mix}$ decreases the settling time and hence reduces the ISI. The required bleed current for a given target IMD depends on the input signal frequency, since a higher frequency results in the $Data$ signal switching more

frequent and thus the ISI occurring more often. This relationship is demonstrated in Fig. 8, which uses $f_{LO}=F_S=1\text{GHz}$ to isolate this specific error source. The operating voltage of the mixer transistors is kept constant by changing the width of the mixer. The chosen bleed current is $30\mu\text{A}$ ($\pm 10\%$ of the signal current), which is a trade-off between performance (ISI at mix, cs and the non-linearity due to increasing $C_{outCasc,s}$), power consumption and area.

C. Data switches and current source

The error sources which are related to the data switches and cascoded current source are identical to baseband DACs. The sizing of the Data switches and current source cascode are optimized for voltage headroom for the current source and for minimizing the parasitic capacitances $C_{mix,cs}$ and $C_{data,cs}$.

D. Local biasing and decoupling

To prevent crosstalk between the various unary current cells, local biasing and decoupling is used. The global gate-source voltage V_{bias} is distributed to generate a local bias current in each current cell. This bias current is used to locally generate V_{g2} , V_{gc} and V_{gm} , as suggested in [19].

E. Binary cells

The response of the binary current cells should be an exactly scaled version of the response of the unary cell. Three techniques are employed to achieve optimal scaling: unit-element approach; scaling of parasitic capacitances; and using replica branches.

Each transistor in the unary current cell is implemented as 2^u unit elements, where u is an integer number. This enables ideal binary scaling of the transistors. However, the performance and area of the unary current cell limit the value of u . Hence, ideal scaling is only possible for the u most-significant binary current cells. For the other binary cells the width of the transistor needs to be scaled to approach the accurate scaling.

Accurate scaling of the parasitic capacitances is necessary to achieve identical time-constants for the internal nodes of the output stage and hence identical responses. As an example, the layout strategy of the output cascode is illustrated in Fig. 9. The parasitic capacitance of $OutCas_{c,s}$ is critical, which consists of a scalable part and a fixed part. The scaling of the parasitic capacitance can be perfected by tuning the width of the $OutCas_{c,s}$ track.

The third technique is to make use of unused unit element transistors in the binary current cells by constructing replica branches, which is illustrated in Fig. 10. The first advantage is that the capacitive load of the Data driver and the LO distribution tree are identical for both unary and binary current cells, which aids the generation of identical LO and $Data$ transitions. The second advantage is that the parasitic capacitances between corresponding nodes of the replica branch and main branch are not relevant, since the replica branch has the same response as the output branch.

F. LO and output signals

For high spectral purity, the delay timing errors between current cells should be minimized, as discussed in section III-B. Hence, balanced tree structures are used to implement the distribution of the LO signal and recombination of the output signal. The tree structure is based on a binary tree. An exemplary tree is shown in inset of Fig. 11, which uses two metal layers and is connected to eight current cells using a tree with three levels.

The actual trees use 7 levels, distributed over 4 metal layers. The connections between the 7 levels are optimized to equalize the delay. The simulated delay difference of both the LO and the output tree are shown in Fig. 11, based on a RC-extraction of the trees and the surrounding structures. The x-axis is the spatial position of the current cell in the array of current cells. The y-axis is the delay error with respect to the average delay. The delay of the unary current cells is more important than that of the binary current cells. The standard deviation of the unary delay errors is 1.8fs for the LO tree and 7.2fs for the output tree, which are both better than the

required 36fs of section III-B.

IV. SYSTEM FRONT-END

The system front-end generates the control signals of the output stage. Two essential elements are the LO driver and the data path.

A. LO driver

The LO driver is implemented as a single global LO driver to prevent timing errors in the mixing function of the output stage. Hence, the LO driver drives the large parasitic capacitance of the LO tree and mixer transistors, with non-standard signal levels between 1.0V and 1.8V. Furthermore, any noise or distortion on the LO signal degrades the output spectral-purity, hence the LO signal is required to be clean. The LO drive-chain of Fig. 12 addresses those requirements. It consists of two cascaded CML drivers, a regulator for the local supply voltage and a reference voltage generator.

Both the main LO driver and the pre-driver are implemented using a CML buffer to prevent signal-dependency in the supply current, and enable control over the signal swing and cross-over point. To enable a voltage swing of 800mV and fast switching, the load resistor $R_{Lm}=20\Omega$ and the tail current through M_{m0} is 40mA. The pre-driver only requires $I_{tail}=10mA$ and $R_{Lp}=80\Omega$ for fast operation. The input of the pre-driver contains a 100Ω differential resistor for transmission-line termination.

Disturbances at the supply of the LO drivers (V_{loHigh}) mainly couple to the Mixing-DAC output through two coupling paths. Low-frequency disturbances first mix with LO frequency, appear at the LO signal and then mix with the input signal and appear at $f=f_{in}+f_{LO}+f_{dist}$. High-frequency disturbances directly couple to the output. Simulations show that the disturbance at V_{loHigh} should be $<10mV$ to maintain an SFDR $>80dBc$ at the Mixing-DAC output. This is guaranteed by the CMRR of the internal regulator. The reference V_{ref} is generated in such a

way as to guarantee that the voltage at the drain of the data switches never exceeds the maximum 1.2V.

B. Data path

The data path consist of a serial interface, digital front-end, a programmable decoder, latches and drivers. The digital front-end is capable of executing signal-processing operations, e.g.: upsampling, filtering and mixing with a sine-wave. These operations can be applied in the complex signal domain and hence the two Mixing-DAC cores can operate in I/Q configuration.

For the data latches and drivers, CML logic is used. This prevents data-dependent current drawn from the power supply and enables control of the crossover point of the *Data* signal.

V. MEASUREMENTS

The proposed architecture is fabricated in a 65nm CMOS process. A photo of the fabricated test-chip is shown in Fig. 13. The size of a single Mixing-DAC core is about 1.6mm².

Fig. 14 shows a block diagram of the measurement setup. The DAC clock *Clk* and the *LO* signals are off-chip synchronized. To achieve the target linearity, the required accuracy of the LO-Clk phase synchronization is measured to be 20°. The nominal full-scale output current is 20mA which is terminated with 50Ω (double terminated). The output current can be tuned up to 50mA. The nominal output power of a single-tone signal in the high Nyquist band at $f_{LO}+f_{in}=1.9\text{GHz}$ is -8.0dBm. Due to losses in the measurement setup, the signal power at the spectrum analyzer is -14.9dBm. In the remaining part of this paper, the measurement results are not corrected for this loss.

The test-chip is characterized with two types of measurements: fundamental and application-related.

A. Fundamental characterization

The annotated output spectrum of the Mixing-DAC is shown in Fig. 15. For this measurement, the LO frequency $f_{LO}=3.0\text{GHz}$, the DAC sampling rate is $F_S=1.5\text{GSps}$, and the input signal

frequency is $f_{in}=155\text{MHz}$. Image bands are created at multiples of both F_S and f_{LO} . The signal power is highest for the 1st Nyquist bands around the carrier, i.e. from 2.25GHz to 3.0GHz and from 3.0GHz to 3.75GHz. One of these two bands is used as the output signal band, while the remaining signal images and spurs can be attenuated by filters.

Fig. 16 shows the full Nyquist band for $f_{LO}=F_S=1.75\text{GHz}$ with $f_{in}=155\text{MHz}$. The even order harmonic distortion components HD2 and HD4 are dominant and limit the SFDR to 66dBc. These are due to small unavoidable unbalances in the output network.

Since transmit filters in a typical transmitter attenuate signals outside a certain bandwidth, the SFDR in a reduced bandwidth (RB) is important. Fig. 17 shows the spectrum for a RB of 300MHz from 1.755GHz to 2.055GHz with $f_{LO}=1.75\text{GHz}$ and $f_{out}=1.905\text{GHz}$. The HD2 is external to this bandwidth, hence the $\text{SFDR}_{\text{RB}} < 75\text{dBc}$ is better than the SFDR in the full Nyquist band. Coupling of the Mixing-DAC core to the digital signal processing supply, which contains spurs at $n \cdot F_S/8$, causes the highest spur in the RB at $f_{LO} + F_S/8 - f_{in}$. Omitting the spurs due to the digital signal processing, the SFDR_{RB} would be 80dBc.

The intermodulation products, e.g. IMD3, are inside the reduced signal BW and hence cannot be filtered out. Fig. 18 shows the output spectrum for a two-tone test around 1.9GHz with $f_{LO}=F_S=1.75\text{GHz}$, where the measured IMD is -84dBc, limited by IMD5. The IMD is caused by mixer timing-errors between the current cells.

Fig. 19 shows an f_{in} sweep when $f_{LO}=F_S=1.5\text{GHz}$ for the two primary Nyquist bands. $\text{IMD3} < -80\text{dBc}$ is maintained in a 200MHz BW for the higher Nyquist band and in a 300 MHz BW for the lower Nyquist band.

Fig. 20 shows the signal frequency range, from 1 to 5.5GHz. For optimal performance, it is divided into three zones, depending on what the ratio between f_{LO} and F_S is. The spectral purity of the reduced BW of 300MHz remains high in the whole range. For a single tone, $\text{SFDR}_{\text{RB}} > 68\text{dBc}$ up to 5.5GHz. For two tone test, $\text{IMD3} < -80\text{dBc}$ up to 2GHz and $\text{IMD3} < -70\text{dBc}$

up to 3.3GHz. For completeness, the SFDR for the whole Nyquist band is also given. SFDR > 60dBc is maintained up to 4.3GHz.

Fig. 20 also shows the results of IMD measurements with dither. In these measurements, a dither signal is added to the digital baseband input signal. The dither signal consists of multiple band-limited pseudo-random signals with an individual amplitude of -50dB_{FS} and a total amplitude of -6dB_{FS} . The dither-band is far from the output signal, and hence can easily be filtered out. The IMD with dither is $< -80\text{dBc}$ up to 3.5GHz. This shows that for $f_{\text{out}} > 1.5\text{GHz}$, cell-dependent timing errors limit the traditional IMD measurements. The dither IMD above 3.5GHz is limited by coupling of the output signal to internal nodes. The thermal noise power is better than -165dBm/Hz or $-153\text{dB}_{\text{FS}}$ at 10MHz from the output frequency for $f_{\text{out}} < 1.9\text{GHz}$.

B. Application-related measurements

One of the most challenging radio standards, with respect to spectral purity, is (multicarrier) GSM. A single-carrier GSM signal is shown in Fig. 21. The GSM signal satisfies the spectral mask close to the signal frequency which demonstrates the excellent phase-noise performance. The spectral mask of -80dBc at $> 6\text{MHz}$ from the carrier is also met up to at least 20MHz from the carrier. The previous section shows that $\text{IMD}_3 < -80\text{dBc}$ up to 2GHz and $P_n = -168\text{dBm/Hz}$, which is sufficient to also satisfy the multicarrier GSM specifications.

The spectrum of a 1-channel LTE signal, with a peak-to-average ratio of 11dB, is shown in Fig. 22. The measured ACLR of -69dBc for $f_{\text{out}} = 2\text{GHz}$ is mainly limited by thermal noise of the measurement setup. The ACLR of 1-channel LTE and WCDMA for $f_{\text{out}} = 2\text{GHz}$ and 4GHz are shown in Table I, which all satisfy the LTE and WCDMA requirements.

The results of a single-tone I/Q cancellation measurement is shown in Fig. 23. Gain correction of the Mixing-DAC front-end and phase correction of the two LO signals are used to compensate for the gain and phase mismatch of the Mixing-DAC and measurement setup. This optimization is generally automatized in high performance transmitters. The image leakage is -83dBc . The

LO leakage is $-91\text{dBm}=-84\text{dBc}$.

VI. COMPARISON WITH LITERATURE

Table I compares this work with the state-of-the-art RF-DAC [5] and Mixing-DACs [7], [16], [25]. The comparison versus the state-of-the-art RF-DAC concerns two different approaches for realizing a wireless transmitter. Although RF-DACs can go up to $F_S > 10\text{GS/s}$ and hence synthesize signals up to 5GHz , their spectral purity is significantly deteriorated at high speeds. The work of [5] reports no noise measurements, IMD and SFDR only at $F_S = 3\text{GS/s}$ and up to $f_{out} = 1.4\text{GHz}$, with a deterioration rate of about 20dB/dec beyond 1GHz . In contrast, Mixing-DACs can position their signal BW around the mixing frequency f_{LO} and hence get optimal linearity in the band of interest. Finally, there is a power consumption penalty for the RF-DACs. The work of [5] consumes double the power of the presented work. The comparison versus the other published Mixing-DACs [7], [8], [16], [25] is straightforward. The presented work features the highest output frequency $f_{out} = 5.26\text{GHz}$, the largest usable reduced bandwidth (RB) of 300MHz and the lowest $\text{IMD} < -82\text{dBc}$ at 1.9GHz and $\text{IMD} < -62\text{dBc}$ at 4.1GHz . Finally, notable is the $\text{NSD} < -165\text{dBm/Hz}$ of the proposed work. Such a low noise is achieved thanks to the sort-and-combine calibration method which adds no noise, and the CML choice for the digital circuits.

VII. CONCLUSION

Co-integrating a current-steering DAC with a passive cascoded mixer can achieve high spectral purity for a wide signal band at high RF carrier. The key techniques that enable such a performance are local mixing per current cell, multilevel cascoding with double bleeding currents and elevated bulk voltage, supply-isolated LO driver, sort-and-combine calibration and digital dither. Given excellent analog design and layout, the two main linearity limitations are the mismatch between the unit cells and the coupling of the output signal to their internal nodes. This analysis is

validated by a dual 16-bit Mixing-DAC test chip in 65nm CMOS capable of output signals up to 5.3GHz. The reported measurement results, $\text{IMD} < -82\text{dBc}$, $\text{SFDR}_{\text{RB}} > 75\text{dBc}$ for $f_{\text{out}} < 1.9\text{GHz}$, and $\text{NSD} < -165\text{dBm/Hz}$, validate that the proposed architecture can simultaneously provide high linearity, low noise and large bandwidth at high RF frequencies.

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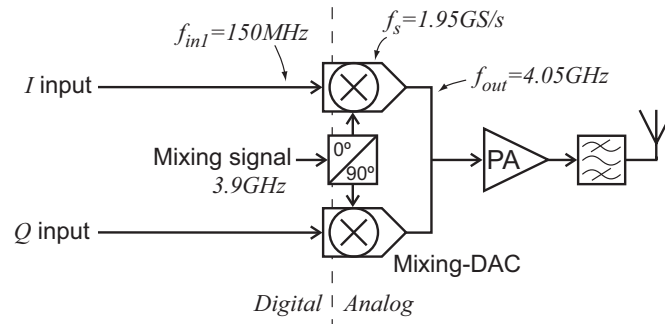


Fig. 1. Signal chain of I/Q transmitter with Mixing-DAC, with exemplary signal frequency values

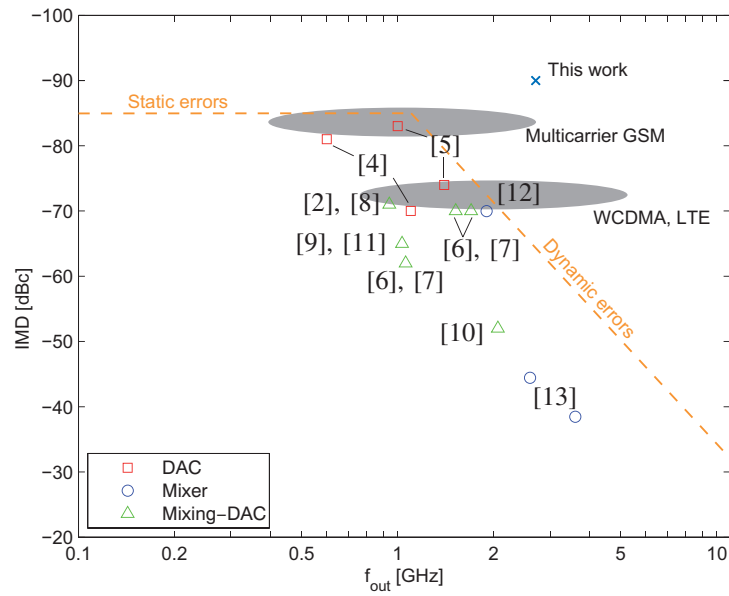


Fig. 2. Overview of the IMD of state-of-the-art Mixing-DAC, DAC and mixer publications (mixers at $1V_{pp}$ output signal amplitude)

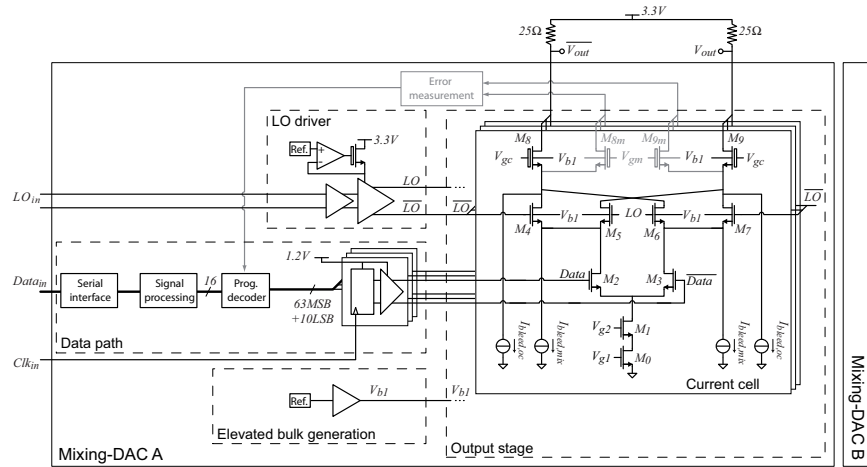


Fig. 3. Overview of Mixing-DAC system

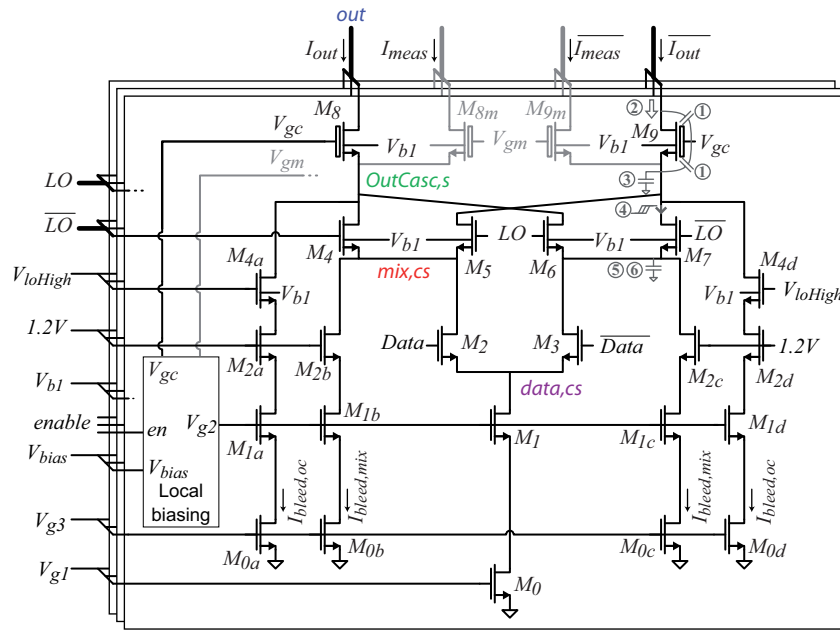


Fig. 4. Schematic of output stage

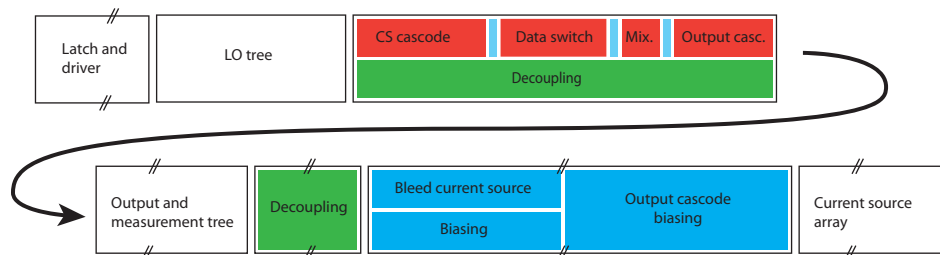


Fig. 5. Layout of one slice of the output stage, which implements one current cell

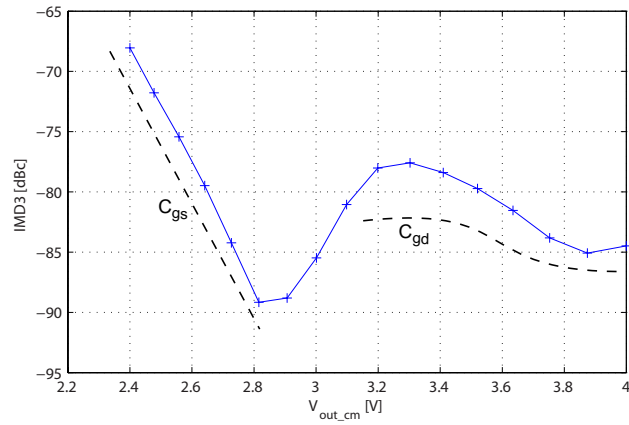


Fig. 6. Linearity dependence on the output common-mode voltage

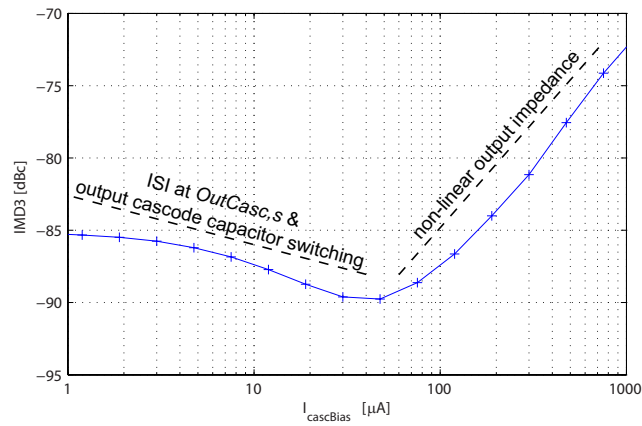


Fig. 7. Linearity dependence on the total bleed current through the output cascode

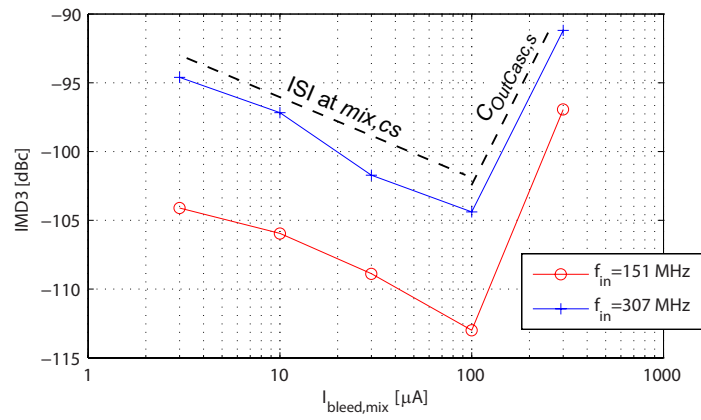


Fig. 8. IMD3 dependence on bleed current and input frequency

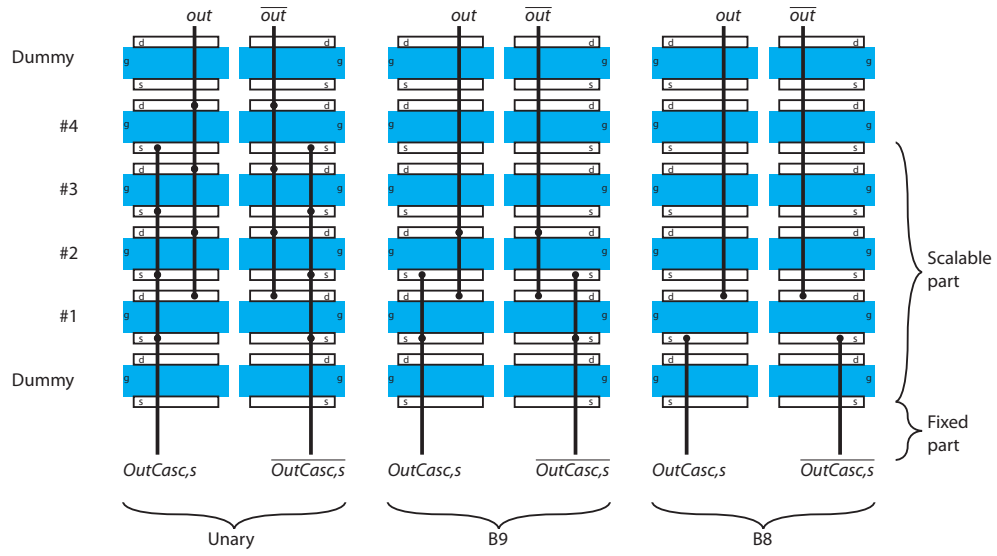


Fig. 9. Layout strategy for the output cascode

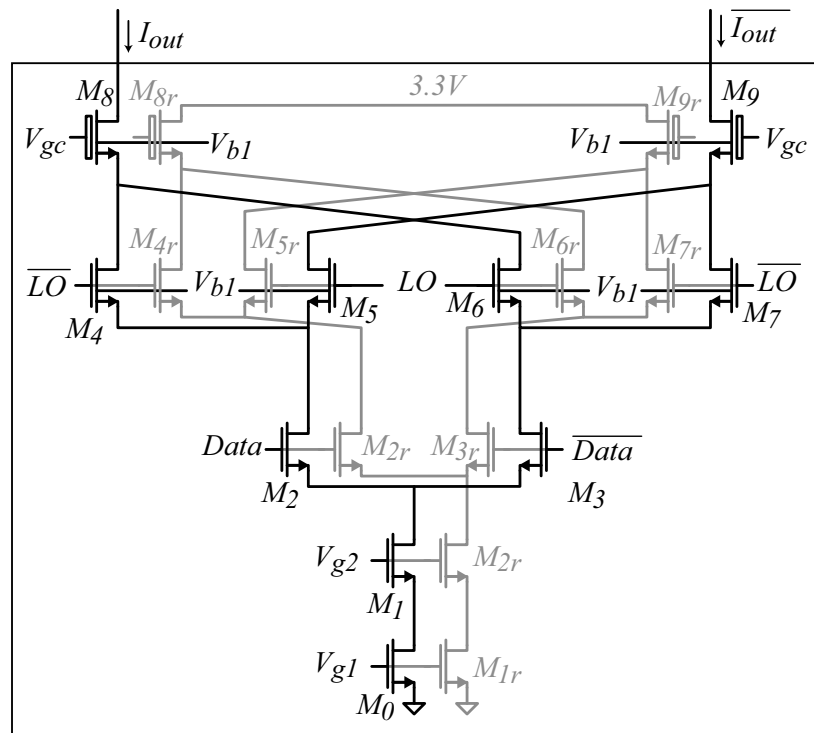


Fig. 10. Binary current cell with ultimate replica branch

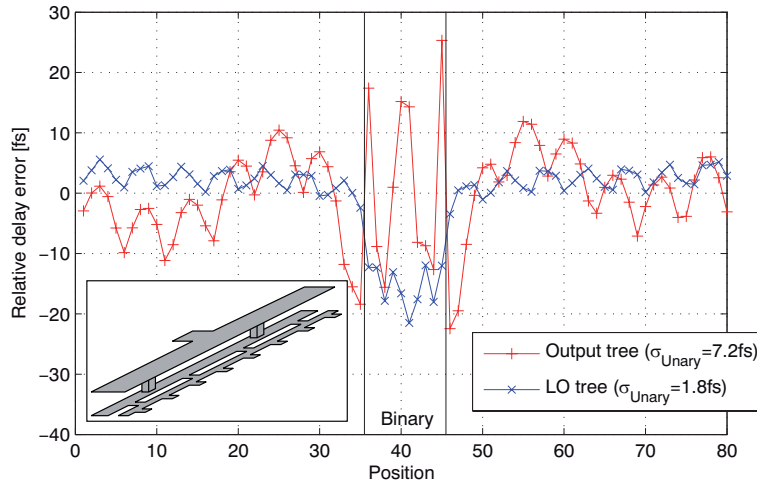


Fig. 11. Simulated delay of the RC extracted LO and output tree, with inset of exemplary tree layout

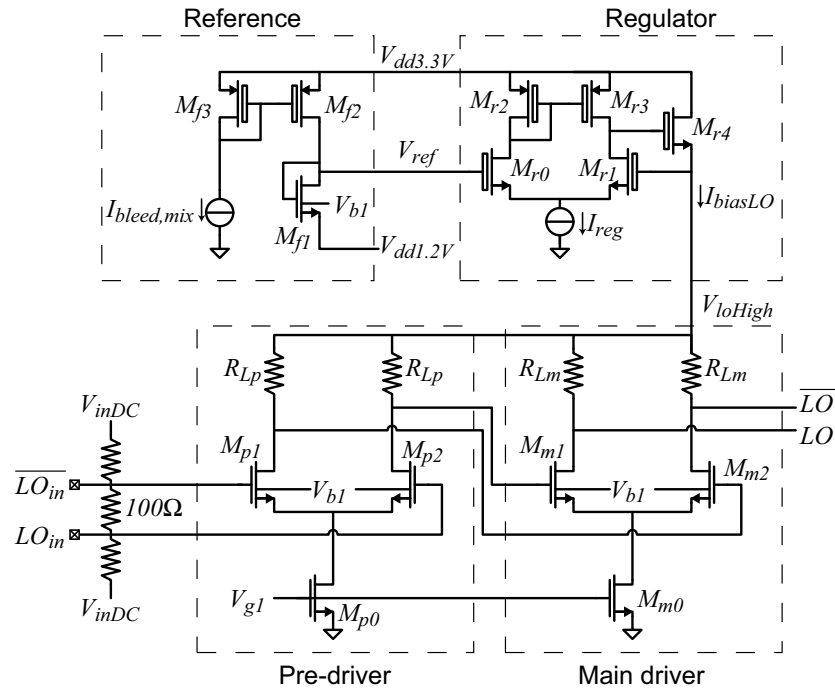


Fig. 12. Schematic LO drive chain

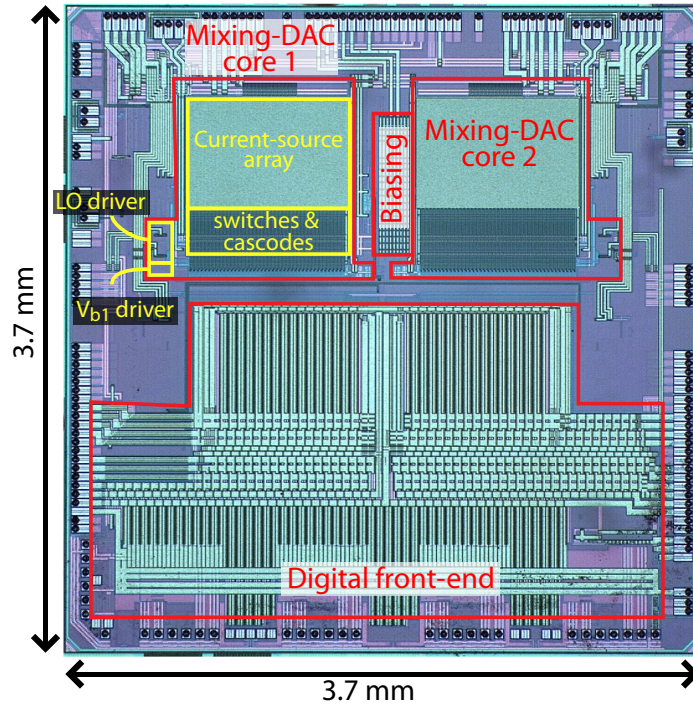


Fig. 13. Photo of the fabricated chip

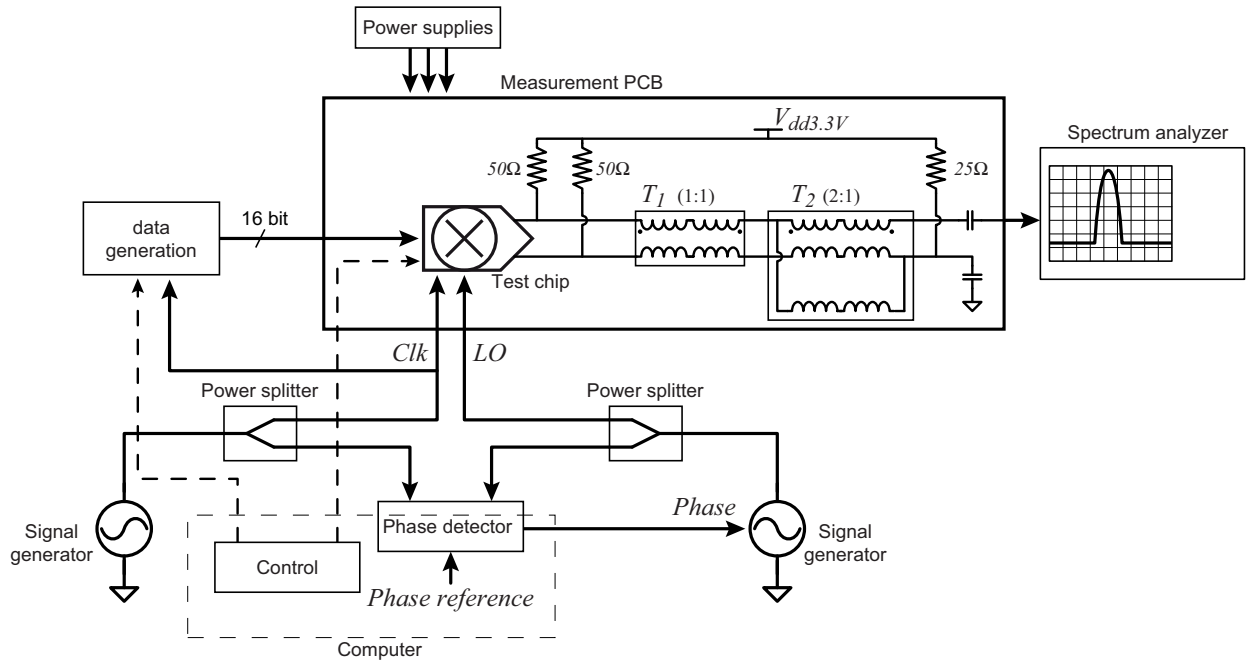


Fig. 14. Measurement setup for single-Mixing-DAC measurements

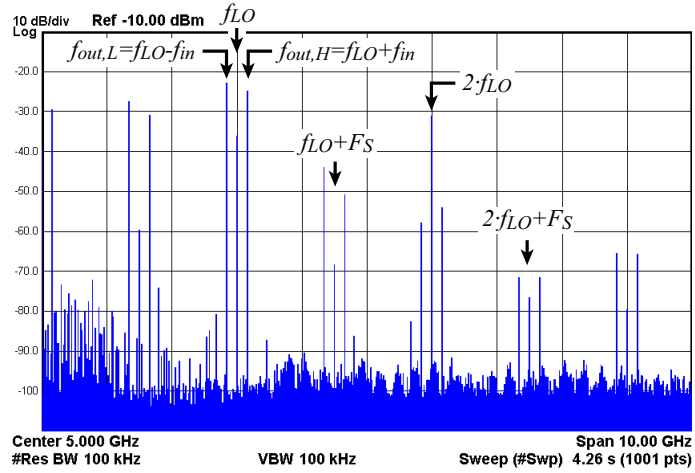


Fig. 15. Wide view of output spectrum

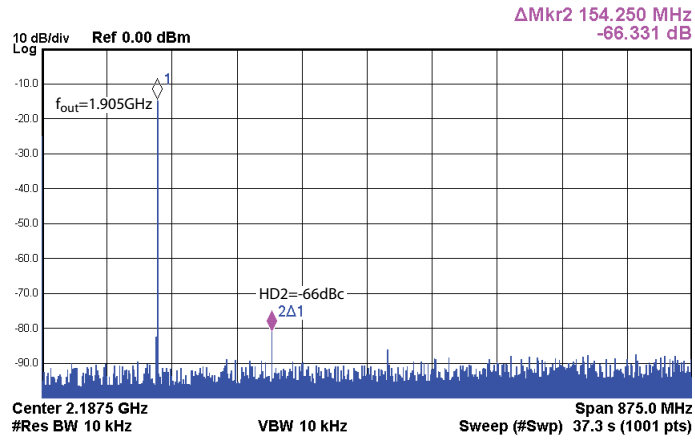


Fig. 16. Spectrum of the full Nyquist band at $f_{LO} = 1.75 \text{ GHz}$, $F_S = 1.75 \text{ GSps}$ and a single-tone signal at $f_{in} = 155 \text{ MHz}$

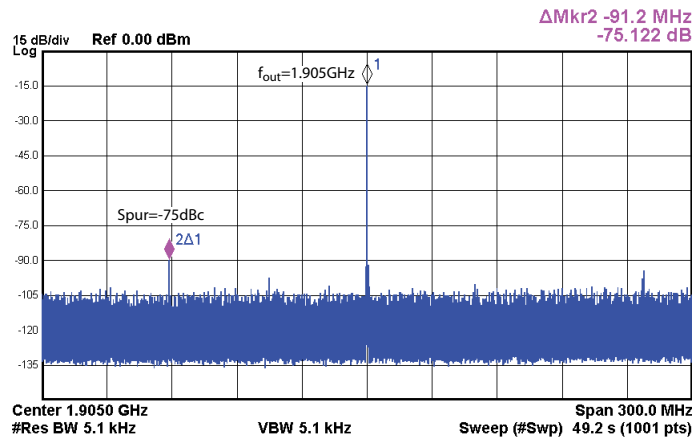


Fig. 17. Spectrum of the 300MHz RB at $f_{LO} = 1.75 \text{ GHz}$, $F_S = 1.75 \text{ GSps}$ and a single-tone signal at $f_{in} = 155 \text{ MHz}$

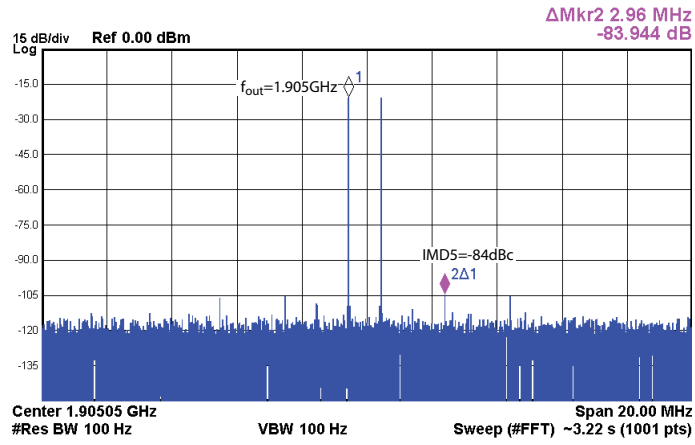


Fig. 18. Spectrum around the output signal at $f_{LO}=1.75\text{GHz}$, $F_S=1.75\text{GSps}$ and a dual-tone signal around $f_{in}=155\text{MHz}$

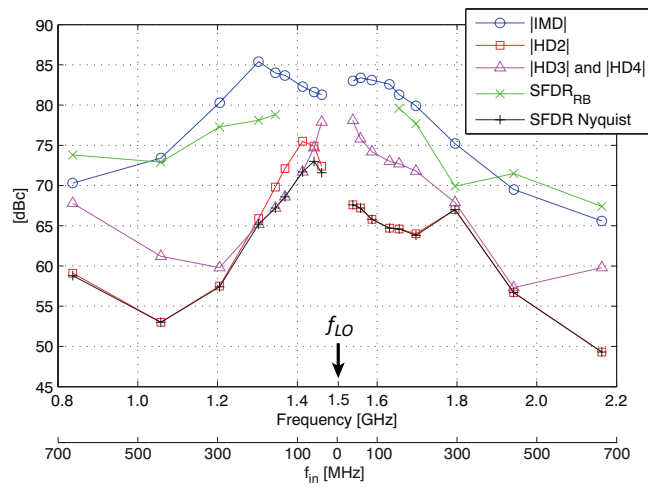


Fig. 19. Sweep over the input frequency in mix mode, $F_S=1.5\text{GSps}$, $f_{LO}=1.5\text{GHz}$

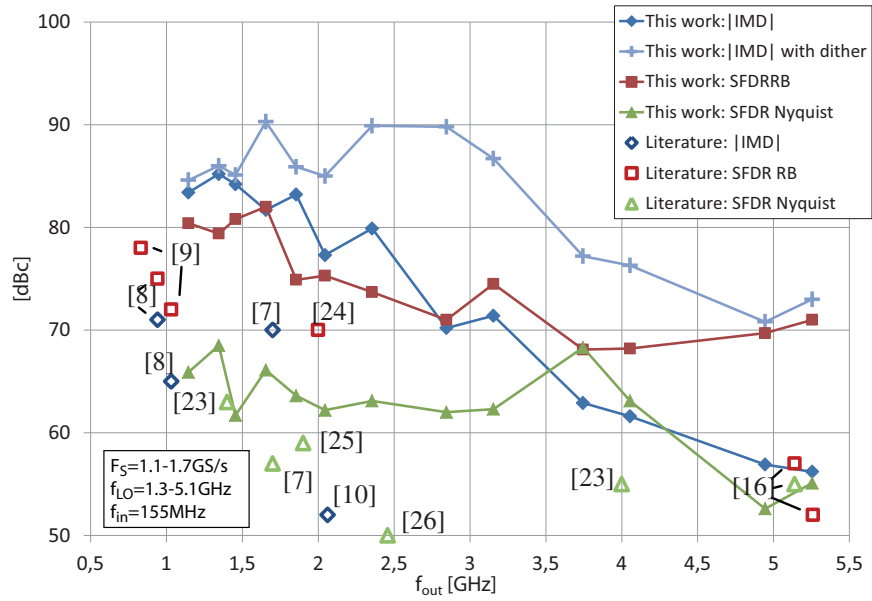


Fig. 20. Sweep over the output frequency, $F_S=1.1-1.7\text{GSps}$, $f_{LO}=1.3-5.1\text{GHz}$, $f_{in}=155\text{MHz}$. Total dither power is -6dB_{FS} .

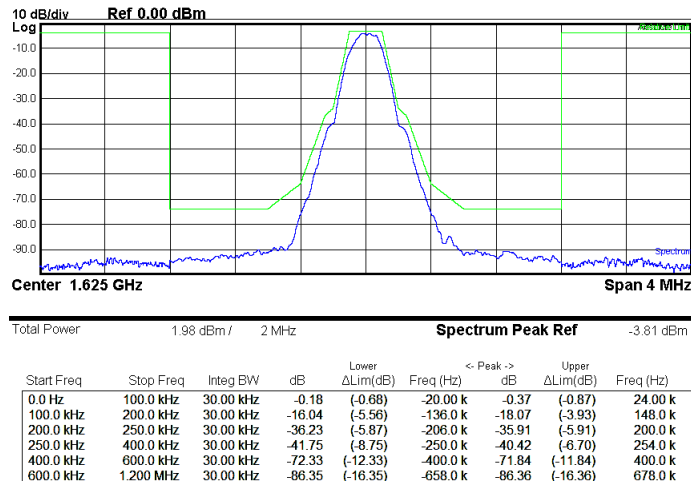


Fig. 21. GSM signal at 1.625GHz and GSM mask ($F_S=1.5\text{GSps}$, $f_{LO}=1.5\text{GHz}$, $f_{in}=125\text{MHz}$, high Nyquist band)

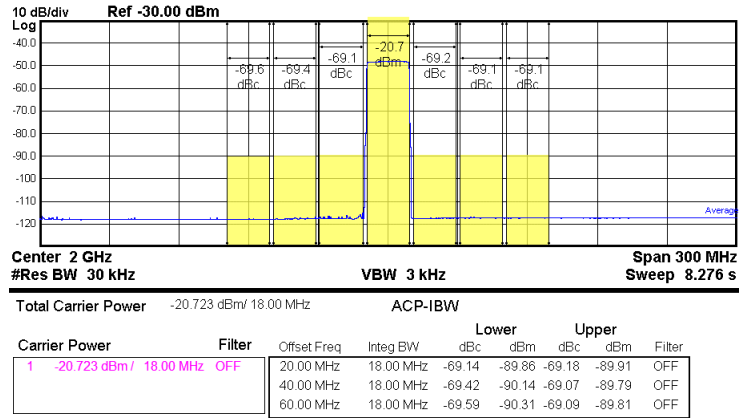


Fig. 22. Single-channel ACLR of a LTE signal at 2.0GHz ($F_S=1.75\text{GSps}$, $f_{LO}=1.75\text{GHz}$, $f_{in}=250\text{MHz}$, high Nyquist band)

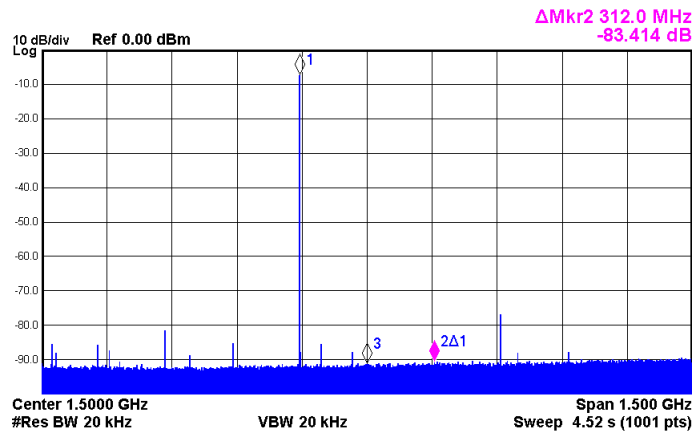


Fig. 23. I/Q configuration with gain/phase mismatch compensation and LO leakage compensation ($F_S=1.75\text{GSps}$, $f_{LO}=1.75\text{GHz}$, $f_{in}=155\text{MHz}$)

TABLE I
SUMMARY AND COMPARISON

	This work		[7]	[25]	[16]	[5]
Technology	65nm CMOS		80GHz f_T GaAs	130nm CMOS	130nm CMOS	65nm CMOS
Core area	1.6mm ²		3.2mm ²	1mm ²	0.7mm²	-
Resolution	16bit		12bit	10bit	3bit ($\Delta\Sigma$)	16bit
Max. sample rate	1.75GS/s		1.6GS/s	0.15GS/s	2.63GS/s	10GS/s
Max. effective signal bandwidth	875MHz		800MHz	75MHz	300MHz	5000MHz
Max. LO frequency	5.1GHz		1.6GHz	1.9GHz	5.25GHz	0
Max. output frequency	5.26GHz		2.4GHz	1.92GHz	5.26GHz	5.0GHz
f_{out}	≤ 1.9 GHz	4.1GHz	1.7GHz	1.92GHz	5.26GHz	1.4GHz
Core power consumption	380mW	380mW	1200mW	92mW	187mW	800mW
Output power	> -8 dBm	-8dBm	-16dBm	-2dBm*	-8dBm	-
IMD	< -82 dBc	-62dBc	-70dBc	-	-	-74dBc
SFDR Nyquist	> 62 dBc	63dBc	57dBc	50dBc	52dBc	69dBc
SFDR RB @ RB	> 75 dBc 0.3GHz	68dBc 0.3GHz	- -	- -	52dBc 0.2GHz	78dBc 1.0GHz
NSD	< -165 dBm/Hz	-167dBm/Hz	-	-146dBm/Hz	-	-
1-ch ACLR: LTE	< -69 dBc	-73dBc	-	-	-	-
1-ch ACLR: WCDMA	< -74 dBc	-77dBc	-	-58dBc	-	-

*With WCDMA signal