A 211-to-263-GHz Dual- LC -Tank-Based Broadband Power Amplifier With 14.7-dBm P SAT and 16.4-dB Peak Gain in 130-nm SiGe BiCMOS

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I. INTRODUCTION

The abundant spectrum resource above 200 GHz makes the sub-terahertz (THz) frequency range a candidate for ultra-high data rate communication such as polymer microwave fiber and short-distance high-resolution radar. The rapid development of silicon-based technology has led to impressive performance and provided a new low-cost solution to these applications. Various silicon-based radar and communication applications operating around 200 GHz have been reported recently [1]–[14]. These works put forward high demands for amplifiers, contributing to high dynamic range compression and low signal-to-noise ratio. In [1]–[3], more than 100-Gbps data rates are supported using quadrature phase shift keying (QPSK) or 16-Quadrature Amplitude Modulation (QAM) modulation and polarization diversity techniques. With the help of the chip-on-lens assembly, a 1-m distance can be achieved with over 7-dBm saturated output power at a carrier frequency of 230 GHz [1], [2]. G-band frequency-modulated continuous-wave radars are presented in [4] supporting sweep bandwidth up to 20 GHz. The peak output power is 13.8 dBm with 6.5% power-added efficiency (PAE) at 170 GHz. In those emerging sub-THz applications, the power amplifier (PA) puts forward a crucial requirement on wide bandwidth, large small-signal gain, and high output power.

Several previous studies have demonstrated amplifiers in CMOS/SiGe technologies that operate over 200 GHz [15]–[24]. In [15]–[19], the $G_{\text{max}}$ core is used to boost the power gain to maximum achievable gain. However, the $G_{\text{max}}$-based amplifiers can only operate at the target frequency with less than 10% relative bandwidth. Other techniques, such as cascode (CC) structures with a gain-boosting inductor at the upper base, are utilized to enhance gain and output power. In our previous work [20], a single-way three-stage CC amplifier achieves a maximum saturated output power ($P_{\text{SAT}}$) of 9.5 dBm at 208 GHz. At the sub-THz band, it is essential to make a tradeoff between power handling capability and small-signal gain when selecting the transistor size. Hence, an effective method to realize high output power is achieved by combining small PA cells on-chip. In [21], a 200-to-225-GHz PA with a four-way differential power combining architecture is presented, and the peak small-signal gain is 25 dB at 215 GHz with a 20-GHz 3-dB bandwidth.

A 211-to-263-GHz Dual-LC-Tank-Based Broadband Power Amplifier With 14.7-dBm $P_{\text{SAT}}$ and 16.4-dB Peak Gain in 130-nm SiGe BiCMOS

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Abstract—This article presents a broadband sub-terahertz (THz) power amplifier (PA) with a low-loss four-way power combiner. The proposed power combiner consists of an improved zero-degree combiner (ZDC) and a three-conductor Marchand balun simultaneously achieving broadband matching and power combining. The proposed three-conductor Marchand balun adopts a dual-LC tank technique by merging two resonators, and it can be equivalent to a transformer-based multi-resonating network. The power distribution is realized by one input power splitter generating two pairs of differential signals and two parallel 1-to-2 active power splitters. This hybrid distribution driving network further enhances efficiency and power gain. Based on these improvements, a high-output-power sub-THz PA with superior efficiency has been fabricated in the 130-nm SiGe bipolar complementary metal oxide silicon field effect transistor (BiCMOS) technology. The three-stage PA achieves a peak power gain of 16.4 dB, 3-dB small-signal gain bandwidth of 52 GHz from 211 to 263 GHz, a measured maximum saturated output power of 14.7 dBm at 224 GHz, and a peak power-added efficiency (PAE) of 3.13% at 220 GHz. The folded input splitter and extremely compact power combining methodology lead to a core area of 770 $\mu$m $\times$ 280 $\mu$m.

Index Terms—Broadband power amplifier (PA), dual-LC tank, power combiner, SiGe, sub-terahertz (THz), three-conductor Marchand balun.
Due to the one-way driving stage, its output power is limited to 9.6 dBm. In [22], the saturated output power of a silicon-based PA is 12 dBm at 230 GHz. The two-stage active driving distribution adopts the same transistor size as the output stage, which ensures driving ability with efficiency improved. The PA in [23] achieves the highest operational frequency and widest bandwidth compared with other works in SiGe/CMOS process operating. Also, Bücher et al. [24] presented a silicon-based work delivering 6.7-dBm saturated output power with a 17.9-dB small-signal gain near 300 GHz.

In this article, a hybrid combining architecture composed of an improved zero-degree combiner (ZDC) and a three-conductor Marchand balun is proposed, which achieves an improvement in operating bandwidth, output power, and PAE. The three-conductor balun is designed based on the dual-LC tank technique merging two resonators, equivalent to a transformer-based broadband matching network at millimeter-wave (mm-Wave) bands. Besides, an optimized two-stage four-way differential driving network is utilized in this work with small-signal gain and efficiency further improved. Furthermore, a folded input power splitter is implemented with a compact area of $106 \times 56 \, \mu m^2$ and generates two pairs of balanced signals for the driving stage. Based on this combining architecture, a compact sub-THz PA prototype is proposed to achieve high output power and wide bandwidth.

This article is organized as follows. In Section II, the architecture of the four-way PA is reviewed. The principles of the proposed power combining are described in Section III. The design details of the power combiner and high-output PA are given in Section IV. Section V presents the experimental results. Finally, a conclusion is provided in Section VI.

II. ARCHITECTURE OF THE FOUR-WAY PA

A. Four-Way PA

A high-output PA based on zero-degree power combining is designed in a 130-nm SiGe bipolar complementary metal oxide silicon field effect transistor (BiCMOS) process with $f_t/f_{max} = 350/450$ GHz. Fig. 1 shows the architecture diagram of this PA with the parameters of components. The PA is composed of a hybrid distribution driving network, a driving stage, a four-way combining power stage, and an output balun using the dual-LC tank matching technique. The proposed hybrid power distribution is realized by one input power splitter generating two pairs of differential signals and two parallel 1-to-2 active power splitters. The input power splitter is based on the modified three-conductor Marchand balun and provides two pairs of balanced signals for two differential driving amplifier (DA) paths. Each active power splitter is composed of a DA and an interstage 1-to-2 zero-degree power splitter. The second DA stage provides sufficient output power to drive the four-way combining power stage saturated.

B. Comparison of Combining Efficiency

When a single path PA cannot provide the required power, an efficient power combiner becomes essential. The power combining technique can be mainly classified into three structures: 1) Wilkinson power combining; 2) transformer-based power combining; and 3) zero-degree power combining, as shown in Fig. 2. T-line-based Wilkinson power combining achieves good isolation with a matched condition for all ports at the designed frequency [25]. However, a transmission line has a long electrical length for on-chip implementations, and its bandwidth is relatively narrow compared with the...
transformation-based network. When the operating frequency deviates away from the designed frequency or there are large parasitics, the port isolation and matching conditions will deteriorate significantly.

Traditional transformer-based combining topologies can be categorized as: 1) current combining [26]–[29] and 2) voltage combining [30], [31]. Due to inter-winding capacitance, undesired common-mode signal and noise can transfer to the single-end output [32], [33]. According to the work in [33], the common-mode conversion of the Marchand balun is much lower than that of the transformer-based balun from 200 to 300 GHz, which leads to lower insertion loss in the sub-THz band.

Zero-degree power combining has been utilized in [21] and [22], which directly combines the currents from multiple paths for large power. Typical T-junction (T-junc) combining networks show the compact size and low insertion loss at the sub-THz band. To optimize each PA channel’s output power and efficiency, an impedance transformation network is necessary. The proposed PA integrates ZDC and three-conductor-coupled output balun to realize a compact and wideband design.

C. Analysis of the Driving Topology

Two types of driving network distribution classified as passive and active have been summarized in [22]. Compared with the passive topology, the power splitters also perform interstage matching in the active topology, as shown in Fig. 3. This fact promises the active topology a higher gain and efficiency. Compared with the active distribution method, an improvement made in the proposed hybrid distribution is to replace the input balun as the current splitter, which equally splits the input power into two pairs of balanced signals.

Due to this distributed driving topology, the transistor could be sized to half compared to the active topology method, leading to a higher gain with the same total active emitter area. Furthermore, the interstage network between the second DA stage and the power stage is optimized according to the load-pull simulation. This LC network is composed of TL5 (58 Ω, 39°), TL6 (58 Ω, 20.4°), and C2 (40 fF) as shown in Fig. 1 and matches the input impedance of the power stage (17.4−j*4.7 Ω) to the optimum load impedance (20.6 + j*35 Ω) of the second DA, ensuring better output capability of the power stage.

III. BALUN-BASED DUAL-LC TANK TECHNIQUE

A. Transformer-Based Model of the Marchand Balun

As the four-way zero-degree current combining topology is used in the design, impedance transformation is a key issue in the input and output networks design. The Marchand-balun-based matching network (MBMN) is used for impedance transformation in this design due to its better common-mode suppression and lower insertion loss at the sub-THz band [33]. The planar Marchand balun consists of two coupled sections, which can be realized using microstrip coupled lines. The impedance $Z_0$ represents the characteristic impedance of the microstrip line, and $\theta$ represents the electrical lengths of the microstrip line. Propagation on these lines is partly described by the even-mode characteristic impedance, $Z_{0e}$, and the odd-mode impedance, $Z_{0o}$, with the coupling coefficient $k$ defined as

\[
k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}}, \quad Z_0 = \sqrt{Z_{0e}Z_{0o}}. \quad (1)
\]

The equivalent circuit of the co-planar coupled line can be described based on the ideal transformer [34], [35], as shown in Fig. 4. The turns ratio, $n$, and translated characteristic impedances, $Z_{01,02}$, are related to the coupling coefficient $k$ as

\[
n = \frac{1}{k} = \frac{Z_{0e} + Z_{0o}}{Z_{0e} - Z_{0o}}, \quad (2)
\]

\[
Z_{01} = \frac{Z_0}{\sqrt{1 - k^2}}, \quad Z_{02} = \frac{Z_0\sqrt{1 - k^2}}{k^2}. \quad (3)
\]

The simplified transformer-based model of a traditional Marchand balun can be obtained by cascading the two coupled-line models, as shown in Fig. 5(a). The parallel of $R_{eq}$ and $C_{eq}$ represents the differential output impedance of the previous stage. For further analysis, the equivalent circuit in Fig. 5(a)
can be redrawn, as shown in Fig. 5(b). Here, the impedance can be expressed as

\[ X_1 = -Z_{02}\cot \theta_0 \]
\[ X_2 = Z_{01}\tan \theta_0. \]  

Also, the equivalent load impedance can be expressed as

\[ R_L = \frac{n^2(n^2-1)(1 + \tan^2 \theta_0)^2}{n^2(n^2-1) + n^2\tan^2 \theta_0} \]
\[ X_L = \frac{(n^2(n^2-1)\sqrt{n^2-1}(\tan \theta_0 - \cot \theta_0) - 2n^2\sqrt{n^2-1})Z_0}{n^2(n^2-1) + n^2\tan^2 \theta_0} \]

where \( R_L \) and \( X_L \) represent the real and imaginary parts of the equivalent load \( Z_L \), respectively. For the design of Marchand balun, the electrical length of the coupled line \( \theta_0 \) is less than 90° within the operating band, and \( jX_1 \) and \( jX_2 \) can represent capacitance and inductance, respectively. In particular, the imaginary part of the equivalent load is capacitive, if \( \theta_0 \) is larger than 45° according to (7).

**B. Dual-LC Tank Matching Technique**

Although a proper impedance transformation ratio can be obtained by adjusting the coupling strength in the MBMN, the matching bandwidth is limited if the network contains only one inductor–capacitor (LC) tank. To achieve both broadband power matching and small-signal gain, a dual-LC tank matching method [38]–[40] is introduced in the output power matching. The main idea of this method is to introduce inductance (or capacitance) at the port of \( Z_L \) to form another resonant network. Because the quality factor of a lumped element is low in the sub-THz band, it is not suitable to use it directly to form a resonant network. Besides, the introduction of extra matching networks will cause the deterioration of output power and efficiency.

At the proposed MBMN, a three-conductor coupled line is used to merge the resonant network into the Marchand balun while maintaining the impedance transformation and matching function. The simplified physical model of the three-conductor Marchand balun is proposed in Fig. 6. \( Z_a, Z_b, \) and \( Z_c \) represent the characteristic impedance of each transmission line. The coupling coefficient (\( k_{ab}, k_{bc}, \) and \( k_{ac} \)) represents the coupling coefficient between adjacent coupling lines and can be adjusted by modifying the width and space (\( W_{1,2,3} \) and \( S_{1,2} \)) of the transmission lines for the desired impedance transformation ratio. The simplified equivalent circuit of the proposed three-conductor MBMN can be evolved from Fig. 5. \( T_{La} \) and \( T_{Lc} \) form a two-conductor model with \( T_{Lb} \), which is similar to the traditional coplanar Marchand balun. At the same time, \( T_{La} \) and \( T_{Lc} \) are coupled with each other. Thus, the original short stub can be replaced by a \( \pi \)-type lumped network consisting of a pair of mutual coupling inductance \( L_{ac} \) and a connecting inductance \( L_{ser}^\text{trans} \), as shown in Fig. 7, where

\[ L_\text{ac} = \frac{Z_{0c}\tan \theta_0}{2\pi}, \quad Z_{0a} = \frac{Z_a}{\sqrt{1 - k_{ab}^2}} \]
\[ L_\text{c} = \frac{Z_{0c}\tan \theta_0}{2\pi}, \quad Z_{0c} = \frac{Z_c}{\sqrt{1 - k_{bc}^2}} \]

To gain insight, lumped inductance elements are introduced to represent \( jX \). Taking \( T_{Lc} \) and \( T_{Lb} \) as a whole two-conductor coupled line, \( T_{Lb} \) can be transformed into a transmission line...
in series with an open stub, where

$$C = \frac{n^2}{2\pi f Z_{0b} \cot \theta_b}, \quad n = \frac{1}{k_b}, \quad Z_{0b} = \frac{Z_b}{k_b} \sqrt{1 - k_b^2}.$$  \hspace{1cm} (10)

Here, $k_b$ represents the coupling coefficient between TL$_b$ and the two-conductor coupled line (TL$_{ac}$), which can be extracted from the electromagnetic (EM) simulation.

The $\pi$-network consisting of $L_a$, $L_c$, and $L_{ser}$ can be related to an ideal transformer model, as shown in Fig. 8. In this equivalent model, the assignment of leakage inductance $L_{ka, kc}$ is not unique as long as the terminal behavior is the same. If all the leakage inductance is moved to the side of $L_a$ ($L_{ka} = L_a (1 - k_{ac}^2)$ and $L_{kc} = 0$), this $\pi$-network can be transformed into a T-network, where

$$L_1 = \frac{(1 - k_{ac} n_{ac}) L_a L_{ser}}{(1 - k_{ac} n_{ac}) L_a + L_{ser} + (n_{ac} - k_{ac} n_{ac}) L_a}$$ \hspace{1cm} (11)

$$L_2 = \frac{(n_{ac} - k_{ac} n_{ac}) L_a L_{ser}}{(1 - k_{ac} n_{ac}) L_a + L_{ser} + (n_{ac} - k_{ac} n_{ac}) L_a}$$ \hspace{1cm} (12)

$$L_3 = \frac{(1 - k_{ac} n_{ac}) (n_{ac} - k_{ac} n_{ac}) L_a^2}{(1 - k_{ac} n_{ac}) L_a + L_{ser} + (n_{ac} - k_{ac} n_{ac}) L_a} + k_{ac} n_{ac} L_a.$$ \hspace{1cm} (13)

Based on the analysis above, when the electrical length of the coupling line is less than 45$^\circ$, the equivalent load can be represented by a parallel connection of resistance $R_L$ and capacitance $C_L$. Thus, the simplified equivalent circuit model of the three-conductor Marchand balun is shown in Fig. 9. For further analysis, an inductive Norton transformation is performed to link the proposed circuit with a non-ideal transformer model, as shown in Fig. 10(a)–(d), and $L_P$ and $L_S$ are the self-inductance of the primary and secondary windings, respectively. It can be viewed that the first tank is formed by $C_L$ and $L_S$, and the second tank is formed by $C_{eq}/n_{ac}^2$ and $L_P$. With this method, this output matching network has the potential to achieve the broadband performance without sacrificing the PA’s small-signal gain and output power. The bandwidth of the matching network can be estimated accurately from this non-ideal transformer model with parameters ($L_P$, $L_S$, and $k_m$) in Fig. 10(d). ($L_P$, $L_S$, and $k_m$) can be given by

$$L_M = L_1 n_L + L_2 n_L^2,$$ \hspace{1cm} (14)

$$L_N = L_3 n_L,$$ \hspace{1cm} (15)

$$k_m^2 = \frac{L_N}{L_N + L_M},$$ \hspace{1cm} (16)

$$L_P = \frac{L_N}{k_m^2} = L_N + L_M,$$ \hspace{1cm} (17)

$$L_S = \frac{L_P}{k_m^2 n_L^2} = \frac{(L_N + L_M)^2}{n_L^2 L_N}.$$ \hspace{1cm} (18)

Similar to the matching network with multi-resonances used in [36] and [37], the two pole frequencies, $f_H$ and $f_L$, of the coupling network can be calculated by ($L_P$, $L_S$, $k_m$, $C_{eq}$, $n_L$, and $C_L$)

$$f_L^2 = \frac{f_{c1}^2 + f_{c2}^2 - \sqrt{(f_{c1}^2 + f_{c2}^2)^2 - 4(1 - k_m^2) f_{c1}^2 f_{c2}^2}}{2(1 - k_m^2)}$$ \hspace{1cm} (19)

$$f_H^2 = \frac{f_{c1}^2 + f_{c2}^2 + \sqrt{(f_{c1}^2 + f_{c2}^2)^2 - 4(1 - k_m^2) f_{c1}^2 f_{c2}^2}}{2(1 - k_m^2)}.$$ \hspace{1cm} (20)

The model of this non-ideal transformer can be obtained from lumped parameter values ($L_P$, $L_S$, and $k_m$) extracted from the Z- and Y-parameters of the EM simulation results. Also, this transformed non-ideal transformer model can be used as a guide to the design of the output broadband matching network based on the dual-LC tank technique.

IV. PA DESIGN WITH THE PROPOSED POWER COMBINING

A four-way zero-degree combining 211-to-263-GHz PA with the proposed dual-LC tank matching technique is designed in a 130-nm SiGe BiCMOS process with $f_T/f_{max} = 350/450$ GHz. The modified three-conductor input power splitter is used to equally split the input power and provide two pairs of balanced signals. Each DA/PA core makes use of an identical stacked HBT topology to achieve high output power. The key implementation details will be introduced in this section.

A. Amplifier Cell Design and Layout

To enhance small-signal gain and power handling capability, each DA/PA core introduces a differential CC topology. However, parasitic collector-to-base coupling capacitance at the common-emitter (CE) stage and collector-to-emitter coupling capacitance at the common-base (CB) stage from the
interconnect introduce positive feedback between the output and input of the amplifier, degrading isolation and narrowing the bandwidth, and are the potential source of instability. The layout of the DA/PA core is optimized to degrade this Miller effect, and a stair-like interconnection [33] is utilized, as shown in Fig. 11. The stair-like structure has a low series resistance ($R_s$) and a small feedback capacitance ($C_{bc}$ and $C_{ce}$) simultaneously.

Besides the transistor layout optimization, an inductive gain-boosting technique [41]–[43] is also used in the design. Introducing an inductance ($L_b$) at the base of the CB transistor can effectively improve the inherent gain, at the expense of stability. Fig. 12 shows the simulated MAG/MSG and stability factor of a differential CC cell for various values of $L_b$. It is clear that longer $L_b$ leads to higher gain but lower stability factor, and oversized $L_b$ will deteriorate the maximum gain instead. Ultimately, the optimum $L_b$ is selected to be 3 pH for a tradeoff between these two contradictory specifications. This feedback inductance can be realized as a part of the transistor connection with lower metals. In this design, it can be implemented by the metal layer M1. With the help of the 3-pH $L_b$, the gain of the differential CC pair can be improved by 2–3 dB over 220–260 GHz. In addition, a series resistor $R_b$ (1000 Ω) is inserted between the virtual ground and the bias network to improve common-mode stability.

Fig. 11. Positive feedback caused by $C_{bc}$ and $C_{ce}$ and the proposed stair-like structure of the unit CC core.

### B. Combining Network Design

The simulated power contours (with the step of 0.5 dB) of the PA core reveal that the optimum impedance is almost fixed from 220 to 260 GHz with a 3.3-V supply, as shown in Fig. 13. An optimum load impedance $Z_{opt,diff} = 16 + j*34.4$ Ω is chosen for the PA core, giving an output power
Fig. 12. Simulated (a) MAG/MSG and (b) stability of one-way PA core with different $L_b$’s.

Fig. 13. Load-pull simulation of one-way power cell.

Fig. 14. Circuit schematic of the improved four-way ZDC and its impedance transformation trajectory on the Smith chart.

Fig. 15. Simulated (a) loss and (b) common-mode suppression of the proposed four-way power combiner.

of 10.7 dBm at 240 GHz. As mentioned before, on-chip high-efficiency power combining should be exploited to enhance the maximum available output power. The proposed combining network is composed of an improved fully symmetrical wideband ZDC and a three-conductor balun based on the dual-$LC$ tank technique. Compared with traditional ZDC with dc feeding bypass capacitors (the root of bandwidth limiting), the proposed wideband ZDC contains RF ground for dc feeding releasing the bandwidth limitation, as shown in Fig. 14. Fig. 15(a) and (b) presents the simulated combining loss and common-mode suppression of the proposed wideband ZDC, respectively. The minimum combining loss of the improved 4-to-1 ZDC is 1.1 dB at 240 GHz. In the whole operating bandwidth, the common-mode suppression reaches over 30 dB.

To design the three-conductor output balun, the specific implementation needs to co-optimize with the characteristics of the four-way ZDC. Based on the model analysis in Section III-B, a systematic design methodology has been developed.

Step 1: Preliminary synthesize the four-way ZDC and estimate impedance transformation trajectory. For a given optimum load impedance $Z_{\text{opt, diff}}$, the impedance transformation trajectory of the combiner can be estimated utilizing the Smith chart. This step aims to determine the differential output impedance of the three-conductor output balun on the Smith chart.

Step 2: Pre-simulate the three-conductor Marchand balun using lumped parameters. Based on the model analyzed in Section III-B, all the lumped parameters in Fig. 7 can be related to electrical lengths, characteristic impedances, and coupling coefficients of the three coupled lines. Through the conversion from Fig. 7 to Fig. 10, a relatively simplified model can be used to reflect the matching condition. Fig. 16 shows the matching conditions by the ideal lumped components extracted from the three-conductor Marchand balun. Two bypass metal–oxide–metal (MOM) capacitors ($C_{\text{b}}$) are used to adjust the balance of the output balun. This step is to determine the size of the balun and the parameters of the three coupled lines.

Step 3: Estimate the bandwidth of the combining network. Based on the preliminarily determined parameters of the three-conductor Marchand balun, an equivalent transformer model with parameters ($L_P$, $L_S$, and $k_m$) can be obtained, as shown in Fig. 10(d). Substituting a set of parameters (i.e., 68 pH, 53 pH, and 0.92 in this design), the two pole frequencies $f_L$ and $f_H$ can be calculated as (19) and (20), respectively.

Step 4: Post-simulate with physical structure. According to parameters determined in Step 2, the physical structure of the three-conductor Marchand balun can be synthesized. To adapt to additional parasitics that the model cannot capture, the lumped parameters used in Steps 2 and 3 can be extracted from EM simulation results of the Marchand balun, as shown in Table I. Check whether its impedance...
YU et al.: 211-TO-263-GHz DUAL-LC-TANK-BASED BROADBAND PA WITH 14.7-dBm \( P_{\text{SAT}} \) AND 16.4-dB PEAK GAIN

Fig. 16. Proposed three-conductor Marchand balun and its impedance transformation trajectory on the Smith chart.

**TABLE I**

**EXTRACTED VALUES OF THE THREE-CONDUCTOR BALUN**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_a, Z_b, Z_c )</td>
<td>61 ( \Omega )</td>
<td>( k_{ab} )</td>
<td>0.56</td>
</tr>
<tr>
<td>( \theta_a )</td>
<td>70.2°</td>
<td>( k_{bc} )</td>
<td>0.6</td>
</tr>
<tr>
<td>( \theta_b )</td>
<td>75.9°</td>
<td>( k_{ac} )</td>
<td>0.11</td>
</tr>
<tr>
<td>( \theta_c )</td>
<td>81.6°</td>
<td>( k_b )</td>
<td>0.86</td>
</tr>
<tr>
<td>( L_{\text{ser}} )</td>
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Fig. 17. Layout and circuit diagram of the folded current-type 1-to-4 power splitter.

transformation trajectory matches that obtained from Step 2 by substituting the extracted lumped parameters. If the trajectory cannot match, Step 1 should be repeated to redefine the differential output impedance of the three-conductor output balun.

Fig. 18. (a) Simulated loss and characteristic of balance. (b) Simulated common-mode suppression of the proposed input power splitter.

Step 5: Post-simulate with PA cores. The final step aims to adapt to additional parasitics that the model cannot capture and adjust the overall combining network slightly.

Benefiting from the improved wideband ZDC and dual-LC tank technique, this hybrid combining topology shows advantages over transformer-based combining and zero-degree combining at the sub-THz band. First, it is difficult to implement a transformer with parameters similar to (36 pH, 48 pH, 0.92). The small inductance, high coupling factor, and accurate turn ratio are hard to achieve in the high-frequency band due to the self-resonance of coils and the common-mode
TABLE II
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART SILICON-BASED AMPLIFIERS OVER 200-GHz

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Process</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>$f_c$ (GHz)</th>
<th>$P_{\text{SAT}}$ (dBm)</th>
<th>$O_{\text{dB}}$ (dBm)</th>
<th>$\text{PAE}_{\text{max}}$ (%)</th>
<th>Gain (dB)</th>
<th>$BW_{3\text{-dB}}$ (GHz)</th>
<th>Area (mm$^2$)</th>
<th>$\text{FoM}_{A/B}$</th>
<th>Topology</th>
</tr>
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<tbody>
<tr>
<td>[17]</td>
<td>65 nm CMOS</td>
<td>300</td>
<td>248.6</td>
<td>3.8</td>
<td>2.3</td>
<td>3.2</td>
<td>12.6</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>$G_{\text{max}}$-core 3-stages CS</td>
</tr>
<tr>
<td>[19]</td>
<td>65 nm CMOS</td>
<td>395</td>
<td>242</td>
<td>-3.3</td>
<td>-5.1</td>
<td>1.6</td>
<td>13.9</td>
<td>227-257</td>
<td>0.14</td>
<td>60.3/0.10</td>
<td>Dual-peak $G_{\text{max}}$ 4-stages CS</td>
</tr>
<tr>
<td>[20]</td>
<td>130 nm BiCMOS</td>
<td>450</td>
<td>221.5</td>
<td>9.5</td>
<td>6</td>
<td>2.96</td>
<td>22.5</td>
<td>204-239</td>
<td>0.16</td>
<td>83.6/0.21</td>
<td>3-stages CC</td>
</tr>
<tr>
<td>[21]</td>
<td>130 nm BiCMOS</td>
<td>370</td>
<td>210</td>
<td>9.6</td>
<td>4</td>
<td>0.5</td>
<td>25</td>
<td>200-220</td>
<td>1.44</td>
<td>78.1/0.14</td>
<td>4-way Diff ZDC 3-stages CC</td>
</tr>
<tr>
<td>[22]</td>
<td>130 nm BiCMOS</td>
<td>450</td>
<td>227</td>
<td>12*(13.5**)</td>
<td>9*(10.5**)</td>
<td>2.14</td>
<td>12.5</td>
<td>200-255</td>
<td>0.83</td>
<td>74.9/0.16</td>
<td>4-way Diff ZDC 3-stages CC</td>
</tr>
<tr>
<td>[23]</td>
<td>130 nm BiCMOS</td>
<td>450</td>
<td>280.5</td>
<td>5</td>
<td>3.3</td>
<td>1.19</td>
<td>15</td>
<td>247-314</td>
<td>0.58</td>
<td>69.6/0.23</td>
<td>3-stages CC</td>
</tr>
<tr>
<td>[24]</td>
<td>130 nm BiCMOS</td>
<td>650</td>
<td>268.5</td>
<td>6.7</td>
<td>5.2</td>
<td>0.92</td>
<td>17.9</td>
<td>239-298</td>
<td>0.26</td>
<td>73.82/0.15</td>
<td>3-stages CC</td>
</tr>
<tr>
<td>[45]</td>
<td>32 nm SOI CMOS</td>
<td>320</td>
<td>213</td>
<td>4.6</td>
<td>2.7</td>
<td>6</td>
<td>15</td>
<td>206-220</td>
<td>—</td>
<td>73.9/0.09</td>
<td>Over-neutralization 3-stages CC</td>
</tr>
</tbody>
</table>

This work | 130 nm BiCMOS | 450 | 237 | 14.7 | 11.5 | 3.13 | 16.4 | 211-263 | 0.4 | 83.6/0.21 | 4-way Diff ZDC 3-stages CC |

* without de-embedding input/output baluns and pads ** with de-embedding input/output baluns and pads

C. Input Power Splitter Design

In the proposed PA, the DA/PA core and interstage network are fully differential. The common-mode effect starts generating from the input single-ended to two-way differential conversion network. A fully symmetrical folded current-type 1-to-4 power splitter is proposed at the input for the improvement of balance and common-mode rejection, as shown in Fig. 17. The input impedance of the first-stage DA core is about $26.5 - j*20.4 \ \Omega$. The power splitter is composed of two folded three-conductor Marchand balun providing more freedom in impedance matching design. Two MOM capacitors are introduced at the combing nodes of the two folded baluns. It brings many benefits, such as ensuring RF ground for short stubs in the two folded baluns, adjusting the balance performance, and providing a low impedance path to RF ground for the unwanted common-mode signal. According to the simulation results shown in Fig. 18, the amplitude imbalance is less than 0.2 dB, and the phase imbalance is less than 2 degrees with an insertion loss lower than 3 dB within the bandwidth of 220–260 GHz. Within the operating frequency band, the common-mode suppression is over 40 dB.

V. EXPERIMENTAL RESULTS

The micrograph of the fabricated chip in the 130-nm SiGe process is shown in Fig. 19(a). The chip occupies a
compact area of $790 \times 500 \ \mu m^2$ and the core area excluding pads is only $770 \times 280 \ \mu m^2$, which is comparable with those single-way differential works [20], [33]. The proposed amplifier consumes 285 mA from a 3.3-V supply. As shown in Fig. 19(b), the amplifier measurement is implemented by on-wafer probing.

A. Small-Signal Measurement Results
The small-signal measurement setup includes a performance network analyzer (PNA) microwave network analyzer (Agilent N5245A) and a pair of OML vector network analyzer (VNA) extender modules. The calibration is performed using the impedance standard substrate (ISS) to ensure measurement accuracy. Fig. 20 shows the simulated and measured $S$-parameters of the implemented amplifier with the supply voltage of 3.3 V. The DA/PA core is biased by a current mirror with $V_b$ of 0.93 V and $V_{cas}$ of 2.3 V. The measured $S_{11}$ and $S_{22}$ curves exhibit similar trends to their simulation counterparts, and the peak gain is approximated as well. The PA provides a measured peak gain of 16.4 dB at 257 GHz, yielding a 3-dB bandwidth from 211 to 263 GHz. The stability $k$-factor is plotted showing values above 7.8 over the whole band. Group delay, another important parameter for broadband communication applications, shows variations of only $\pm 10 \ \text{ps}$ across the whole band, as shown in Fig. 21. The measured group delay shows fluctuations with the swing of around 20 ps, which is similar to some other THz amplifiers [22], [23]. The effect of group delay should be taken into consideration when designing a high-order modulated system with very wide bandwidth. The common approach is to use carrier aggregation technology to improve the reliability of the system.

B. Large-Signal Measurement Results
The large-signal performance is characterized by two Ceyear mm-Wave source modules addressing 170–260 GHz (82401SA) and 220–325 GHz (82406D), as shown in Fig. 19(b). The output of the PA is measured using a power meter (Erikson PM4). The loss of interconnects is de-embedded through back-to-back measurement. Fig. 22 shows the measured $P_{out}$ versus input power, power gain versus input power, and PAE versus input power at 220, 240, and 260 GHz, respectively, in comparison with the simulation results. The measured power gain is similar to the small-signal measurement, yet is slightly smaller, which is caused by calibration deviations of the drive stage gain. The measured $P_{out}$ and PAE show similar trends to those of the simulation results. The delivered output power from the mm-Wave source module was not enough to drive the PA saturated. Therefore, an on-chip three-stage driver amplifier with a saturated output power higher than 3 dBm [44] was inserted before the PA as a driver for the measurement of $P_{SAT}$. The measured maximum output power and peak PAE of the amplifier are 7.8–14.7 dBm and 0.7%–3.13% over 211–261 GHz, respectively, as shown in Fig. 23. The amplifier consumes 924 mW at a supply voltage of 3.3 V.

To compare the performance of the amplifiers independent of the employed processes, the figure of merit (FoM$_A$) is defined as [46]

$$
\text{FoM}_A = G(\text{dB}) + P_{SAT}(\text{dBm}) + 10\lg(\text{PAE}(%)) + 20\lg(f_c(\text{GHz}))
$$

(21)

where $P_{SAT}$, $f_c$, and $G$ represent the maximum output power, center frequency, and the power gain of the amplifier. FoM$_A$ can indicate the overall performance of the PAs. However, this
factor is limited since it does not include circuit bandwidth and fabrication process difference, which are two of the important characteristics of an amplifier. For a more comprehensive comparison, a new figure of merit (FoM) considering operating bandwidth and fabrication process is proposed [19]

\[
\text{FoM}_B = \sqrt{G} \left( \frac{f_c}{f_{\text{max}}} \right)^2 \frac{\text{BW}_{-3\text{dB}}}{f_c}
\]

where BW_{-3dB} and N represent the 3-dB bandwidth and the stage number of gain devices, respectively. Table II shows the summary of the performance and comparison with the state-of-the-art CMOS/SiGe amplifiers operating over 200 GHz.

VI. CONCLUSION

To realize a wideband single-ended PA, this work presents a hybrid combining architecture composed of a wideband ZDC and a three-conductor Marchand balun. The dual-\text{LC} tank matching technique is introduced in the design of the output three-conductor Marchand balun. Two resonators can be merged into the output balun without extra lumped elements maintaining wideband and low loss simultaneously. This combining network has an excellent amplitude/phase balance, and the simulated minimum insertion loss of the combiner structure is 2 dB.

A high-output four-way combining sub-THz PA with superior efficiency in a 130-nm SiGe BiCMOS process was designed and characterized. The proposed PA demonstrates a peak small-signal gain of 16.4 dB with 52-GHz 3-dB bandwidth from 211 to 263 GHz. The measured maximum output power and maximum PAE_{max} of the PA over 211–261 GHz are 7.8–14.7 dBm and 0.7%–3.13%, respectively. The proposed compact ZDC and the folded input splitter lead to a small chip area of 790 \mu m \times 500 \mu m. This PA achieves a recorded P_{SAT} of 14.7 dBm FoM of 83.6 among previously sub-THz PAs.

REFERENCES


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