

A 1.2V Inductorless Receiver Front-End for Multi-Standard Wireless Applications

Citation for published version (APA):

Vidojkovic, V., Sanduleanu, M. A. T., Tang, van der, J. D., Baltus, P. G. M., & Roermund, van, A. H. M. (2008). A 1.2V Inductorless Receiver Front-End for Multi-Standard Wireless Applications. In *IEEE Radio and Wireless Symposium, 22-24 Jan. 2008* (pp. 41-44) <https://doi.org/10.1109/RWS.2008.4463423>

DOI:

[10.1109/RWS.2008.4463423](https://doi.org/10.1109/RWS.2008.4463423)

Document status and date:

Published: 01/01/2008

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

A 1.2V Inductorless Receiver Front-End for Multi-Standard Wireless Applications

¹Maja Vidojkovic, ²Vojkan Vidojkovic, ²Mihai A.T. Sanduleanu, ³Johan van der Tang, ¹Peter Baltus and ¹Arthur van Roermund

¹Eindhoven University of Technology, Eindhoven, The Netherlands, ²Philips Research, Eindhoven, The Netherlands, ³Holst Center/IMEC-NL, Eindhoven The Netherlands

Abstract — A novel, broadband, inductorless, multi-standard receiver front-end in a digital CMOS 90nm Low Power (LP) process is described. The front-end operates in the frequency range from 0.8 GHz up to 1.7 GHz. It achieves a voltage gain of 24dB and a noise figure of 5.5dB. The measured IIP3 and IIP2 of the receiver are -13dBm and +30dBm, respectively. The input return loss is better than -10dB in the frequency band from 0.8 GHz up to 1.7 GHz. The front-end consumes 26mA from 1.2V power supply and occupies a chip area of 1mm².

Index Terms — Multi-standard receiver, inductorless receiver front-end, low voltage receiver front-end, broadband receiver front-end, software-defined radio.

I. INTRODUCTION

Nowadays, the number of wireless standards is increasing rapidly. This has motivated the wireless industry to look for multiple radio devices. The integration of multiple functions on-chip enables connectivity with different systems at various locations. In order to increase hardware flexibility and functionality, RF designers are trying to design and implement cost-effective, multi-standard RF transceivers. It is a challenge to stretch the design space of an RF front-end in such a way that it satisfies simultaneously the requirements of as many standards as possible. One possibility is the use of tuned RF front-ends based on narrow band, tunable LNAs [1]. The complexity and the occupied chip area of this multi-standard RF front-end grow rapidly as the number of covered standards increases. As performance and frequency control are inter-related, the complexity in the design increases a lot. Another approach is a single broadband RF front-end that can satisfy the requirements of any standard in a wide frequency range [2]. In a combination with a tunable RF filter after the antenna, this seems as a straightforward and a cost-effective solution for a multi-standard RF front-end. This paper addresses a novel broadband inductor-less RF front-end that can operate in a frequency range from 0.8GHz up to 1.7 GHz.

Section II of this paper presents the operation of the multi-band receiver front-end, the measurement results are discussed in Section III and conclusions are given in Section IV.

II. MULTI-BAND RECEIVER FRONT-END

The broadband receiver front-end is presented in Fig. 1. The first building block in the RF front-end is an inductorless, broadband LNA. A single-ended to differential converter (SDC) plays the role of an active BALUN. It converts the single-ended signal into a differential one. I/Q harmonic reject mixers (HRI/HRQ) convert the RF signal to low or zero intermediate frequencies (IF). The output of the mixer is connected to a transimpedance amplifier configured as a low-pass filter. For measurement purposes an eight-phase LO generator provides the required LO phases to the HR mixer.

A. Broadband LNA

A simplified schematic of the inductorless broadband LNA with resistive feedback is illustrated in Fig. 2. The first stage in the feedforward path of the LNA is a common source, cascode amplifier. It consists of the common source amplifier M_{n1} , the cascode transistor M_{n2} and the load resistor R_{d1} .

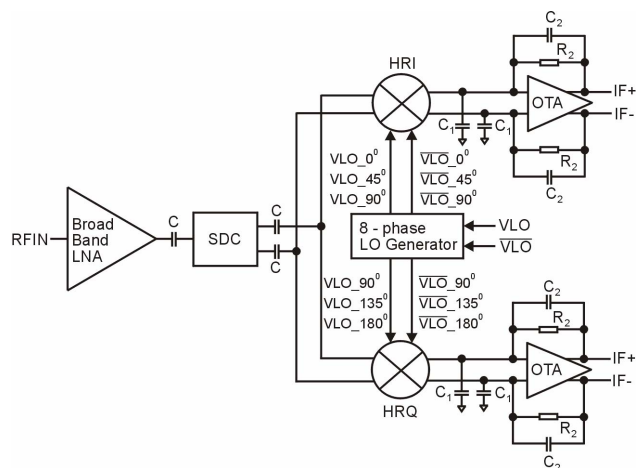


Fig. 1. Broadband receiver front-end

The cascode transistor M_{n2} increases the output impedance and the reverse isolation. At low supply voltage ($V_{DD}=1.2V$) the voltage drop across the load resistor and transistors becomes critical.

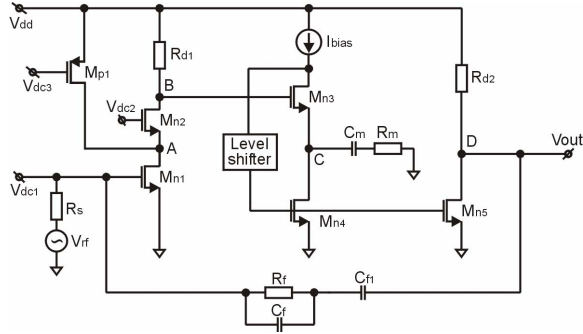


Fig. 2. Simplified circuit diagram of the broadband LNA

The PMOS transistor M_{p1} diverts a part of the DC current to V_{DD} . For that, the AC current flows through the transistor M_{n2} , as the output impedance of M_{p1} is larger relative to the input impedance of M_{n2} .

The second stage of the LNA acts as a voltage-to-current converter. The follower circuit, M_{n3} and M_{n4} , provides a voltage-to-voltage conversion. The voltage in node C (V_C) tracks the voltage in node B (V_B). The current variation of M_{n3} is sensed on the output resistance of the current source I_{bias} . A local feedback loop follows these fluctuations by modulating the current source M_{n4} . As a consequence, the voltage signal V_C is converted in a current on a series R_m , C_m combination and M_{n4} . The DC current on the resistor R_m is blocked by the capacitor C_m .

The gate voltages of M_{n4} and M_{n5} are equal. Therefore, the drain current of M_{n5} is a scaled copy of the current in M_{n4} . The ratio between the dimension of M_{n5} and M_{n4} determines the ratio between the drain currents of M_{n5} and M_{n4} . The output current is converted into a voltage on the load resistor R_{d2} . The feedback resistor R_f is DC blocked by C_{f1} , while C_f is used to control peaking at higher frequencies and improves input matching (S11).

B. Single-Ended to Differential Converter

A simplified schematic of the single-ended to differential converter (SDC) is presented in Fig. 3.

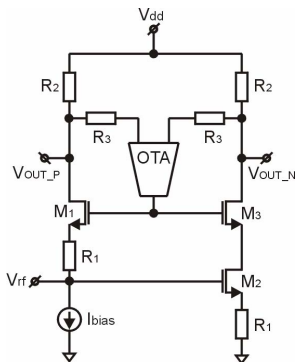


Fig. 3. Simplified schematic of the single-ended to differential converter

The SDC converts the single ended signal from the LNA into a balanced signal required by the mixer.

The RF input is AC coupled to the LNA. The OTA ensures a self-biasing mechanism of the SDC and an offset correction at the two differential outputs of the circuit. The resistors R_1 improve matching between the transistors M_1 and M_2 . The drain currents of these two transistors have the same amplitude and opposite phases. The SDC isolates the HR mixer from the LNA. Besides, it improves the overall noise figure of the RF front-end.

C. Harmonic-Rejection Passive Mixer

Fig. 4 shows the passive harmonic rejection mixer [3]. The individual mixers are AC coupled to SDC and driven with six LO phases. The voltage signal from SDC is converted in a current on the resistors R_1 and R_2 . By properly scaling the resistor values $R_2=R_1/\sqrt{2}$ and the transistors of the three switching sections i.e. $(W/L)_2=\sqrt{2}*(W/L)_1$, the third and the fifth harmonic are rejected.

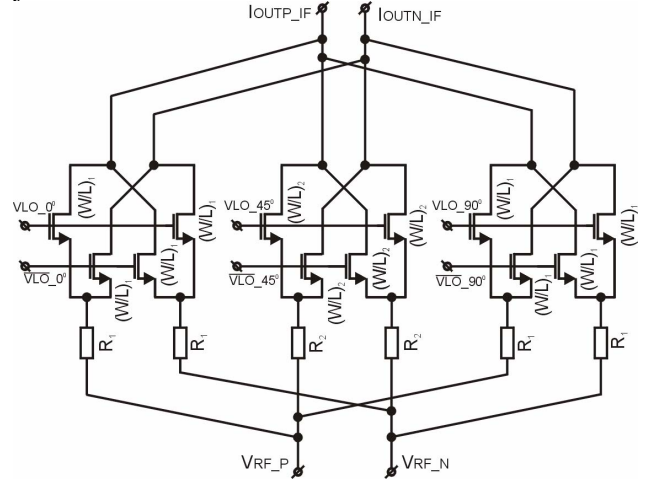


Fig. 4. Passive harmonic reject mixer

D. Transimpedance amplifier

Fig.5 shows the operational transconductance amplifier (OTA) that is used in the transimpedance amplifier (see Fig.1). The OTA is a differential version of the second and third stages in the broadband LNA (see Fig. 2).

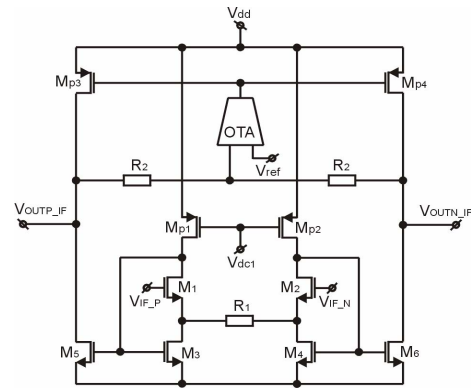


Fig. 5. Simplified schematic of the OTA

The first stage of the transimpedance amplifier provides a voltage-to-current conversion. The source follower, M_1 - M_3 (M_2 - M_4), performs the voltage-to-voltage conversion. The voltage signal at the source of M_1 (M_2) is converted into a current by the resistor R_1 and the transistor M_3 (M_4). The current of the transistor M_3 (M_4) is transferred to transistor M_5 (M_6) at the output stage of the amplifier. The output current is converted in a voltage on the output impedance of the transistor M_{p3} (M_{p4}).

E. LO Generator

For measurement purposes, the eight-phase LO generator, (see Fig.6(a)), produces the required LO phases to the HR mixer. It consists of a polyphase filter, [4], and a resistive interpolation network (see Fig.6(b)). The choice of the resistor values in the interpolation network is not arbitrary. For equal amplitudes, R_2 and R_3 are related as $R_3=2(1+\sqrt{2})R_2$. The choice of R_1 is fairly independent of R_3 and R_2 . At the output of the interpolation network, eight phases with equal amplitudes are produced. In order to drive the mixers, buffers are connected at the outputs of the interpolation network.

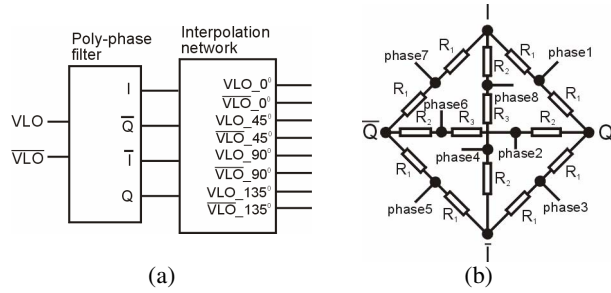


Fig. 6. (a) Eight phase LO generator, (b) Resistive interpolation network

III. MEASUREMENT RESULTS

Using the insights into the operation of the presented building blocks, the RF front-end is designed and implemented in a baseline CMOS 90nm LP process.

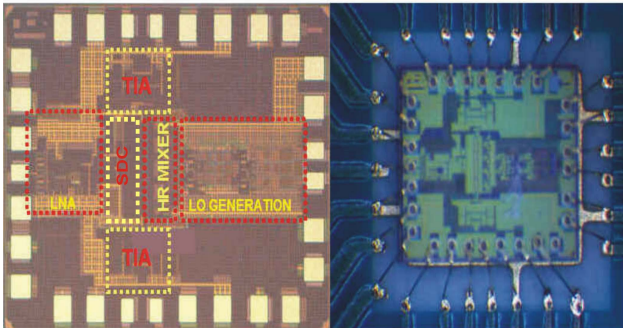


Fig. 7. Die photomicrograph and die-on-board

Fig. 7 shows the chip photo together with the die mounted on a PCB with bonding wires and interconnect.

The active chip area of the receiver front-end including the RF signal path and the LO generation is $1600\mu\text{m} \times 1088\mu\text{m}$ (see Fig.7). The active chip area of the RF signal path is $980\mu\text{m} \times 1070\mu\text{m}$.

The power dissipation of the receiver front-end is 32mW at a supply voltage of 1.2V. The power dissipation of the LO generator is not taken into consideration since this configuration of the LO generator is used only for measurements.

In Fig. 8 and Fig.9 the measured voltage gain of the receiver front-end as a function of IF frequency and RF frequency, respectively, are presented. The voltage gain is 24dB. The voltage gain as a function of the IF frequency is measured for an input frequency of 1GHz.

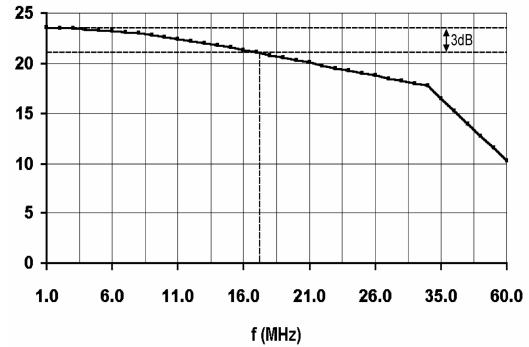


Fig. 8. Measured voltage gain as a function of IF frequencies

The 3-dB bandwidth of the low pass filter at the output of the mixer is 16MHz (see Fig. 8) and the 3-dB bandwidth of the receiver front-end is 1.7 GHz as shown in Fig. 9.

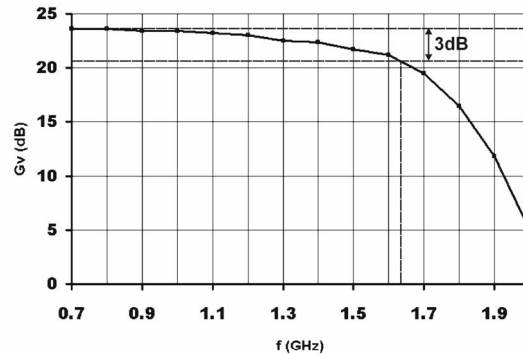


Fig. 9. Measured voltage gain as a function of RF frequencies

The measured NF of the front-end is 5.5dB. As the implemented receiver front-end has a single-ended input, it does not require a BALUN when connected to an antenna. Therefore, the noise figure impairment of typically 1.5 to 2.5dB is prevented, and a higher noise figure of the implemented receiver front-end is accepted.

In measurement the achieved harmonic rejection of the third and fifth harmonic are -52dB and -87dB, respectively.

The input matching ($S_{11} < -10\text{dB}$) is achieved in the frequency range 0.8GHz – 1.7GHz and it is plotted in Fig. 10.

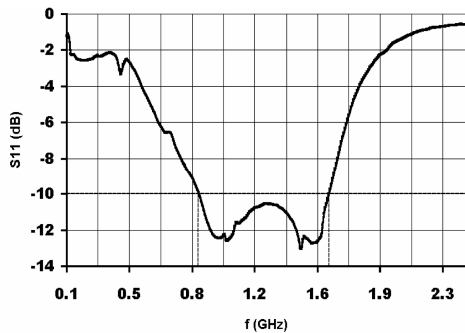


Fig. 10. Measured S_{11} parameter vs. frequency

Figure 11 illustrates the measured $IIP3$ of the implemented front-end. The two test tones are at 1GHz and at 1.001GHz. The frequency of the LO signal is 997MHz. The output fundamental signals are at 3MHz and 4MHz, while the third order intermodulation products are located at 2MHz and 5MHz. The measured $IIP3$ is -13dBm.

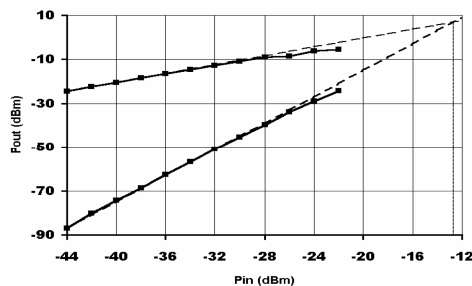


Fig. 11. Measured $IIP3$ vs. input power

Figure 12 shows the measured $IIP2$ of the front-end. The frequencies of the two test tones are 1.01GHz and 1.0103GHz. The frequency of the LO signal is 1GHz. The output fundamental signals are at 10MHz and 10.3MHz, while the second order intermodulation products are located at 0.3MHz. The measured $IIP2$ is 30dBm. In the presented receiver front-end MOS capacitors are used (MIM capacitors are not available).

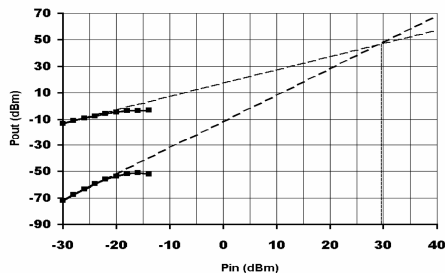


Fig. 12. Measured $IIP2$ vs. input power

The MOS capacitors are realized as a parallel-series combination of drain/source-shorted MOS transistors.

MOS capacitors deteriorate the linearity of the implemented front-end. Replacing these capacitors with MIM capacitors a better linearity performance can be obtained.

Analyzing the measured results the following features of the implemented front-end can be highlighted: low power consumption, high voltage gain and small chip area. Apart from this, it operates at a low supply voltage of 1.2V. The front-end has a moderate noise figure and a moderate $IIP3$. Linearity can be improved by replacing the MOS capacitors with MIM capacitors. Increasing the power consumption will further improve the noise figure, the linearity and the bandwidth of the receiver chain.

IV. CONCLUSION

A novel broadband inductorless RF front-end has been presented. The circuit is implemented in a baseline 90nm CMOS LP process. The main features of the proposed solution are: operation in the frequency range from 0.8GHz up to 1.7 GHz, low power consumption (32mW), high voltage gain (24dB), moderate noise figure (5.5dB) and small occupied chip area (only 1mm^2). In addition, it operates at a low supply voltage (1.2V). This is an important requirement for modern baseline deep sub-micron CMOS processes and one of the most difficult to fulfill in the RF part of the front-end. In a combination with a tunable RF filter after the antenna it represents a cost-effective solution for a multi-standard RF front-end. Multi-mode and multi-band applications can be envisaged as an application area of this design.

REFERENCES

- [1] F. Agnelli, G. Albasini, I. Bietti, A. Gnudi, A. Lacaita, D. Manstretta, R. Rovatti, E. Sacchi, P. Savazzi, F. Svelto, E. Temporiti, S. Vitali and R. Castello, "Wireless multi-standard terminals: system analysis and design of a reconfigurable RF front-end," *IEEE Circuits and Systems Magazine*, vol. 6, no. 1, pp. 38-59, First quarter 2006.
- [2] R. Bagheri, A. Mirzaei, S. Chehrizi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang and A. A. Abidi, "An 800-MHz - 6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860 – 2876, December 2006.
- [3] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K. C. Tsai, C. W. Lee; P. R. Gray, "A 1.75GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers" *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2003 – 2015, December 2001.
- [4] S. H. Galal, H. F. Ragaie and M. S. Tawfik, "RC sequence asymmetric polyphase networks for RF integrated transceivers," *IEEE Transactions on Circuits and System-II: Analog and Digital Signal Processing*, vol.47, no. 1, pp. 18-27,2000.