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Citation for published version (APA):

Palermo, S. M., & Pineda de Gyvez, J. (2000). A multi-band single-loop PLL frequency synthesizer with dynamically-controlled switched tuning VCO. In *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, 2000, 8-11 August 2000, Lansing, Michigan* (Vol. 2, pp. 818-821). Institute of Electrical and Electronics Engineers. <https://doi.org/10.1109/MWSCAS.2000.952881>

DOI:

[10.1109/MWSCAS.2000.952881](https://doi.org/10.1109/MWSCAS.2000.952881)

Document status and date:

Published: 01/01/2000

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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A Multi-Band Single-Loop PLL Frequency Synthesizer with Dynamically-Controlled Switched Tuning VCO

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Abstract- A phase-locked loop (PLL) frequency synthesizer architecture for multiple-band applications is presented. A dynamically-controlled switched tuning voltage-controlled oscillator (VCO) is used to achieve superior frequency range and phase noise performance over a conventional PLL. Implemented in 1.2 μ m CMOS, the PLL has a 111-290MHz range, phase noise of -92.3dBc/Hz at a 50kHz offset, and dissipates 9mW from a 2.7V supply.

I. INTRODUCTION

A frequency synthesizer used in multi-band applications is required to produce a spectrally pure output signal over a wide frequency range. This presents a design challenge because PLL performance is limited by VCO tunability and phase noise. A wide range VCO implies a high conversion gain, K_{VCO} , for a given tuning voltage range. This results in increased noise power at a given frequency offset due to FM modulation of control voltage noise [1]. Also, loop stability limits increasing PLL bandwidth excessively to minimize VCO phase noise contribution [2]. Double-loop architectures are often used to widen the PLL bandwidth while insuring stability [3]. However, this approach requires effectively twice the amount of circuitry of a standard single-loop PLL. This results in larger circuit area and increased power consumption. An effective technique to achieve a wide VCO tuning range, while preserving a low VCO conversion gain to improve phase noise performance, is to use a VCO with digitally switched tuning elements [4]. Using this type of oscillator provides an increased tuning range at the expense of PLL design complexity because the switched tuning control system must be designed carefully to insure locking and stability over the entire frequency range.

This paper presents a wide range PLL frequency synthesizer implemented in 1.2 μ m CMOS. The single-loop PLL achieves a range greater than an octave (111-290MHz) without compromising phase noise performance by using a switched tuning VCO [4]. The advantages of using the proposed multi-band architecture are: 1) a wide frequency range is achieved while maintaining a relatively low VCO conversion gain to improve phase noise performance; 2) a single-loop architecture is used for minimal duplicated circuitry; and 3) the adaptive switch control system allows the PLL to lock in different frequency bands with no external control signals. The multi-band PLL achieves wider tuning range with superior phase noise performance over a conventional PLL presented for comparison. The PLL architecture, conditions for loop stability, and circuit design are detailed. Prototype measurement results are also presented.

II. MULTI-BAND PLL ARCHITECTURE

Unlike typical phase-locked loops which cover a given frequency range with only one band of operation, the multi-band PLL has cascaded frequency bands to cover the entire range of interest. A switched tuning VCO implements the different frequency bands of the PLL shown in Fig. 1. The VCO is continuously controlled by the loop filter output voltage and digitally controlled by a switch control network that monitors the VCO control voltage during acquisition. The switch control network detects the control voltage crossing a certain threshold and changes the oscillator's frequency band by applying different capacitive tuning loads. Fig. 2 illustrates a case where the PLL output is initially oscillating too slow. Assuming a positive VCO conversion gain, the control voltage rises as the loop dynamics take over to increase the output frequency. After the control voltage passes the positive threshold of the initial frequency band, the oscillator is changed to the next higher frequency band by the digital switch control network. The control voltage is then grounded to set the oscillator operating in the mid-band region of the new frequency band and control is returned to the normal loop dynamics. This mechanism repeats until the oscillator locks in the correct band.

For systems with a damping factor $\zeta < 1$, a frequency overlap is introduced between adjacent bands to prevent oscillation between bands due to the characteristic overshoot and ripple of the control voltage during acquisition. The amount of band overlap can be determined by converting this overshoot voltage into a frequency value using the VCO conversion gain. As way of illustration assume a system with

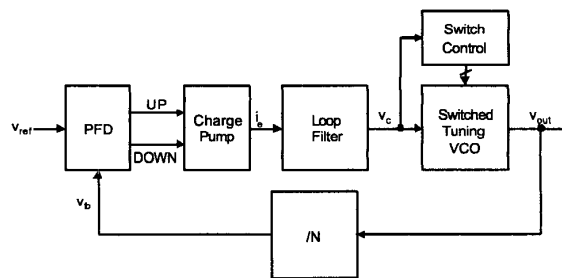


Fig. 1. Multi-band PLL frequency synthesizer block diagram.

This work was supported by Texas Instruments Incorporated.

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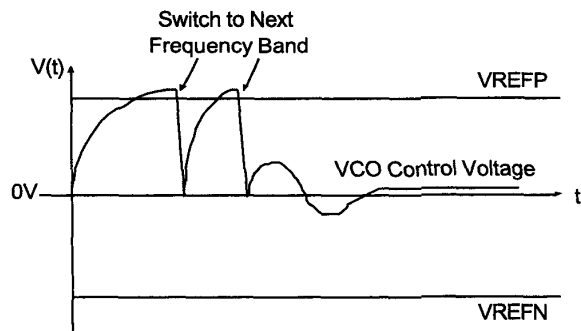


Fig. 2. VCO control voltage with switched tuning.

a damping factor $\zeta = 0.707$ shown in Fig. 3. Band-1 has a positive threshold, L^+ , a symmetric negative threshold, L^- , and a center frequency, f_{c1} , that corresponds to 0V. When a reference frequency step is input into the system the control voltage reaches a peak value of $L^+ = 1V$ before settling onto a value of $0.83L^+$. The frequencies that correspond to $0.83L^+ - L^+$ cannot be synthesized in band-1 because the overshoot will force the switch control network to switch to the next higher frequency band. To synthesize the frequency that corresponds to $0.83L^+$, the overshoot of $\theta = 0.17L^+$ forces L^- of band-2 to be placed at a maximum of $L_2^- = 0.66L^+$. Thus the overlap amount between adjacent bands due to the characteristic overshoot is 17% of the total band for $\zeta = 0.707$ systems. An additional 8.4% overlap is necessary to accommodate the control voltage ripple caused by discrete charging of the loop filter by the charge pump. Overall, a 30% overlap is an appropriate starting value in the design procedure. The overlap may be decreased with an increased damping factor and a narrower loop bandwidth.

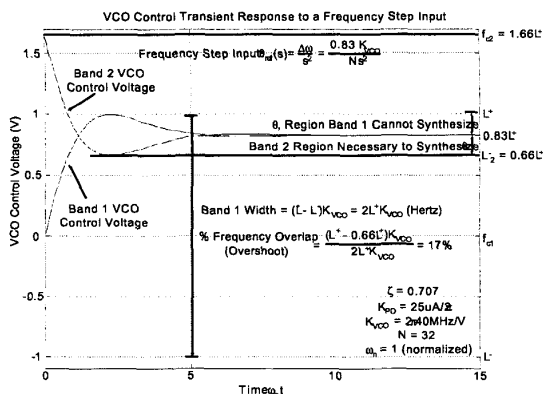


Fig. 3. VCO control voltage frequency step response used to determine adjacent band frequency overlap.

III. CIRCUIT DESIGN

A. Switched Tuning Voltage-Controlled Oscillator

The VCO is a three-stage ring oscillator with inverting delay cells loaded with one continuously tuned capacitive load, C_C , and three discrete tuning capacitors, C_{D1-3} , as shown in Fig. 4. Changing the propagation delay of the inverting cells by adjusting the effective amount of loading capacitance is used to tune the VCO output frequency. The MC NMOS active resistors are tuned with the controlling voltage, v_c , to adjust the effective value of the 600fF C_C capacitors the delay cells must drive. The VCO displays a negative conversion gain due to the NMOS active resistors because as the control voltage increases the active resistance value decreases causing the delay elements to be loaded by more effective capacitance which increases their propagation delay. It is optimal to make capacitor C_C much larger than the delay cell input transistors' parasitic capacitors in order to have a wide tuning range.

Switching in the 300fF discrete capacitors, C_{D1-3} , allows the oscillator to achieve a wide range of operation while maintaining a low conversion gain. Having three discrete tuning capacitors of the same value permits the oscillator to operate in four different frequency bands. The amount of adjacent band overlap is inversely proportional to the amount of discrete capacitance that is incrementally applied to the delay cells. This frequency overlap may be adjusted to suit individual design requirements by appropriately sizing the discrete capacitors. A 33.7% minimum adjacent band overlap is implemented insuring PLL stability across the entire frequency range. The VCO displays a measured range of 111-297MHz with a low average gain of -41.7MHz/V with a 2.7V supply.

B. VCO Switch Control System

The switch control network shown in Fig. 5 controls the discrete capacitive loading applied to the VCO. The two comparators, designed with over 300mV of hysteresis to avoid unnecessary switching due to control voltage ripple, are used to detect when the control voltage significantly crosses the $\pm 0.8V$ $VREFP$ or $VREFN$ thresholds. Loop control is then switched from the normal loop dynamics to the switch control network. Depending on which threshold is crossed, a rising edge occurs on the $B-UP$ or $B-DOWN$ signal. The

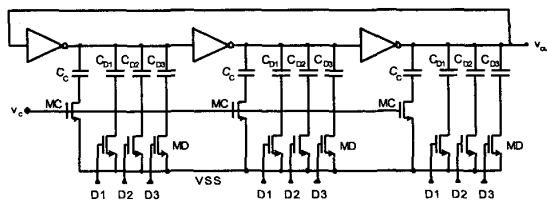


Fig. 4. Switched tuning VCO.

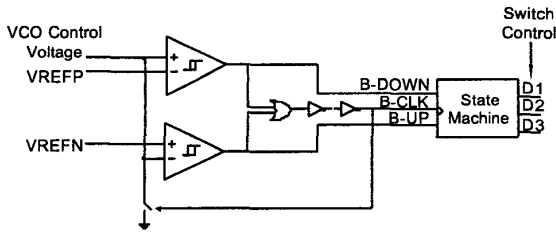


Fig. 5. VCO switch control system.

state-machine is then clocked to change the $D1-D3$ switch control signals accordingly and adjust the amount of discrete capacitance that the VCO delay cells must drive. The control voltage is grounded momentarily to reset the tuning system and set the VCO oscillating in the middle region of the next frequency band. When the control voltage has returned within the thresholds sufficiently, the $B-UP$ or $B-DOWN$ signals return low. The switch which grounds the control voltage is opened and control is returned to the normal loop dynamics.

C. Phase/Frequency Detector, Charge Pump, & Loop Filter

The phase/frequency detector (PFD), charge pump, and loop filter are shown in Fig. 6. The PFD – charge pump configuration cancels the negative VCO gain to insure a negative feedback loop. The PFD controls the charge pump with the $UP/DOWN$ signals produced during each cycle of the reference and VCO feedback signal. A leading rising edge on the frequency divided VCO feedback signal, v_{fb} , forces a rising edge on the $DOWN$ signal which causes the charge pump to positively charge the loop filter. This causes the VCO control voltage to rise and the output frequency to decrease due to the negative VCO gain. Conversely, if a leading rising edge occurs on v_{ref} the filter will be negatively charged and the output frequency will increase.

Designing the PFD reset delay to be longer than its output delay to the charge pump effectively eliminates any dead-zone as the phase of the reference signal and VCO feedback signal approach lock. The PFD output signals become synchronized with similar minimum width when the loop is locked due to the reset delay.

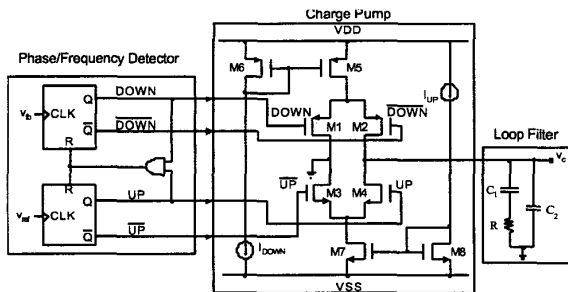


Fig. 6. Phase/frequency detector, charge pump, and loop filter.

The charge pump current, I_{UP}/I_{DOWN} , is nominally $25\mu A$ to provide a loop gain of 10^6 for loop stability. An average loop bandwidth of approximately $230kHz$ is set with the $62.2pF$ poly1-poly2 capacitor C_1 . The $6pF$ capacitor C_2 reduces ripple on the VCO control voltage caused by the switching interaction between the charge pump and loop filter. A nominal damping factor of 0.7 is set with the $31.8k\Omega$ poly1 resistor R .

IV. PLL MEASUREMENT RESULTS

The multi-band PLL, shown in Fig. 7, was fabricated in a standard $1.2\mu m$ n-well two-poly two-metal CMOS technology through MOSIS. The complete synthesizer occupies an area of $1.04 mm^2$.

The dynamic operation of the multi-band PLL is verified experimentally by the VCO control voltage response to a frequency step input. Fig. 8 shows the control voltage response as the output frequency goes from $240MHz$ to $190MHz$ due to a reference frequency step input. The PLL is initially operating in band-4 with no discrete tuning capacitors applied to the VCO delay cells. When the reference frequency is decreased, the loop dynamics take over and the control voltage increases past the positive threshold of band-4. This triggers the switch control system to take control of the loop. The VCO capacitive loading is increased by switching in one discrete capacitor to each of the delay cells. The control voltage is then grounded to reset the switch control system and set the oscillator operating in the middle region of band-3. Loop control is then returned to the normal loop dynamics and the PLL locks to synthesize the $190MHz$ signal shown in Fig. 9. An acquisition time of $8.56\mu s$ is measured for the $-50MHz$ frequency step.

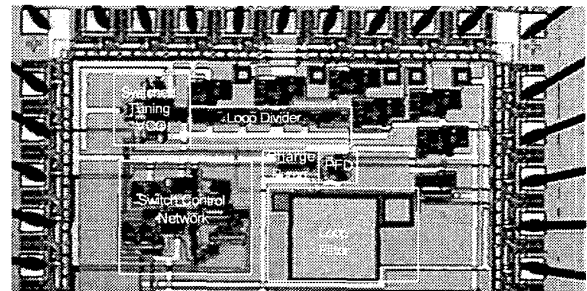


Fig. 7. Chip photograph.

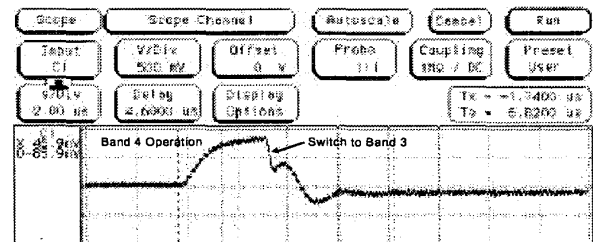


Fig. 8. Experimental switched tuning VCO control voltage step response.

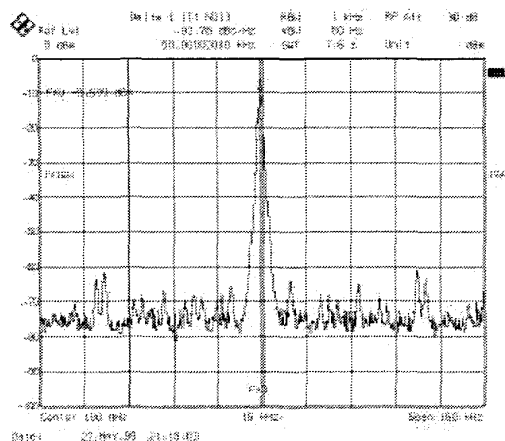


Fig. 9. Frequency synthesizer 190MHz output spectrum.

Table I summarizes the experimental multi-band PLL frequency synthesizer performance. The PLL operates over a range of 111–290MHz, as shown in Fig. 10. The average phase noise is -92.3dBc/Hz at a 50kHz offset. This phase noise performance is maintained throughout the entire frequency range with the majority of points displaying between -90 to -95dBc/Hz values. Stability is achieved over the entire range due to the overlap between the VCO bands. This hysteresis between adjacent bands minimizes the band-to-band switching that occurs during acquisition. This also allows the multi-band PLL to be used for modulation or demodulation applications over the entire range because no discrete tuning capacitors are switched over a defined modulation bandwidth [4].

A PLL using a conventional single band VCO that operates over a similar range was designed, fabricated, and tested for comparison. The same circuit blocks are implemented in this design except for the VCO. The oscillator is the same type as used in the multi-band PLL design except the discrete tuning capacitors and switch transistors have been removed so that it operates in only a single band. The VCO displays a measured conversion gain of -97MHz/V . This is more than double the conversion gain of the multi-band oscillator. The increase in conversion gain is due to the reduction in the amount of parasitic capacitance associated with the routing of the discrete tuning capacitors. Thus the single tuning capacitor is a larger percentage of the overall capacitance at the output of the individual VCO delay cells and has an increased effect on the propagation delay.

TABLE I
MEASURED MULTI-BAND PLL PERFORMANCE

Items	Measured Results
Technology	1.2 μm 2-Metal, 2-Poly
PLL Active Area	1.04 mm^2
Frequency Range	111-290MHz
Avg. VCO Gain	-41.7MHz/V
Avg. Phase Noise @ 50kHz	-92.3dBc/Hz
Power Dissipation @ 2.7V	Core PLL = 9mW Chip = 29.1mW

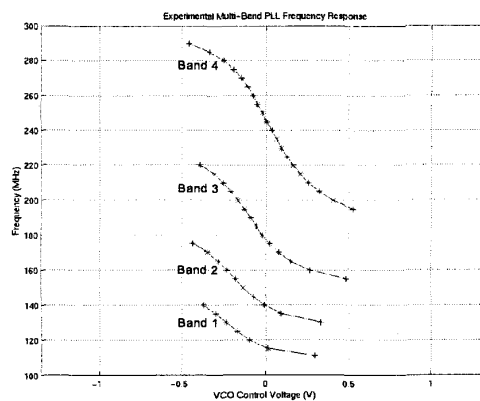


Fig. 10. Experimental multi-band PLL frequency response.

Experimental results show the multi-band PLL achieves a 20% wider frequency range with an average 7.3dB superior phase noise performance when compared to the single-band PLL design. Acquisition times were similar for both synthesizers.

The multi-band PLL frequency synthesizer dissipates 29.1mW from a 2.7V power supply while operating at a maximum frequency of 290MHz. However, if the output buffers required to drive the signals off-chip for measurement are excluded, the power dissipation of the core PLL synthesizer is only 9mW.

V. CONCLUSION

The design and implementation of a proposed multi-band PLL frequency synthesizer have been presented. A dynamically-controlled switched tuning VCO provides a low gain over a wider range for improved phase noise performance compared to a conventional PLL architecture. No external control signals are necessary for the switched tuning VCO, as the control circuitry is triggered only by the normal loop dynamics. Experimental results serve as proof of concept that the presented architecture is suitable for multi-band applications. The implementation of the proposed architecture in sub-micron technology could be used to increase the synthesizer's operation into the gigahertz frequency range and allow the use of a higher Q switched tuning LC oscillator for enhanced phase noise performance.

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