A 2.98pJ/conversion 0.0023mm2 Dynamic Temperature Sensor with Fully On-Chip Corrections

Citation for published version (APA):

Document license:
Unspecified

DOI:
10.1109/ISSCC42615.2023.10067789

Document status and date:
Published: 01/01/2023

Document Version:
Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

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Download date: 24. Jul. 2023
A 2.98pJ/conversion 0.0023mm² Dynamic Temperature Sensor with Fully On-Chip Corrrections

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Nowadays, many battery-operated SoCs for IoT and environmental monitoring applications are equipped with temperature sensors. In these miniaturized systems, power and area are two critical concerns. One challenge for temperature sensors is that they are sensitive to process corners and random mismatch. Generally, a 2-point trim and systematic non-linear error removal are required, especially for resistor-based sensing front-ends with two types of resistors, whose spread is partially uncorrelated [1,2]. These corrections are done off-chip and digitally in most publications. In particular for low power sensors, they may consume more power and area than the sensor itself when integrated on-chip [3]. This work presents a resistive temperature sensor that integrates on-chip offset, gain and non-linearity correction techniques, while keeping state of the art power and size performance. The prototype consumes 2.98 pJ/conversion with an area of 0.0023 mm² including all the correction techniques and achieves <0.7-0.6 °C inaccuracy.

Fig. 1 shows the architecture of the temperature sensor, which is similar to [5,6]. It consists of a resistive bridge sensor to sense the temperature, a 9-bit asynchronous SAR ADC to read out the temperature and a power gating switch (MGP) to minimize the leakage of the system. Power switches (M1-M4) are applied to the Wheatstone bridge to realize system level correlated double sampling (controlled by a direction signal DIR) and to duty-cycle the resistive sensing front-end. Thanks to the dynamic operation, P-type polysilicon resistors (Rp) and N-type diffusion resistors (Rn) with a relatively small value of 100 kΩ can be employed with high energy efficiency [5]. On top of this, the offset, gain and non-linearity correction techniques are integrated into the ADC. The basic principle of the three corrections is to replicate the errors caused by the resistive sensing front-end in the ADC but with an opposite polarity so they will cancel out each other for the final output. To minimize area overhead, the corrections re-use the existing DAC capacitance, supplemented with several small capacitors (C0, Caux, Cb and Cauxb) plus extra logic. First, offset correction with a range of ±2⁰²¹ LSB is realized by pre-setting the DAC capacitors of an N-bit DAC during the tracking phase and then resetting them after the sampling moment [6] to induce a voltage step that compensates for the offset. Fine tuning capacitors (Cf) are added to further improve the offset correction accuracy to ±1 LSB. By adding a programmable capacitor (Cg), the ADC range can be adjusted to compensate gain errors [6]. A 3-bit Cg array is used in this work to achieve a gain correction range of 6.4% with a step size of 0.8%.

The differential output of a Wheatstone Bridge (WhB) sensor front-end can be calculated as shown in Fig. 1, where α0 and α1 are the temperature coefficients for Rp and Rn respectively. Since α0 is not equal to -α1, Vout is inherently a non-linear function of ΔT. This mostly second-order distortion is the dominant non-linearity source of the entire system. While offset and gain errors are randomly distributed for each sample and thus could be corrected based on batch-level characterization. By means of the analog correction, the measured offset value is improved from 58-to-100 LSB to ±0.5 LSB. Because of the analog non-linearity correction, the systematic non-linearity is significantly mitigated. The non-linearity correction logic requires 6 XOR, 11 NAND and 12 NOT gates.

The measured offset and gain inaccuracy from approximately 2.73 °C to 0.68 °C. The measured RMS resolution for this sensor is around 0.47K at 750MHz output and 750mV supply, which equals to 1.74 °C/0.0023mm² power consumption. The sensor, including all correction functions, consumes 2.98pJ/conversion and can at least maintain this efficiency from 1ks/s to 100ks/s.

A 3-bit Cg array is used in this work to achieve a gain correction range of 6.4% with a step size of 0.8%.

The output of a Wheatstone Bridge (WhB) sensor front-end can be calculated as shown in Fig. 1, where α0 and α1 are the temperature coefficients for Rp and Rn respectively. Since α0 is not equal to -α1, Vout is inherently a non-linear function of ΔT. This mostly second-order distortion is the dominant non-linearity source of the entire system. While offset and gain errors are randomly distributed for each sample and thus could be corrected based on batch-level characterization. By means of the analog correction, the measured offset value is improved from 58-to-100 LSB to ±0.5 LSB. Because of the analog non-linearity correction, the systematic non-linearity is significantly mitigated. The non-linearity correction logic requires 6 XOR, 11 NAND and 12 NOT gates.

To confirm functionality, Fig. 4 shows the measured temperature error curves with various offset, gain and non-linearity correction settings. As shown in Fig. 4 (top left), a ±4LSB offset could already result in significant temperature errors (around 2 °C). Simulations show that the offset of the sensor can be tens of LSBs, which makes it the largest error source. Mismatch also results in random gain variations but in a secondary way [6]. As can be seen from Fig. 4 (top right), a 2.2% variation could result in a temperature error of around 2.5 °C. Besides, the temperature error also depends on the non-linearity compensation setting, whose magnitude is controlled by Cg (Fig. 4 bottom). For the given batch of samples, the appropriate compensation setting helps to improve the maximum inaccuracy from approximately 2.73 °C to 0.68 °C.

The die size is 0.0023 mm² including all the correction techniques and achieves <0.7-0.6 °C inaccuracy. This work presents a resistive temperature sensor that integrates on-chip offset, gain and non-linearity correction techniques, while keeping state of the art power and size performance. The prototype consumes 2.98 pJ/conversion with an area of 0.0023 mm² including all the correction techniques and achieves <0.7-0.6 °C inaccuracy.

Fig. 5 summarizes the measured offset, gain, non-linearity and noise characteristics. With the analog correction, the measured offset value is improved from 58-to-100 LSB to ±0.5 LSB. The gain variation is improved from 3.5% to 0.8%. As can be seen from Fig. 5, with the analog non-linearity correction, the systematic non-linearity is significantly mitigated. There are still offset and gain errors remaining since the offset and gain corrections are quantized. This sensor achieves an inaccuracy of <0.7-0.6 °C and the resulting relative inaccuracy is 0.97%. The measured RMS resolution for this sensor is around 0.47K at room temperature. Thanks to CDS, 1 LSB is mitigated. The measured output spectra is shown in Fig. 5 (bottom right). The performance of this work is summarized in Fig. 6. Compared to state-of-the-art WhB temperature sensors, it is the only low-power and compact WhB temperature sensor which integrates on-chip offset, gain and non-linearity error corrections. These features make it suitable for IoT ambient temperature monitoring applications in which low power and small size are demanded, together with moderate resolution.

Acknowledgement

This work is financed by the Dutch Research Council (NWO) with project number 16594. We kindly acknowledge EUROPRACTICE for its MPW and design tool support. References

Figure 23.6.1: Architecture of the dynamic temperature sensor and output voltage as function of temperature

Figure 23.6.2: Operation of the proposed non-linearity correction

Figure 23.6.3: Circuit implementation of the proposed non-linearity correction. Circuit implementation of the non-linearity correction

Figure 23.6.4: The measured sensor's temperature errors with various offset, gain and non-linearity correction settings

Figure 23.6.5: The measured sensor's offset, gain, and overall error for 15 samples, and noise characteristics

Figure 23.6.6: Summary of measurement results and comparison with state-of-the-art WhB temperature sensors
Figure 23.6.7: Die photo