A 0.0033 mm\(^2\) 3.5 fJ/conversion-step SAR ADC with 2× Input Range Boosting

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A 0.0033 mm$^2$ 3.5 fJ/conversion-step SAR ADC with 2× Input Range Boosting

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Abstract—This paper proposes an input range boosting technique for successive-approximation-register (SAR) analog-to-digital converters (ADC). By performing a pre-comparison and switching the DAC accordingly, the input range of a SAR ADC can be doubled with limited power and area overhead. This effectively improves the power efficiency by relaxing the noise requirement and improves the area efficiency by using less DAC capacitors. A prototype ADC is fabricated in 65 nm CMOS and occupies an area of 0.0033 mm$^2$. It consumes 34.06 µW at 10 MHz sampling rate from a 1 V supply. The measured SNDR is 62 dB for a 5 MHz bandwidth, resulting in a Walden figure of merit (FoM$_W$) of 3.28 fJ/conversion step.

Index Terms—Analog-to-digital converter (ADC), flying capacitor sampling, internet of the things, input range boosting, successive approximation register (SAR).

I. INTRODUCTION

Moderate-resolution ADCs are essential in many IoT and biomedical applications. For example, for miniature ultrasound probes, ADCs with a resolution of 10-12bit and tens of MHz sampling rate are needed [1], [2]. For imaging, an array of digitizers is required. Hence, the chip area and power consumption of each channel are critical. SAR ADCs are the most popular choice in these applications thanks to their high efficiency. For SAR ADCs with moderate resolution, usually the DAC occupies above 50% of the area and the comparator consumes a large portion of the total power. These area and power limitations originate from the absolute noise requirements, and cannot be overcome easily. What’s more, advanced techniques, such as noise shaping, may not be that efficient for converters with moderate resolution and relatively high bandwidth due to the extra overhead and required over-sampling [3]. Alternatively, boosting the input signal power beyond the regular input range (IR) can be a straightforward and effective way to enhance SNR [4], [5].

To extend the input range of a converter, [4] employs two sub-ADCs, each of them serving for half of the input range. It achieves high energy efficiency with a 0.3 V supply. However, two sets of hardware are required, which increases chip area. Besides, due to mismatch between the two sub-cells, redundancy and foreground calibration are essential to avoid overrange and meet the linearity requirements. In [5], a 1.5× input range extension technique based on analog prediction is proposed. The resulting area overhead is small by reusing most of the existing hardware. However, a maximum timing duration for prediction is required to ensure accurate compensation, which may increase the required input driving strength.

This work presents a SAR ADC with 2× input range adopting a similar principle as [5]. Flying capacitor sampling is used to avoid prediction errors and the equivalent input range is further boosted to 2× without doubling the hardware.

The remainder of this paper is organized as follows: Section II introduces the proposed input range boosting technique. Its operation and circuit imperfections are discussed. Section III describes the implementation details of this work. Section IV presents the measured results. Finally, Section V concludes this paper.

II. PROPOSED INPUT RANGE BOOSTING TECHNIQUE

A. Operation

The operation of the proposed input range boosting procedure in different timing phases, together with the timing diagram is shown in Fig. 1. For the sake of simplicity, a single-ended diagram is shown. The actual work is implemented in a differential way and the original input range is $[-V_{ref}, V_{ref}]$. 

Fig. 1: Operation of the proposed input range boosting technique (a) and timing diagram (b).
\[ V_{\text{in,cmp}} = V_{\text{in}} - V_{\text{ref}} \]

\[ D_{\text{pre}} = D_{\text{ref}} \]

\[ V_{\text{in,cmp}} = V_{\text{in}} - V_{\text{ref}} \]

\[ D_{\text{ref}} = \frac{2kT}{C_S} + \frac{2kT}{C_{\text{DAC}}} \]

\[ V_{\text{ref,f}} \], which is within the regular conversion range. Then, a regular SAR conversion starts.

**B. Non-idealities**

1) **Sampling noise:** By sampling the input signal with a flying-capacitor, the sampling noise power of the differential converter is now calculated as:

\[ \frac{2kT}{C_S} + \frac{2kT}{C_{\text{DAC}}} \]

which is \( \frac{C_S + C_{\text{DAC}}}{C_S} \) times larger than the original sampling noise \( (2kT/C_{\text{DAC}}) \). A larger \( C_S \) helps to reduce this overhead. Fortunately, \( C_S \) is not that sensitive to mismatch and thus can be implemented in an area-efficient way.

2) **Mismatch:** The matching of \( C_S \) does not matter for the ADC performance, since it affects all voltage steps in the same way, and thus linearity is maintained. However, the matching of the \( C_{\text{DAC}} \) capacitors is critical. Fig. 4 shows the simulated SNDR of a 10-bit SAR ADC with the proposed input range boosting technique, a regular 11-bit SAR ADC and a regular 10-bit SAR ADC with DAC mismatch. Each point is obtained by 1000 Monte Carlo simulations. As can be seen, with the proposed IR boosting technique, the SNDR of a SAR ADC can be improved by 6 dB. What's more, compared to a conventional 11-bit SAR ADC, this approach can achieve slightly better SNDR with 50% less DAC area, because there are less elements (and thus less errors) involved in the DAC operation.

**III. CIRCUIT IMPLEMENTATION**

**A. Overview**

Fig. 5 shows the schematic and main design parameters of this work. For the track and hold (T&H) circuit, a 1 pF sampling capacitor is used. \( S_1 \) is implemented as a bootstrapped switch and \( S_2 \) is implemented as a clock boosted switch for linearity requirements. For the DAC implementation, the 3 MSBs adopt a split monotonic switching scheme and the remaining LSBs adopt a conventional switching scheme as a compromise of DAC switching energy and logic energy.
Besides, self-synchronized SAR logic [6] and a two-stage dynamic comparator [7] are used. On top of that, the input range boosting logic is integrated.

B. Logic implementation
An overview of the asynchronous logic used in this converter, as well as a simplified state machine, are shown in Fig. 6. The clocks signals of \( \varphi_1 \) and \( \varphi_2 \) are provided externally. The other clock phases are generated internally. As shown in Fig. 6(b), a falling edge of \( \varphi_2 \) will move the ADC from the tracking state to the pre-cmp state. Here, the DAC is controlled by the pre-cmp logic. A falling edge of \( \varphi_2 \) will move the ADC from the pre-cmp state to the reset state, where the DAC is reset. A falling edge of the reset phase, which is generated by an internal delay, will move the ADC from the reset state to the SAR conversion state, where the DAC is controlled by the SAR register. The circuit operation of each state is as explained in Section II-A.

C. Layout implementation
The overall layout design is shown in Fig. 7. Since the capacitors occupy most of the area, their implementation is the most important consideration in terms of layout design. In this work, the sampling capacitor \( C_S \) is implemented by regular MOM capacitors from the library. The DAC capacitors are implemented by custom designed unit-length capacitors proposed in [6]. To further save area, the DAC capacitors are placed on the top of the ADC circuity (Metal 6 and 7) and vertically connected to the drivers.

IV. Measurement results
The prototype ADC is fabricated in 65 nm CMOS and occupies an area of 0.0033 mm\(^2\). Fig. 8 shows its die micrograph. It is operated from a 1 V supply voltage, which is also the \( V_{\text{ref}} \) voltage. The \( V_{\text{CM}} \) voltage is set to 0.5 V in measurements, but its accuracy does not affect the overall performance.

Fig. 9 shows the measured spectra with the regular SAR mode (‘IR×1’) and with the proposed input range boosting mode (‘IR×2’), respectively. They are measured with an input close to the ADC bandwidth and a 10 MHz sampling rate. The measured ENOB is 9 bit for this prototype at ‘IR×1’ mode, where the maximum input signal power is -0.32 dBFS. With input range boosting, the maximum input signal power is improved to 5.72 dBFS and the measured ENOB is improved to 10.04 bit. The measured INL and DNL without and with input range boosting are shown in Fig. 10, using a 1 million points histogram test.

Fig. 11 shows the measured SNDR for both operation modes as a function of input amplitude. The measured DR is 56 dB
Fig. 9: Measured spectra without (a) and with (b) 2× input range boosting.

Fig. 10: Measured INL and DNL without (a) and with (b) input range boosting.

for ‘IR×1’ mode and 62.1 dB for ‘IR×2’ Mode. As can be seen, the maximum input amplitude as well as the DR are improved by 6 dB with the proposed input range boosting technique.

Fig. 12 shows the power breakdown of this prototype at 10 MHz sampling rate without and with input range boosting. The total power consumption with input range boosting is 34.06 µW, which is 14.8% more compared to its regular SAR mode.

Finally, table I summarizes the performance of this ADC and compares it with other designs. Compared to [4] with 2× input range, this work is 11× smaller. Compared to other state-of-the-art designs, this work achieves comparable energy-efficiency and area efficiency with 2× input range.

V. CONCLUSION

This work presents a SAR ADC with an input range boosting technique. With input range boosting, N-bit hardware can be used to realize N+1 bit resolution, which improves the area efficiency. Also, the absolute noise requirement is relaxed, which improves the power efficiency. The prototype fabricated in 65 nm CMOS occupies an area of 0.0033 mm² and consumes 34.06 µW at 10 MHz sampling rate. The measured SNDR is 62.1 dB and the SFDR is 83.3 dB, resulting in a Walden figure of merit of 3.28 fJ/conversion. These features make this work suitable for applications where power and area efficient ADCs are desired.

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TABLE I: Performance summary and comparison

<table>
<thead>
<tr>
<th>Technology [nm]</th>
<th>90</th>
<th>65</th>
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<tr>
<td>Area [mm²]</td>
<td>0.035</td>
<td>0.0013</td>
<td>0.0013</td>
<td>0.0033</td>
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<tr>
<td>Supply voltage [V]</td>
<td>0.3</td>
<td>0.8</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Resolution [bit]</td>
<td>11</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Sample rate [MS/s]</td>
<td>0.6</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Bandwidth [MHz]</td>
<td>0.3</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Ideal input swing [V ref]</td>
<td>±2</td>
<td>±1.5</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>Power [µW]</td>
<td>0.187</td>
<td>18.65</td>
<td>24</td>
<td>29.66</td>
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<tr>
<td>ENOB [bit]</td>
<td>10</td>
<td>9.74</td>
<td>9.18</td>
<td>9.00</td>
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<tr>
<td>SFDR [dB]</td>
<td>72.0</td>
<td>82.2</td>
<td>72.46</td>
<td>76.3</td>
</tr>
<tr>
<td>FoM [W/(ENOB × 2 × BW)]</td>
<td>0.44</td>
<td>2.2</td>
<td>4.1</td>
<td>5.79</td>
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<tr>
<td>Acknowledgment</td>
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</table>

1 FoM_W = Power/(2^ENOB × 2 × BW)
REFERENCES


