Performance and scalability of a single-stage SOA switch for 10 x10 Gb/s wavelength striped packet routing

Performance and Scalability of a Single-Stage SOA Switch for 10 × 10 Gb/s Wavelength Striped Packet Routing

T. Lin, K. A. Williams, R. V. Penty, I. H. White, M. Glick, and D. McAuley

Abstract—**This letter reports successful routing of 10 × 10 Gb/s multiwavelength optical packets using single-stage semiconductor optical amplifier switches. Performance under switching is assessed with up to ten wavelengths with particular emphasis being placed on the limit of operation. A 15.2-dB power margin is demonstrated which allows at least eight port connections with a commercially available 0-dBm output 10-Gb/s transmitter and −21-dBm sensitivity receiver.**

Index Terms—**Optical interconnect, optical packet switching, semiconductor optical amplifier (SOA).**

I. INTRODUCTION

EMERGING applications in storage area networking, short reach interconnects, and desk area networking require reconfigurability, functionality, low latency, compactness, and cost-effectiveness. Here short packet time-slots using high capacity wavelength-multiplexed data can provide an attractive solution for high capacity on demand without imposing a channel granularity which may be restrictive in terms of latency and bandwidth in the datacom environment [1]–[3]. Photonic switches offer advantages in capacity but proposed solutions with large numbers of channels have often been complex. As data routing applications require low loss broad-band switches with low complexity and low power consumption, semiconductor optical amplifier (SOA)-based switches have been of great interest. They are promising because of their high extinction ratio, high optical gain, and subnanosecond switching time.

A range of hybrid and monolithic integrated SOA switches has been studied, focusing on switch function, error and crosstalk performance under single wavelength operation [4] with second-stage wavelength routing and regeneration being implemented to achieve the necessary performance [4], [5]. Such single-wavelength schemes can, however, impose a channel granularity and a hardware complexity which may be unsuited to the datacomms environment. Reduced complexity routes to 12 node connectivity have been proposed using networks with cascaded SOA switches [2]. Here wavelength-division-multiplexing (WDM) packets at 14 × 10 Gb/s

have been assessed over paths with three discrete SOAs. An optical signal-to-noise ratio has been performed for up to 40 × 10 Gb/s channels [6]. The impact of channel provisioning on millisecond timescales has also been assessed, although here the assessed channels and the SOAs have been operated continuously [7]. Here the placement of continuously operating repeaters at regular intervals leads to a relaxed performance with respect to switched gates where a wider range of input conditions is anticipated.

The proposed architectures for SOA-based switches have largely been broadcast and select configurations [1], [4], and this is well suited to the characteristics of the SOA switch. The concatenation of power splitters, amplifier gates, and power combiners allows for the effective exploitation of inherent gain while enabling multiple inputs and outputs. This structure may subsequently be used as the generic building block in a multistage configuration to achieve higher connectivity [8]. The switch fabric topology will depend on the optimum choice of such building blocks, but little research has been performed to quantify design constraints such as power margin in relation to connectivity and data capacity.

In this work, for the first time, we assess such a single-stage SOA switch configuration in terms of its performance for 10 × 10 Gb/s WDM routing and the limits on connectivity. We study the capacity of the SOA switch and the extrapolated limit for a switched 10 × 10 Gb/s optical packet switching system from the power margin calculation by mapping out the regions for tolerable error performance under switched operation.

II. SOA SWITCH IMPLEMENTATION

For a single-stage SOA switch, it is possible to realize a network between input and output ports using power splitters and combiners. Each connection path may be switched ON or OFF using a single SOA [9]. An isolator may be placed after each SOA gate to reduce reflection. All the SOAs may be activated by means of electronic logic, e.g., field programmable gate array (FPGA) control. This switch architecture may be extended by increasing the number of SOA gates and the number of splitter stages. An $N \times N$ switch of this type requires $\log_2 (N)$ splitter stages and N^2 SOA gates. When the number of ports is not very large, i.e., $N < 16$, this architecture has the least number of SOA gates compared with other conventional space switch architectures [8]. The main drawback for this architecture is the high insertion loss. However, for moderate port number, the losses may be compensated by the gain of the SOA.
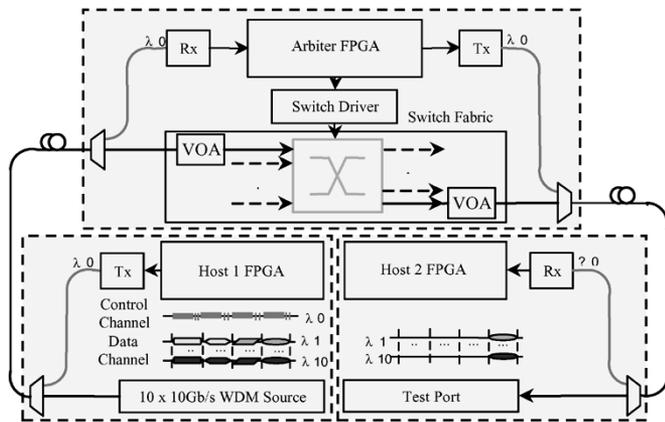
Fig. 1. 10×10 Gb/s testbed showing FPGA control scheme and the switch element.

Fig. 2. Decorrelated 10×10 Gb/s WDM data source.

Fig. 3. Switched routing performance for the center 10-Gb/s wavelength channel. (a) Input interleaved packet stream. (b) Output switched packets (55 μs/div). (c) Eye of one of the 10-Gb/s channels with the optical input power of -21 dBm.

The number of ports this architecture may support is limited by the dynamic power margin of the SOA, the number of wavelengths, and the line speed for each channel. In addition, increasing the number of splitter stages increases the insertion loss for both the input and output side of the switch fabric. This renders the splitters in this architecture equivalent to two optical attenuators for a single SOA gate. For the input side, the number of splitter stages is limited by the output power of the transmitter, while for the output side, it is limited by the sensitivity of the receiver if the remaining system loss is fixed.

III. ASSESSMENT OF 10×10 Gb/s ROUTING

The focus of the experimental work is on determining SOA performance under packet switching. As a result, a testbed configuration is used to assess routing using off-the-shelf components and is assembled to allow an operating data rate of up to 10×10 Gb/s with flexible and intelligent control (Fig. 1). The control channel is set at 1.3-μm wavelength at 1.25-Gb/s bit rate to facilitate full addressing and switch control for multiple destinations. The GBIC transceiver interfaces to the high-speed RocketI/O ports in the FPGA board. The control information precedes the wavelength-striped packet payload in the 1.5-μm channel to allow processing time. A switch driver waveform is generated to configure the optical switch to route the desired multiwavelength packet [9].

In order to test the capacity limit of the single-stage SOA switch, it is important to ensure decorrelated data for high numbers of wavelengths. Two $1:2$ broad-band splitters and two $1:4$ electrical data splitters with amplifiers and variable delays are used to decorrelate data channels (Fig. 2). Ten integrated DFB-EAM sources centered at 1550 nm on a 100-GHz grid and modulated at 10 Gb/s are used as the 10×10 Gb/s WDM source.

The payload is programmed as 94.72-μs packets with 1.28-μs guard-bands. A $2^{15} - 1$ pseudorandom bit sequence is selected to represent the data as this is a widely implemented test pattern enabling cross-comparison with other published work. This pattern length also identifies potential limitations due to distortion in the amplifier gates, while being sufficiently short to fit entirely within the available time slot. A fiber pigtailed SOA with
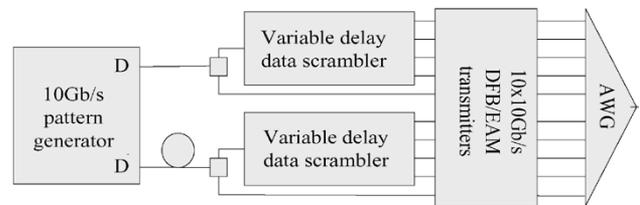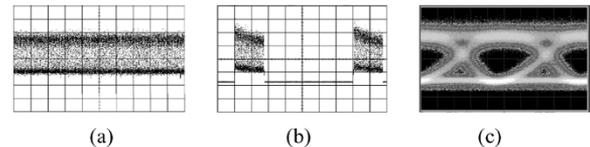
an isolator and two variable optical attenuators before and after is used to simulate the gate in a large single-stage SOA switch. The optically isolated SOA element has a linear gain of 19 dB when operating at an ON-state current of 90 mA. The 3-dB input saturation power at this current is -7.5 dBm. An Agilent 81 250 error test set, with a fast-acquisition-time external 10-Gb/s clock data recovery circuit is used to test the bit-error rate (BER) of the packet from each channel. Fig. 3 shows the output from the switch for the central wavelength channel when ten channels are running. The data source implementation restricts the optical extinction ratio to 7 dB. The role of extinction ratio on amplifier performance has not been explored in this work.

IV. EXPERIMENTAL RESULTS

The performance of the SOA switch is assessed as a function of wavelength number and combination of wavelengths to address the roles of noise, crosstalk, and saturation on the routed dynamic range. The BER is assessed when all the ten channels are running. Stable, error-free operation is demonstrated for all ten channels under routing operation with no evidence of noise floors. For Fig. 4(a), BER curves are assessed for a range of input conditions, and the value of input power is recorded which will give an error rate of 10^{-9} for a receiver sensitivity of -21 dBm, this being consistent with commercially available 10-Gb/s PIN receivers.

The upper curve in Fig. 4(a) indicates the maximum tolerated input power into the switch (MAX) while the bottom curve indicates the minimum required power (MIN). As the number of wavelengths increases, the maximum tolerable power is seen to decrease. This indicates a narrowing margin as the number of wavelengths increases. When ten wavelengths are running, the acceptable input power for the SOA is from -24 to -15 dBm. It is also noted that an increase in mean power of 10 dB for ten wavelength channels only leads to a 5-dB reduction in tolerated input power. The minimum tolerated input power is dominated by the sensitivity of the receiver. While the amplifier gain is measured to be 19 dB for the minimum input power, over the wavelength range of interest, this is observed to decrease for the maximum input powers used. Here the gain measured
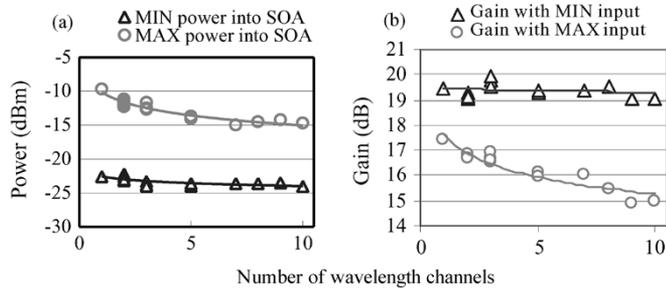
Fig. 4. (a) Minimum and maximum acceptable power into the SOA per channel; (b) gain of the SOA with minimum and maximum input power. Number of wavelength channels.

TABLE I
CALCULATED POWER MARGIN OF SINGLE-STAGE SOA SWITCH FOR DIFFERENT PORT NUMBERS (Transmitter output power = 0 dBm)

No. of Ports	Loss (one side) (dB)	Input side power margin for SOA (dBm)	Output side power margin from SOA (dBm)	Overall power margin (dB)
2	10.4	4.6-13.6	10.6-1.6	15.2
4	13.8	1.2-8.4	7.2-0	8.4
8	17.2	0-1.6	1.6-0	1.6

is 17.4 dB for one wavelength running at -10-dBm power and 15.0 dB for ten wavelengths running at a maximum tolerated power -15 dBm into the amplifier. This is shown in Fig. 4(b).

A number of channel permutations for each of the channel number points are also shown as overlapped points in Fig. 4 for the same number of wavelengths. This indicates a weak dependence on wavelength channel spacing. Logarithmic lines of least squares fit are included to assist the eye.

V. DISCUSSION

From the switched 10×10 Gb/s assessment, the power margins may be used to estimate the maximum tolerable losses, which may be introduced by additional splitter stages.

The loss from a transmitter to a receiver for a single optical path is described. The broad-band de/multiplexers used to route the 1.3-μm control channel along the same duplex link as the 1.5-μm wavelength multiplexed payload channels both incur losses of 0.5 dB. An additional 4-dB loss is introduced by the data channel de/multiplexers and a 2-dB margin is made available for connector losses. If one splitter stage with 3.4-dB loss is used on both the input and the output sides of the switch, this leads to a total loss of 10.4 dB on each side for the system.

The power margin with a commercial 10-Gb/s data transmitter operating at 0 dBm is listed in Table I for different numbers of ports supported. The input power margin for the SOA is calculated from Fig. 4 with ten channels running, while the output margin from the SOA is calculated with the -21-dBm receiver sensitivity accounting for a gain of 15 dB from the SOA. The maximum and minimum input power limits for the SOA result in a continuous range of the power margin in Table I. If a single splitter stage switch is used, this corresponds to an overall margin of 15.2 dB which is sufficient to include two additional power splitters on both input and output stages, each with 3.4-dB loss. The implementation of three stages of splitters on both input and output, therefore, allows for eight inputs and eight outputs while maintaining 10×10 Gb/s data transfer. The large margin may also be used to accommodate additional

penalty as well as loss, thereby allowing the use of multistage optical switch fabrics for higher connectivity.

By increasing the power of the transmitter, the system power margin can be further increased. If the output power of the transmitter can be increased to 5.2 dBm, the overall margin of the system can be increased to 20.4 dB, which would support four splitter stages (32 ports). If more than four stages are required, the power map for the receiver sensitivity cannot be met. Further improvements might be anticipated with either avalanche gain or optical preamplification for the receiver.

VI. CONCLUSION

This letter reports the performance of a single-stage SOA switch for wavelength striped packet routing. It is shown that for 10×10 Gb/s switching, routing can be achieved with sufficient power to operate with eight independent connections with a commercially available 0-dBm output power 10-Gb/s transmitter and a -21-dBm sensitivity receiver.

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