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Silicon heterojunction solar cell passivation in combination with nanocrystalline silicon oxide emitters

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1 Introduction Silicon heterojunction (SHJ) solar cells hold the record efficiency for crystalline silicon (c-Si) wafer-based solar cells of 25.6%. This outstanding performance is enabled by the high short-circuit current density \( J_{sc} \), facilitated by their back-contacted configuration [1]. A possibility to achieve high \( J_{sc} \) but maintain the simple cell design of conventionally contacted SHJ solar cells lies in the implementation of a more transparent front layer stack of SHJ solar cells. In the search for this, boron-doped nanocrystalline silicon oxide (nc-SiO\(_x\):H(p)) has come to great attention as the emitter layer [2–5]. The implementation of these material leads to an increase in \( J_{sc} \) compared to the use of a conventional boron-doped amorphous silicon (a-Si:H(p)) emitter layer [6]. In addition to a high \( J_{sc} \), another prerequisite to achieve outstanding high efficiencies is a high open-circuit voltage (\( V_{OC} \)), requiring excellent surface passivation of the c-Si wafer. For conventional boron-doped amorphous silicon (a-Si:H(p)) emitter layer, the degradation of passivation properties upon even moderate annealing temperatures has been a limiting factor during post-production manufacturing [7, 8].

In this work, nc-SiO\(_x\):H(p) combined with an intrinsic amorphous silicon (a-Si:H(i)) buffer layer, is presented as thermally superior emitter layer whose passivation properties improve upon annealing temperatures of 293 °C. The beneficial behaviour of the material is attributed to the natural spatial separation of hydrogen and most of the active boron within the nc-SiO\(_x\):H(p) material. Because the boron doping is not in direct vicinity to the Si–H bonds within the material, the Fermi-level-dependent Si–H bond rupture takes place at a much higher temperatures in nc-SiO\(_x\):H(p) than in a-Si:H(p).

Moreover, the influence of i-layer thickness in a-Si:H(i)/nc-SiO\(_x\):H(p) passivation stacks on the minority carrier
lifetime is evaluated. The remarkable result on the characteristics of the interface of a wafer with this passivation stack is that it not only withstands temperatures higher than the deposition temperature of the stack, but even improves upon annealing at such temperatures. This could be of high interest for commercial solar cell producers, as it enables the use of higher post processing temperatures in the production process.

2 Experimental For this study, different samples consisting of thin silicon-based layers deposited on <111> oriented n-type float zone c-Si wafers (thickness ~275 μm, resistivity ~2–5 Ω cm) have been fabricated. To remove the native oxide layer, the wafers were dipped for 2 min in 1% hydrofluoric acid (HF) solution (diluted in de-ionised water) and blow dried with nitrogen (N₂) prior to deposition. All layers were deposited in the PASTA (process equipment for amorphous silicon thin-film applications) parallel plate reactor using radio frequency (13.56 MHz) plasma enhanced chemical vapour deposition (RF-PECVD) [9]. For the deposition of the nc-SiOₓ:H(p) films a gas mixture of silane (SiH₄), hydrogen (H₂), trimethylboron (TMB) and carbon dioxide (CO₂) was used. The deposition conditions and material properties, determined from 185 (±10) nm thick nc-SiOₓ:H(p) layers deposited on Corning borosilicate (Eagle XG) glass, are shown in Table 1. An extensive study of the nc-SiOₓ:H(p) material and its properties [10], as well as the deposition conditions of all amorphous silicon layers [7] have been reported elsewhere.

To confirm the crystallinity of the nc-SiOₓ:H(p) layer with a thickness as actually used in devices, and to illustrate the crystal growth and distribution in the material, a focused Ion Beam made lamella of a stack of a c-Si wafer, 5 nm a-Si:H(i) with a thickness as actually used in devices, and to illustrate for amorphous silicon thin-layers were deposited in the PASTA (process equipment parallel plate reactor using radio frequency (13.56 MHz) plasma enhanced chemical vapour deposition (RF-PECVD) [9]. For the deposition of the nc-SiOₓ:H(p) films a gas mixture of silane (SiH₄), hydrogen (H₂), trimethylboron (TMB) and carbon dioxide (CO₂) was used. The deposition conditions and material properties, determined from 185 (±10) nm thick nc-SiOₓ:H(p) layers deposited on Corning borosilicate (Eagle XG) glass, are shown in Table 1. An extensive study of the nc-SiOₓ:H(p) material and its properties [10], as well as the deposition conditions of all amorphous silicon layers [7] have been reported elsewhere.

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To evaluate the effect of annealing temperature on the minority carrier lifetime, the c-Si wafer was coated on both sides with 5-nm thin a-Si:H(i) layers. On top of these, 20-nm nc-SiOₓ:H(p) layers were deposited on both sides of the wafer. Figure 1 shows the structure of this passivation SJH semi-cell sample. The sample was annealed in consecutive steps of 1 h each in N₂ ambient. After each annealing step, a Sinton WCT120 lifetime tester has been used to investigate the minority carrier lifetime. The values were determined at an injection level of 10¹⁵ cm⁻³ in generalised mode with slowly decaying light pulse for lifetimes below 100 μs and in transient mode with short light pulse for lifetimes above 100 μs [11]. In the second step, the influence of the front side i-layer thickness on the passivation quality in SHJ semi-cells with nc-SiOₓ:H(p) emitter was investigated. For this, samples of SHJ semi-cells with 5 nm a-Si:H(i) and 20 nm a-Si:H(n) layers on the back side and a front side consisting of an i-layer with variable thickness (0–5 nm) and 20 nm nc-SiOₓ:H(p) were fabricated (Fig. 2). The samples were annealed for 16 h in vacuum after the deposition. Again, the minority carrier lifetime after the annealing treatment was evaluated. In addition, the implied VOC is determined from the minority carrier lifetimes at a light intensity of 1 sun.

To investigate the electrical and optical properties after prolonged annealing, layer stacks of 5 nm a-Si:H(i) and 20 nm nc-SiOₓ:H(p) have been grown on Corning borosilicate (Eagle XG) glass. The optical bandgap E₀ and the dark conductivity σD have been determined for one as deposited sample, as well as for one sample after 56 h of annealing in vacuum at 200 °C. For the conductivity measurements, two coplanar silver contacts of 0.5 mm distance and 20 mm length were thermally evaporated on the layer stacks. The measurement was done in vacuum

### Table 1 Deposition conditions and material properties of the nc-SiOₓ(p):H layer (taken from Ref. [10]), with TMB being diluted in H₂ (2% TMB in H₂).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>150 °C</td>
</tr>
<tr>
<td>Pressure</td>
<td>2.57 mbar</td>
</tr>
<tr>
<td>Power density</td>
<td>38 mW cm⁻²</td>
</tr>
<tr>
<td>SiH₄ flow</td>
<td>1.2 sccm</td>
</tr>
<tr>
<td>H₂ flow</td>
<td>200 sccm</td>
</tr>
<tr>
<td>CO₂ flow</td>
<td>1 sccm</td>
</tr>
<tr>
<td>TMB + H₂ flow</td>
<td>0.4 sccm</td>
</tr>
<tr>
<td>Bandgap E₀</td>
<td>2.33 eV</td>
</tr>
<tr>
<td>Dark conductivity σD</td>
<td>7.9 × 10⁻⁴ S cm⁻¹</td>
</tr>
<tr>
<td>Activation energy Eₐ</td>
<td>0.2 eV</td>
</tr>
<tr>
<td>Refractive index n₂</td>
<td>2.7</td>
</tr>
</tbody>
</table>

aTMB is diluted in H₂ (2% TMB in H₂).

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Figure 1 Structure of the passivation samples used to investigate the annealing temperature dependence of the minority carrier lifetime (drawn not to scale).

Figure 2 Structure of the SHJ semi-cells used to investigate the influence of the front side i-layer buffer thickness on the minority carrier lifetime (drawn not to scale).
and $\sigma_d$ was calculated assuming a layer thickness of 20 nm (neglecting any contribution of the much less conductive a-Si:H(i) layer). The optical bandgap $E_{oa}$ of the nc-SiO$_x$:H(p) layer was determined for the same samples by spectrosopic ellipsometry (SE). The measurements were performed using a J.A. Woollam, Inc., M2000 UV ellipsometer. The data were analysed using a Bruggeman effective medium approach model [12].

3 Results and discussion The cross-sectional TEM image in Fig. 3 shows the wafer coated by a 5-nm thick a-Si:H(i) buffer layer followed by the 20-nm nc-SiO$_x$:H(p) emitter layer. Proof of the crystallinity of the thin nc-SiO$_x$:H(p) layer is found. Silicon nanocrystals together with the amorphous silicon oxide matrix (a-SiO$_x$:H) surrounding it form the nc-SiO$_x$:H(p) layer. The desired early nucleation of the nanocrystals and the increasing crystalline fraction with increasing p-layer thickness is clearly visible.

The dependence of the minority carrier lifetime $\tau$ of the passivation stack (Fig. 1) on the annealing temperature $T$ can be seen in Fig. 4. The initial lifetime is rather low. The lifetime of the sample increases with increasing annealing temperature of $T \leq 293^\circ$C and decreases at higher temperatures. The low minority carrier lifetime of 54 $\mu$s for the lowest annealing temperature of 150 $^\circ$C can be attributed to a high amount of defects in the a-Si:H(i) material. The buffer layer is grown at a relatively low temperature of 130 $^\circ$C, which does not provide enough energy for diffusion of the depositing species on the growing surface. This results in a rather disordered and porous material, providing a high amount of dangling bonds at the c-Si surface. These dangling bonds act as recombination centres in the bandgap resulting in a low lifetime. Upon annealing the hydrogen in the a-Si:H(i) becomes mobile and propagates towards the c-Si surface, thus reduces the defect density [7]. These effects are well known and studied for a-Si:H(i)/c-Si/a-Si:H(i) passivation samples without doped layers.

However, for an i/p-layer sample the observed behaviour is exceptional. It is remarkable that annealing temperatures well above the deposition temperature have a positive effect. To our knowledge it has not been reported earlier that annealing of complete passivation stacks including p-type silicon-based layers can improve upon annealing at such high temperatures. The decrease of minority carrier lifetime at comparably high temperature of $T = 293^\circ$C is in sharp contrast to the behaviour known from samples that include a-Si:H(p) layers. De Wolf et al. fabricated a-Si:H(i)/a-Si:H(p) stacks whose annealing properties degrade at temperatures above 220 $^\circ$C [8]. Schüttauf et al. found that the passivation of a-Si:H(i)/a-Si:H(p) stacks deteriorates upon annealing at temperatures as low as 150 $^\circ$C [7]. The Fermi level dependent rupture of Si–H bonds takes place at lower temperatures in the a-Si:H(p) layer compared to the a-Si:H(i) layer. By thermal annealing Si–H bonds are ruptured and $H_2$ is formed which consecutively effuses from the layer [13]. This leads to an unfavourable hydrogen gradient within the amorphous silicon layers. Hydrogen within the a-Si:H(i) layer becomes mobile during annealing and relocates from the intrinsic to the hydrogen-deficient boron-doped layer. Thereby, the c-Si/a-Si:H(i) interface becomes depleted from hydrogen, resulting in a decrease of passivation [7].

For the a-Si:H(i)/nc-SiO$_x$:H(p) layer stack however, this behaviour does not take place. We assume a high fraction of the active boron (fourfold coordinated) to be located in the silicon nanocrystals, whereas the inactive boron (threefold coordinated) is mostly located in the amorphous silicon oxide (a-SiO$_x$:H) domain of the layer [14]. The concentration of active boron in this amorphous phase is expected to be much lower compared to typical a-Si:H(p). Thus, the Fermi level of the amorphous domain within the nc-SiO$_x$:H(p) layer will be closer to mid gap. Because hydrogen solubility in crystalline silicon is very low, most of the hydrogen is expected to be located in the a-SiO$_x$:H matrix, thus in the domains where the Fermi level is comparably far from the band edge. Therefore, the Fermi level dependent Si–H bond rupture, and thus the $H_2$ effusion, will take place at much higher temperatures.
temperatures in nc-SiO$_2$:H(p) compared to the a-Si:H(p) layer.

Studies by Beyer indicate that for a-SiO$_2$:H at low-oxygen concentration (<20%) the hydrogen effusion is smaller and the effusion peak shifts to higher temperature compared to pure a-Si:H [15]. Hence, we do not expect any significant increase of hydrogen diffusion/effusion in the a-SiO$_2$:H matrix due to the oxygen content in the material.

Hydrogen effusion from a-Si:H(i) and a-SiO$_2$:H(i) passivation layers upon annealing has also been investigated by Nakada et al. [16]. They attribute hydrogen effusion in these layers to the combination of two phenomena. On one hand, molecular H$_2$ can effuse from internal surfaces and out-diffuse through interconnected voids. In case of a less void-rich material, this H$_2$ out-diffusion is hindered and the effusion peak shifted towards higher temperatures. In addition, atomic H can effuse through the network and recombine at the surface of the layer to H$_2$ and thereby also effuse from the layer. This second mechanism benefits from a high amount of isolated voids in a dense material. In case of a more compact material this atomic hydrogen diffusion is hindered and the effusion peak shift towards higher temperatures. Especially notable, for a-SiO$_2$:H this peak also shifts towards higher temperatures compared to a-Si:H. This is caused by a stronger Si–H bond due to the higher electronegativity of O atoms backbonded to the Si–H [16]. We expect similar behaviour in nc-SiO$_2$:H(p).

In the second step, the intrinsic buffer layer thickness was investigated. It has been shown that nc-SiO$_2$:H(p) material grown with large CO$_2$/SiH$_4$ ratios exhibit poor passivation quality [17]. Moreover, epitaxial growth, as well as the formation of crystallites near the a-Si/c-Si interface, results in a high amount of unpassivated dangling bonds at the interface [18, 19]. Therefore, the nc-SiO$_2$:H(p) layer should not be grown directly on top of the c-Si wafer. A certain buffer i-layer thickness is essential to guarantee a good passivation quality. On the other hand, the buffer layer also needs to be reasonably thin to limit the parasitic absorption of light [20]. To evaluate the influence of the i-layer thickness in our particular layer stack, SHJ semi-cells with variable front buffer layer thicknesses from 0 (no layer) to 5 nm have been fabricated in steps of 1 nm (Fig. 2) and annealed for 16 h at 200 °C in vacuum to improve passivation properties. Instead of 293 °C, which has been proven to be most beneficial annealing temperature for passivation properties of this layer stack, the temperature of 200 °C was chosen in order to be able to compare our result with those obtained with standard a-Si:H passivation and p-type a-Si:H layers.

Figure 5 shows the dependence of the minority carrier lifetime $\tau$ on the i-layer thickness $d$. A strong dependence is visible, the expected gain in minority carrier lifetime with increasing i-layer thickness can be observed. As predicted, the sample with nc-SiO$_2$:H(p) grown directly on the wafer shows an extremely poor lifetime of 54 $\mu$s. Acceptable lifetimes of 1144 and 1460 $\mu$s are achieved for layer stacks with 4 and 5 nm a-Si:H(i), respectively. The implied $V_{oc}$ at 1 sun light intensity of the samples is depicted in Fig. 6. A rise of $V_{oc}$ with increasing i-layer thickness can be observed. This dependence illustrates the improvement of c-Si interface passivation for thicker i-layer.

In addition to the beneficial annealing behaviour up to high temperatures of 293 °C, the wide bandgap nc-SiO$_2$:H(p) layer has an increased transparency compared to conventional a-Si:H(p) emitter layer, thus enabling an increased amount of light to enter the active absorber layer of the cell [10]. Moreover, it is known that SHJ solar cells with amorphous silicon oxide replacing conventional amorphous silicon buffer layer show a more favourable temperature coefficient of performance and thus better operation under increased temperatures than conventional SHJ solar cells [21]. A similar effect is expected for replacing the conventional a-Si:H(i) buffer layer by nc-SiO$_2$:H(p).

To assure good optical and electrical properties of the nc-SiO$_2$:H(p) layer upon implementation in SHJ solar cells, these properties have been investigated before and after annealing. As can be seen in Fig. 3, the first few nanometres of the nc-SiO$_2$:H(p) material consists of an amorphous incubation phase. With increasing layer thickness the crystallinity of the material increases. It is known that an amorphous silicon starting surface will result in a thicker
incubation layer than an oxide material, such as borosilicate glass [14]. In order to mimic the growth conditions and material properties of the nc-SiO$_2$:H(p) material in a solar cell, 20-nm thick nc-SiO$_2$:H(p) was grown on Corning borosilicate (Eagle XG) glass precoated with a 5 nm a-Si:H(i) layer. The dark conductivity $\sigma_D$ was calculated in the as deposited state and after 56 h annealing in vacuum at 200 °C. This long annealing time was chosen in order to assure any notable effect on the material properties.

We observed an increase in $\sigma_D$ from $1.3 \times 10^{-7}$ to $2.6 \times 10^{-6}$ S cm$^{-1}$ after annealing. This gain in conductivity is attributed to the activation of boron upon annealing [14]. Due to the amorphous seed material and a layer thickness of only 20 nm, the layer is expected to be less crystalline and thus less conductive than the 185 nm thick layer. Therefore, we consider the difference in values of the band gap before and after annealing to use metallisation paste with higher curing temperatures leading to better metal grid conductivity and lower contact resistivity.

4 Summary We have presented a nc-SiO$_2$:H(p) material with superior thermal behaviour. A-Si:H(i)/nc-SiO$_2$:H(p) passivation stacks exhibit an increase in minority carrier lifetime after annealing at relatively high temperatures up to 293 °C. This outstanding behaviour is mostly attributed to the hydrogen bonds predominantly in the amorphous SiO$_2$ phase where the Fermi energy is deep in the gap. Thereby, the Fermi level dependent Si–H bond rupture takes place at higher temperatures than for conventional a-Si:H(p). This temperature-withstanding emitter/passivation layer stack opens up opportunities, for instance, to use metallisation paste with higher curing temperatures leading to better metal grid conductivity and lower contact resistivity.

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