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A Low-Power Highly Digitized Receiver for 2.4-GHz-Band GFSK Applications

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***Abstract*—This paper describes the design and measurement results of a low-power highly digitized receiver for Gaussian frequency-shift keying modulated input signals at 2.4 GHz. The RF front-end has been based on a low-IF architecture and does not require any variable gain or filtering blocks. The full dynamic range of the low-IF signal is converted into the digital domain by a low-power high-resolution time-continuous $\Sigma\Delta$ analog-to-digital converter (ADC). This leads to a linear receive chain without limiters. A fifth-order poly-phase loop filter is used in the complex $\Sigma\Delta$ ADC. The digital block performs filtering and demodulation. Channel filtering is combined with matched filtering and the suppression of noise resulting from the $\Sigma\Delta$ ADC. The high degree of digitization leads to design flexibility with respect to changing standards and scalability in future CMOS generations. The receiver has been realized in a standard 0.18-μm CMOS process and measures 3.5 mm^2. The only external components are an antenna filter and a crystal. The power consumption is only 32 mW in the continuous mode, which is at least a factor of two lower than state-of-the-art CMOS receivers.**

***Index Terms*—CMOS integrated circuits (ICs), demodulation, digital signal processors, sigma–delta modulation, UHF receivers.**

I. Introduction

SEVERAL standards for low-cost short-distance wireless systems are emerging, such as Bluetooth, IEEE802.11x, and Zigbee. In addition to low cost, low power is also important for the portable devices implementing these standards. Low cost is achieved by minimizing the number of external components for the transceiver integrated circuit (IC) and by using a standard baseline IC process technology. The size of the digital hardware, forming a considerable part of the transceiver IC, scales down for newer CMOS generations. Therefore, full integration in CMOS becomes interesting.

Low power is influenced by the chosen architecture. Architectures using limiters are commonly considered for low power, but lack flexibility. As the available bandwidth is limited, new standards for higher data rates will require the use of nonconstant envelope modulation techniques. A highly digitized architecture offers flexibility at low power.

Several transceivers realized in CMOS and aimed at Bluetooth/Gaussian frequency-shift keying (GFSK) applications have been reported in the literature [1]–[5]. Most referenced transceivers have been realized in 0.18-μm CMOS, whereas the Bluetooth receiver revealed in [5] has been realized in 0.13-μm CMOS. All cited references report power consumptions for the receiver part of over 60 mW. Most receiver architectures use a limiter, after which demodulation takes place based on zero-crossing detection [1], [3], [4]. Although suitable for GFSK applications, the disadvantage of such nonlinear receivers is that the concept is not applicable to nonconstant envelope modulation.

The concept presented in [2] uses a linear receiver, where digitization of the IF signal is performed using a variable-gain amplifier (VGA), an eighth-order filter, and a 6-bit ADC. This enables digital demodulation, but this has not been included in the presented silicon. The receiver architecture presented in [5] is also linear and performs demodulation in the digital domain. Discrete-time analog signal processing is applied at the input involving RF sampling with an all-digital phase-locked loop (PLL) using a digitally controlled oscillator. A considerable amount of filtering and variable-gain control occurs in the signal path before the analog-to-digital converter (ADC). The Bluetooth specifications are met with a considerable margin, but the power consumption is still relatively high.

The receiver architecture presented in this paper aims at a high level of integration, low power consumption, and a high degree of digitization [6]. Removing all analog filtering and VGA in the front-end significantly reduces the design complexity and power consumption of the RF part. Instead, channel filtering and demodulation take place in the digital domain with the advantages of flexibility with respect to changing standards and lower power consumption and chip area for newer CMOS generations. Moreover, the receiver chain is linear, which enables using the same architecture for future systems with nonconstant envelope modulation. The concept does place tough requirements on the design of the ADC.

In order to verify our concept, an IC has been designed in 0.18-μm CMOS for applications in the 2.4-GHz industrial–scientific–medical (ISM) band with GFSK-modulated input signals. Specifications have been derived from the Bluetooth standard. The architecture is described in Section II. Section III highlights important design issues of the analog front-end and Section IV describes the design of the digital filter and demodulator. Top-level design issues are described in Section V and measurement results are discussed in Section VI. Finally, conclusions are drawn in Section VII.

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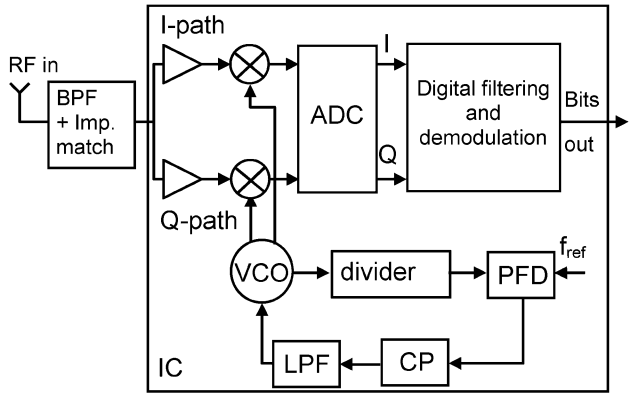

Fig. 1. Simplified block diagram of the receiver.

II. Receiver Architecture

A. Block Diagram

A simplified block diagram of the receiver is shown in Fig. 1. An external bandpass filter (BPF) selects the 2.4-GHz band and performs impedance matching. Two matched low-noise amplifiers (LNAs) are used in parallel to provide sufficient isolation between the in-phase (I) and quadrature (Q) channels after the mixers. The LNAs have been implemented as *V–I* converters. The RF output current is down-converted to a low IF of 500 kHz by passive mixers, driven directly by a quadrature voltage-controlled oscillator (VCO) in a PLL. A high-resolution complex $\Sigma\Delta$ ADC converts the quadrature IF currents into noise-shaped I and Q bit streams. The digital block performs channel and decimation filtering, as well as demodulation.

B. Derivation of the Main Specifications

The noise figure (NF) of the analog front-end has been based on the -70-dBm sensitivity specification in 1-MHz bandwidth of the Bluetooth standard. The thermal noise power in 1-MHz bandwidth at the receiver input equals kTB or -114 dBm with $B = 1$ MHz, assuming a perfect match between antenna impedance and LNA input impedance. A signal-to-noise ratio (SNR) of 18 dB is needed at the demodulator input to properly demodulate an input signal with a bit error rate (BER) of 0.1%. Taking into account a 2-dB margin, the NF of the analog front-end must be less than 24 dB.

When the noise of the RF front-end is made dominant, the design of the ADC becomes very difficult and vice versa. Therefore, equal noise contributions of the RF front-end and the ADC have been adopted as a best compromise with respect to design complexity of the RF front-end and ADC. This leads to an NF requirement for the RF front-end of 21 dB, which should be relatively easy to achieve. With a maximum input power of -20 dBm based on Bluetooth, the required dynamic range (DR) of the ADC becomes 73 dB. The linearity and interference specifications of the front-end have also been based on Bluetooth. This implies a specified third-order input-referred interception point (IIP3) of -21 dBm.

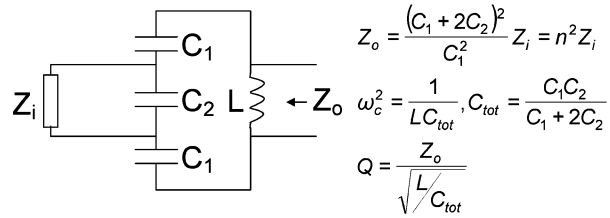

Fig. 2. Schematic and basic design equations for the BPF/impedance-matching network.

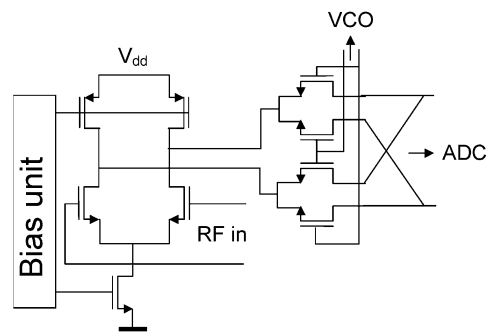

Fig. 3. Circuit schematic of the LNA/mixer combination.

III. Design of the Analog Front-End

A. BPF/Impedance-Matching Network

The schematic and basic design equations of the BPF/impedance-matching network are shown in Fig. 2. The filter comprises an *LC* tank tuned to the Bluetooth band from 2.4 to 2.5 GHz with capacitive tapping to achieve voltage multiplication and impedance matching. The filter has been designed such that the differential antenna impedance of 150 Ω (Z_i), seen at the output of the filter (Z_o), matches the LNA input impedance of 1350 Ω. For the current version of the IC, an external filter has been used with $C_1 = C_2 = 3.3$ pF and $L = 4.2$ nH at 2.4 GHz. The approach has been chosen to be able to integrate this filter, enabling tuning by adding switchable MOS capacitors to the circuit. However, this has not yet been implemented on the current version of the IC.

B. LNA/Mixer Combination

A circuit schematic of the LNA/mixer combination is shown in Fig. 3. The LNA is a simple differential pair providing voltage-to-current conversion. The ADC has been designed such that it can handle the entire DR. Therefore, the LNA just acts as a buffer and driver toward the mixer. The receive chain has been dimensioned such that for a maximum input signal of -20 dBm at the antenna, the differential output current of the LNA/mixer combination is 50 μA_{peak}. This is achieved with a transconductance for the LNA of 0.6 mA/V. When this full-scale (FS) input current is applied to the ADC, a digital output signal corresponding to digital FS minus 3 dB results, i.e., a bit stream of all ones.

The LNA should also provide isolation between the I and Q paths. This can be obtained by using cascode techniques, leading to a reduced output voltage range. We have chosen to use two LNAs, leading to optimum isolation at the cost of higher power consumption. However, as the LNAs have been designed

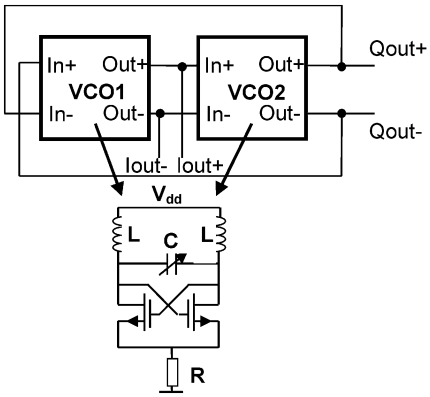

Fig. 4. Block diagram of the quadrature VCO and circuit schematic of the oscillator core.

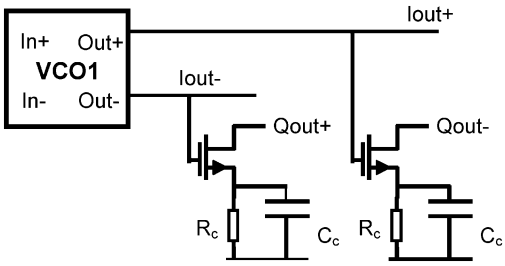

Fig. 5. Placing an additional zero (90° phase shift) in the couplings of the I and Q paths in Fig. 4. A similar technique is needed for VCO2.

to function at much lower power than the other front-end blocks, this becomes less of an issue.

Passive mixers are used at a common-mode voltage of 0.8 V and a nonoverlapping clock scheme has been implemented in order to reduce distortion and noise. Therefore, the dc level of the VCO output that is directly driving the mixer has been set to 1.4 V, i.e., at least a threshold voltage above the common-mode voltage.

C. VCO and PLL

The VCO has been designed to provide a large output voltage swing of 1 V_{pp} differential to enable direct drive of the mixers. A quadrature VCO has been realized by cross-coupling two identical oscillator cores, as indicated in Fig. 4 [7]. The tank circuit in each core has been built up around two inductors of 2.2 nH each with a measured quality factor Q of 10 at 2.45 GHz and with a resonance frequency of 9 GHz. The tunable capacitance has been realized with two identical nMOS devices.

VCO2 is connected to VCO1 in antiphase in Fig. 4, while VCO1 is connected to VCO2 in common phase. This implies a 180° phase shift from the VCO2 output to the VCO1 input, forcing a 90° phase shift in each core, where a 0° phase shift is preferable for optimum phase-noise performance. Therefore, an additional zero has been introduced in each coupling in the form of a common-source amplifier with a capacitor C_c, introducing a 90° phase shift between gate voltage and drain current (see Fig. 5) [7]. This brings the oscillator-core phase shift back to the optimum value of zero. A similar coupling is used to connect VCO2 to VCO1.

Analog tuning with the tunable capacitance results in 200 MHz or 8% tuning range. This is enough to cover the

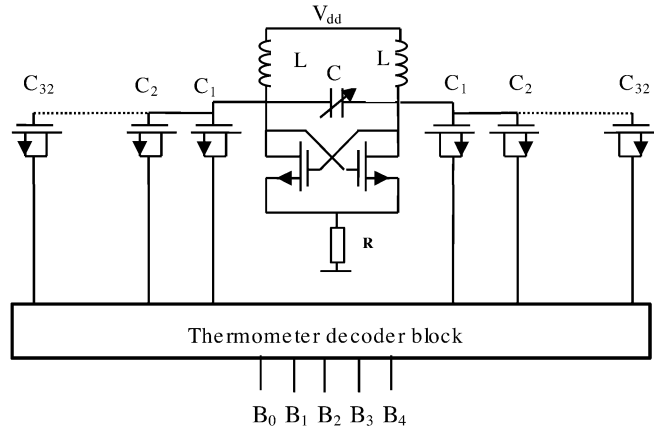

Fig. 6. Use of two 32-MOS capacitor banks to enable digital tuning of the VCO center frequency to deal with process spread.

Bluetooth band, but not enough to cover process spread as well. Increasing the analog tuning range to cover process spread is not preferable since it leads to a higher VCO gain in the PLL loop and, hence, increased sensitivity to noise on the VCO tuning input. Therefore, digital tuning using a 32-MOS capacitor bank on each side of each core is used to cope with process spread. This is indicated in Fig. 6. The individual capacitors are turned ON or OFF by applying a control voltage of either zero or the supply voltage to the drain/source connections of the MOSFETs using a 5-bit digital-code word and a thermometer decoder block. The digital tuning is used to set the VCO to the proper center frequency at startup.

The VCO has been included in a PLL using a multimodulus divider and a reference frequency of 500 kHz derived from a 64-MHz clock signal generated by an on-chip third-overtone crystal oscillator [7]. Analog tuning is applied in a synthesizer loop (PLL) to lock the VCO at various channel frequencies. Combined analog and digital tuning leads to a measured total tuning range of 400 MHz or 16%.

The phase noise at 3 MHz offset has been measured at −120 dBc/Hz. For digital code word 15, i.e., halfway the digital tuning range, the Bluetooth band is completely covered by the analog tuning range of the PLL [7].

D. Continuous-Time $\Sigma\Delta$ ADC

No analog filters or VGA are present in the architecture of Fig. 1. By consequence, the ADC needs to handle the entire signal DR and must be immune to interferer channels over the entire Bluetooth band. The signal bandwidth from 0 to 1 MHz can, in principle, be converted into the digital domain using two identical low-pass $\Sigma\Delta$ ADCs processing the I and Q channels separately. The transfer function of both ADCs is symmetrical with respect to dc in this case, leading to the same resolution as from 0 Hz to 1 MHz being available from −1 MHz to 0 Hz. Since this is not necessary, we have chosen to use a single complex $\Sigma\Delta$ ADC with quadrature inputs and outputs with a poly-phase loop filter [8].

The fifth-order poly-phase loop filter has been implemented in continuous time, which is advantageous for low power consumption and provides inherent antialiasing filtering. The five notches of this filter can only be placed in the band from 0 to

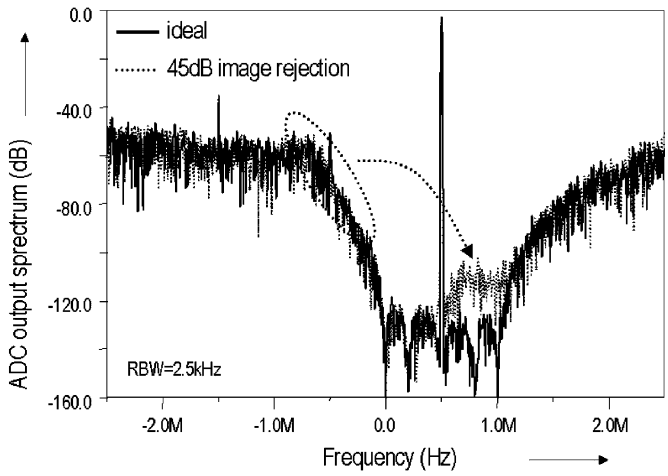

Fig. 7. Simulated effect on the ADC output spectrum of limited image rejection due to mismatch between the quadrature parts of the $\Sigma\Delta$ ADC.

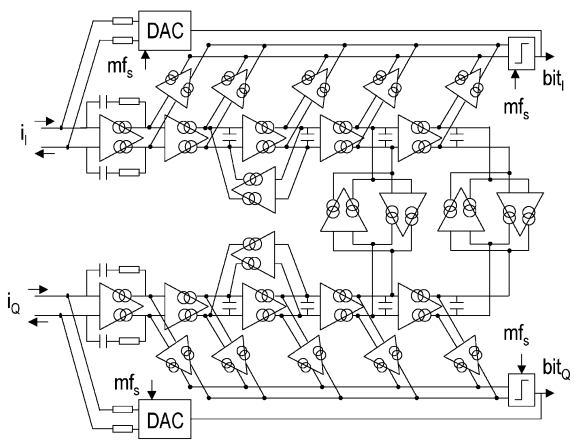

Fig. 8. Block diagram of the fifth-order complex continuous-time $\Sigma\Delta$ ADC.

1 MHz. As the converted bandwidth is halved compared to two real $\Sigma\Delta$ ADCs, the effective over-sampling is doubled and efficient bandpass noise shaping around the IF frequency occurs. However, mismatch between the quadrature parts of the ADC will lead to leakage of quantization noise from negative frequencies to the wanted band and, hence, to degradation of the SNR. This is illustrated in Fig. 7, showing the effect of limited image rejection on the simulated output spectrum of a fifth-order $\Sigma\Delta$ ADC. Therefore, one filter notch has been placed at the edge of the image band from -1 MHz to 0 Hz; the remaining four notches being placed in the wanted signal band from 0 to 1 MHz [8]. A detailed discussion on interferer immunity of continuous-time $\Sigma\Delta$ ADCs and further improvements thereof can be found in [9].

The block diagram of the complex fifth-order $\Sigma\Delta$ ADC is shown in Fig. 8 [8]. Feed-forward branches are used in the loop filter to ensure stability and to ensure graceful degradation in case large input signals are applied. A sampling frequency of 64 MHz is used, leading to a theoretical maximum SNR of 90 dB. The on-chip third-overtone crystal oscillator generates the 64-MHz clock signal.

For sufficient linearity of the overall receiver chain, the input impedance of the ADC needs to be low compared to the output impedance of the RF front-end. As can be seen in Fig. 8, an

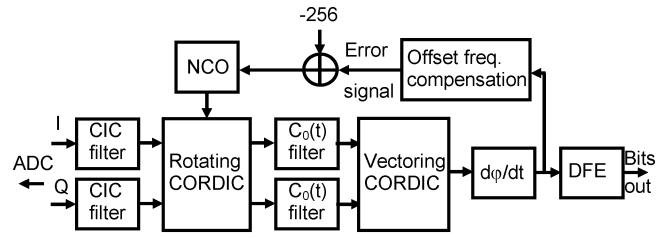

Fig. 9. Block diagram of the digital filter and demodulator.

operational transconductance amplifier in integrating feedback configuration determines the input impedance of the ADC. This provides a virtual-ground summing node, which makes the ADC itself highly linear, preventing intermodulation of interferers from decreasing the resolution in the wanted channel. Moreover, it provides the desired low-ohmic termination of the RF front-end. The differential input impedance is below 400 Ω over the entire Bluetooth band. This specification sets the current consumption of the input stage and dominates the overall consumption. As a consequence, instead of the input stage, the resistive DAC used in the feedback path of the $\Sigma\Delta$ ADC and the second integrator limit the SNR to 79 dB due to thermal noise. A further 3-dB reduction in SNR results from white noise induced by the 7-ps$_{\rm rms}$ timing jitter present on the 64-MHz clock. This results in a fair distribution of power consumption between crystal oscillator and ADC.

The measured performance of the standalone $\Sigma\Delta$ ADC includes a DR of 76 dB and a third-order intermodulation (IM3) distortion below -82 dBc. Applying an FS input signal with a frequency near that of the 64-MHz clock signal causes a folding component in the signal band at -77 dB, which illustrates the antialiasing behavior of the ADC [8].

IV. Digital Filter and Demodulator

A block diagram of the digital filter and demodulator is shown in Fig. 9. The I and Q output bit streams from the ADC are clocked in at 64 MHz. After filtering and decimation in the cascaded integrator-comb (CIC) filters, the clock frequency in the remainder of the block is 8 MHz.

CIC filters have been introduced in [10]. These filters offer good performance and are relatively easy to implement in a short design time. The structure consists of R integrator stages in series, followed by a decimation down-sampling of the signal by a factor of N, followed by R differentiation stages in series. The transfer function of this filter is given by

$$H(z) = \frac{(1-z^{-N})^R}{(1-z^{-1})^R} = \left(\sum_{k=0}^{N-1} z^{-k}\right)^R \tag{1}$$

where $N = 8$ and $R = 6$ have been chosen in the design. These parameters have been chosen such that a reasonable over-sampling factor of eight of the signal is maintained, a high suppression of the aliasing frequency is achieved, and the deformation of the passband remains small.

The rotating coordinate rotation digital computing (CORDIC) rotates the complex input signal composed of an I and Q data stream by a given angle φ, which is provided by the phase input signal [11]. Elementary rotations are combined,

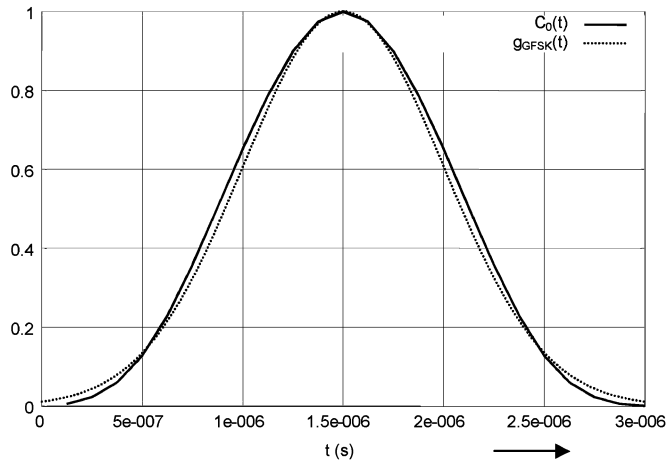

Fig. 10. Comparison of $C_0(t)$ and $g_{\mathrm{GFSK}}(t)$ impulse responses.

each of them realizing a different elementary rotation angle, to realize different rotation angles φ. This leads to a simple implementation only based on additions and subtractions. The rotating CORDIC shifts the IF frequency of the output signals of the CIC filters from 500 kHz to 0 Hz.

The complex GFSK baseband signal present at the output of the rotating CORDIC is represented by

$$s(t) = \exp\left(j \cdot 2\pi \cdot \Delta f \cdot \varphi_{\mathrm{GFSK}}(t)\right) \tag{2}$$

where the instantaneous phase $\varphi_{\mathrm{GFSK}}(t)$ is given by

$$\varphi_{\mathrm{GFSK}}(t) = \int_0^t \sum_{i=0}^{\infty} d(i) \cdot g_{\mathrm{GFSK}}(\xi - iT) d\xi \tag{3}$$

with Δf denoting the frequency swing of the GFSK-modulated signal ($\Delta f = \eta/(2T)$ with η the modulation index and T the symbol period time), $d(i)$ denoting the data bits (part of the set $\{-1, +1\}$) and $g_{\mathrm{GFSK}}(t)$ expressing the impulse response of the combined impulse-shaping and Gaussian filter used to shape the data bits before modulation. It can be proven that this nonlinear representation of the complex GFSK-modulated baseband signal can be rewritten as a series expansion containing a finite number of time-limited amplitude-modulated pulses $C_i(t)$ [12]. Moreover, the signal can be approximated with good accuracy using only the main impulse response $C_0(t)$. The result is a linear approximation of the complex GFSK-modulated signal given by

$$s(t) \approx \sum_{i=0}^{\infty} \left(\exp\left(j\pi\eta \sum_{l=0}^{i} d(l) \right) C_0\left(t - iT\right) \right). \tag{4}$$

Using a filter matched to $C_0(t)$ leads to optimum suppression of white noise [13]. Fig. 10 shows that the impulse response $C_0(t)$ is very similar to a pure Gaussian impulse response $g_{\mathrm{GFSK}}(t)$. The $C_0(t)$ impulse response is only weakly dependent on the modulation index η. The advantage of using a matched filter defined by impulse response $C_0(t)$ is that it leads to a simpler implementation since a Gaussian filter would have a somewhat longer impulse response.

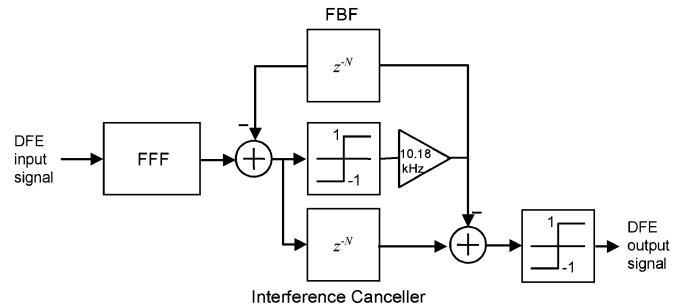

Fig. 11. Block schematic of the DFE.

The vectorizing CORDIC calculates the phase φ of the complex signal represented by a Cartesian vector. The CORDIC rotates the given vector in several steps until it meets the x-axis. Elementary rotations are used in a similar way as for the rotating CORDIC. As the receive chain is linear, the vectorizing CORDIC can also be used to determine the amplitude of the signal as a future extension to deal with other modulation techniques. Phase differentiation $(d\varphi/dt)$ takes place at the output of the vectorizing CORDIC to obtain the instantaneous frequency. The combination of the vectorizing CORDIC and phase differentiation forms a frequency modulation (FM) demodulator.

A decision-feedback equalizer (DFE) yields an output bit stream that is eight times over-sampled compared to a 1-Mb/s symbol rate. The DFE is a nonlinear equalizer, which gives better performance in terms of the BER compared to a linear equalizer at only slightly increased complexity [13]. A block diagram of the DFE is shown in Fig. 11. Compared to a standard DFE with a three-tap feed-forward filter (FFF) and a 1-tap feed-back filter (FBF), an additional interference canceller has been added. This leads to a further improvement of the BER performance since only using a standard DFE with optimized coefficient settings for the FFF and FBF does not fully suppress precursive inter-symbol interference (ISI).

The implemented three-tap FFF is a finite impulse response (FIR) filter. The input signal of the DFE is an instantaneous frequency. Since the output of the slicer drawn in the middle of Fig. 11 is either 1 or -1, it needs to be translated back into a frequency value. Therefore, the outcome of this slicer is multiplied by 10.18 kHz, the value of which has been obtained from simulations in order to optimize the BER performance of the demodulator. A slicer is also used at the DFE output to obtain the original data bits.

Due to differences in crystal frequencies of transmitters and receivers in, for example, a Bluetooth system, a frequency offset will be present in the signal that has to be demodulated. This leads to a dc shift in the differentiator output. Therefore, a frequency-compensation loop including first-order filtering is used. The loop error signal is added to the default frequency shift of -256, i.e., the digital representation of the IF frequency of 500 kHz, and then fed to a numerically controlled oscillator (NCO). This leads to a shift to 0 Hz of the incoming signal by the rotating CORDIC, even in the presence of an offset frequency. The system has been designed to deal with frequency offsets up to ± 150 kHz.

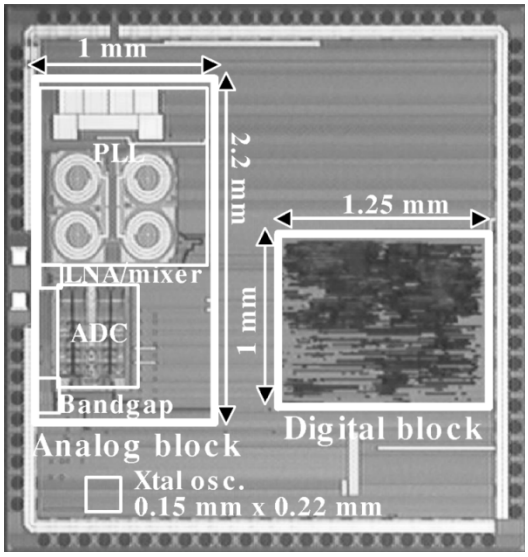

Fig. 12. Die photograph of the receiver test IC.

V. Design of the Complete IC

The receive chain has been realized in a six-metal-layer 0.18-μm standard CMOS process on a 10-$\Omega \cdot$cm substrate. The die photograph in Fig. 12 shows a core area of 3.5 mm^2.

The IC has been packaged in a 48-pin low-profile quad flat package (LQFP) plastic package and mounted on an FR-4 board. Apart from supply decoupling capacitances, the only external components needed are an antenna filter/impedance-matching network and a 64-MHz crystal.

Several measures have been taken to deal with crosstalk between the digital and analog blocks. The complete analog front-end has been implemented differentially and many substrate contacts connected to a clean analog ground have been used. The pad ring has been cut at two places yielding an analog and a digital pad ring. Finally, a guard ring connected to the positive digital supply voltage has been laid out around the digital block to minimize any generated substrate noise.

As an additional means to investigate crosstalk from the digital block to the analog block substrate contacts ("sensors") have been placed at various locations on the IC and connected to dedicated pads. The same die will also be used in the future to experiment with wafer-scale packaging techniques [14]. An advantage of wafer-scale packaging is the small size of the package, i.e., roughly 3 mm $\times$ 3 mm, as opposed to the size of the LQFP48 package of 7 mm$\times$7 mm. Moreover, the possibility exists to etch a trench between analog and digital. Substrate "sensors" have been placed on either side of the future trench. This will enable determination of the additional suppression due to the trench of noise generated by the digital block as perceived on the analog side of the IC.

VI. Measurement Results

The measured power consumptions of the various blocks in the receiver chain are listed in Table I. The supply voltage for the analog part is 1.8 V, whereas the digital supply voltage is 1.4 V. The total power consumption is 31.7 mW in continuous mode.

TABLE I
Measured Power Consumption of Receiver Blocks

Block	Power consumption
2xLNA	2x0.3 mAx1.8 V=1.1 mW
PLL	7.6 mAx1.8 V=13.7 mW
ADC	2.3 mAx1.8 V=4.1 mW
Bandgap	0.1 mAx1.8 V=0.2 mW
Crystal oscillator	1.2 mAx1.8 V=2.2 mW
Digital filter+demodulator	7.4 mAx1.4 V=10.4 mW
Total (analog+digital)	31.7 mW

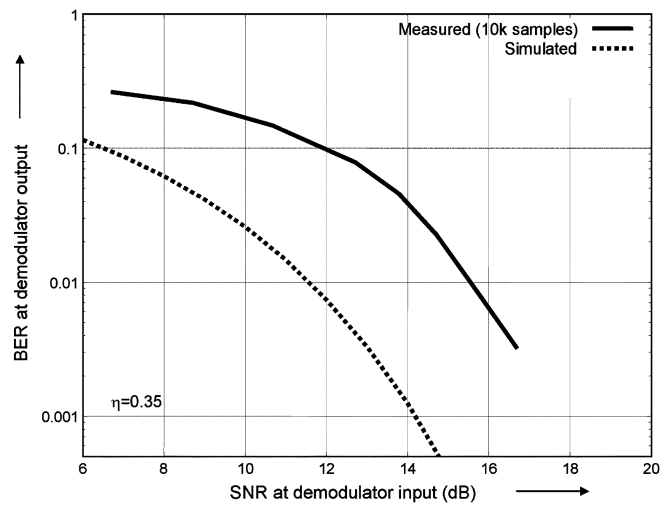

Fig. 13. Measured and simulated BER curves versus SNR at the demodulator input. Simulations have been based on an ideal front-end and AWGN channel.

This is at least a factor of two lower than for other reported CMOS receivers with identical functionality [1]–[5].

The measured and simulated behavior of the demodulator are compared in Fig. 13 by plotting the SNR at the demodulator input versus the achieved BER at the demodulator output based on a modulation index η of 0.35. The number of samples used in the measurements is 10K. The simulations have been performed with an ideal receiver front-end model for the additive white Gaussian noise (AWGN) channel. The difference in SNR for $\mathrm{BER} = 0.001$ (0.1%) is roughly 3 dB, which can be found by extrapolating the measured line. This is caused by nonidealities in the real receiver chain compared to the simple ideal model, e.g., the effect of limited rolloff of the CIC filters that has not been considered in the ideal model used in the simulations.

The behavior of the digital demodulator is illustrated in Fig. 14 for Bluetooth channels 0, 48, and 78. Similar behavior occurs for all channels as expected, leading to an extrapolated SNR for which $\mathrm{BER} = 0.001$ of 17 dB. Fig. 15 shows the BER curve versus RF input power for channel 0. Measurements obtained for 10K and 300K samples have been combined to extend the BER curves to values below 0.001. The RF input power corresponding to an SNR of 17 dB at the output of the ADC and a BER of 0.001, i.e., the sensitivity level, is -71 dBm. The measured DR of the ADC was found to be 76 dB [8]. This leads to an NF of the RF front-end of 25 dB, which is higher than the designed value due to matching problems at the RF input. Modeling inaccuracies at the time of designing the RF input circuits have caused these problems. This will be addressed by

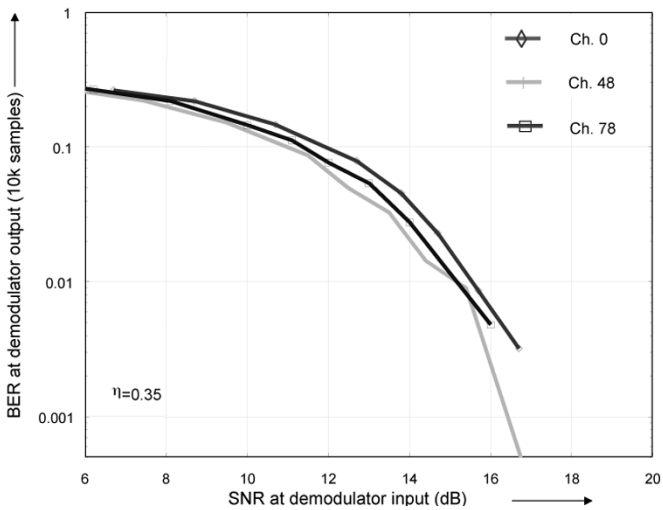

Fig. 14. Measured BER curves versus SNR at the demodulator input for Bluetooth channels 0, 48, and 78.

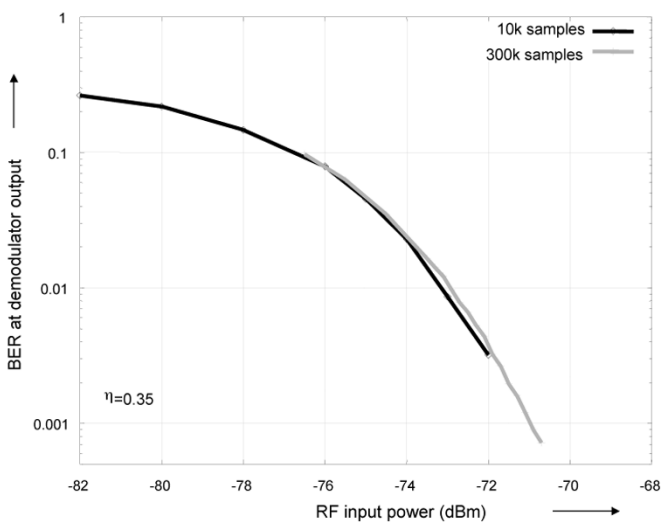

Fig. 15. Measured BER curve versus RF input power using 10K and 300K samples (channel 0).

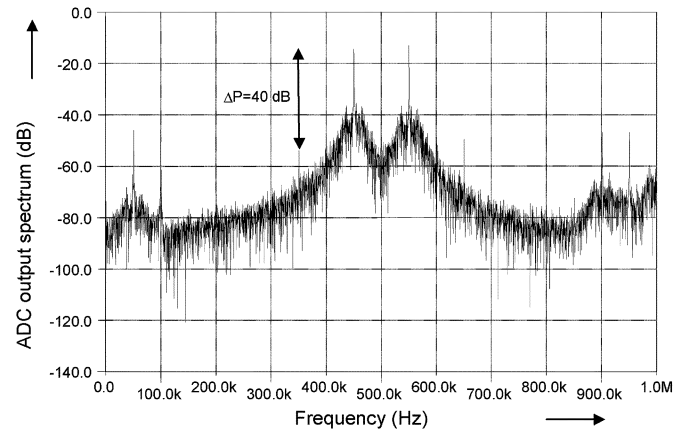

Fig. 16. Measured ADC output spectrum for two-tone experiment with −30-dBm input power (channel 48).

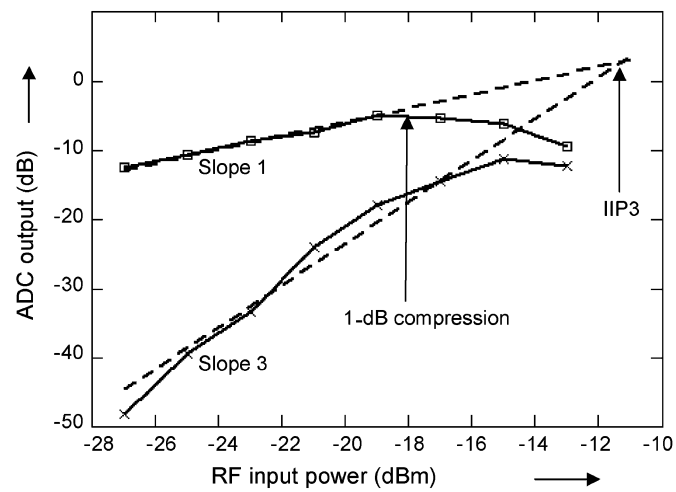

Fig. 17. Measured linearity of the receiver chain based on extrapolation of fundamental (slope 1) and IM3 powers (slope 3) (channel 0).

a redesign of the input circuits using proper models, including the design of an integrated and tunable version of the antenna filter. For the current realization, the maximum input power has been determined at −19 dBm. This leads to a signal range of the receiver chain of 52 dB across the entire band.

The linearity of the receiver chain has been determined by offering two tones separated 100 kHz apart in the band of interest. The measured output spectrum of the ADC for a two-tone experiment in channel 48 is depicted in Fig. 16. The fundamental tones at 450 and 550 kHz and the IM3 products at 350 and 650 kHz can be clearly recognized. The RF input powers of the two tones have been installed at $P_{\text{in}} = -30$ dBm. An IIP3 value of −10 dBm can be calculated from the spectrum using $\text{IIP3} = P_{\text{in}} + \Delta P/2$ [15]. An alternative method to assess the IIP3 is by extrapolation [15]. The result is shown in Fig. 17 for channel 0, revealing an IIP3 value of −11 dBm and a 1-dB compression point of roughly −18 dBm.

Additional linearity measurements have been performed according to the Bluetooth specification. A GFSK-modulated signal has been applied at −64 dBm in the wanted channel at frequency f_0. A static sine wave has been applied at a power level of −39 dBm and frequency f_1, whereas a GFSK-modulated signal with random data has been applied at a power level of −39 dBm at frequency f_2. The relations between these frequencies are given by $f_0 = 2f_1 - f_2$ and $|f_1 - f_2| = 3$ MHz. The BER has been determined in the wanted channel based on 300K bits yielding 0.003% in channel 0, 0.005% in channel 48, and 0.01% in channel 78. This means that the BER is indeed lower than 0.1% in all channels, as specified. This can be expected from the IIP3 value of −11 dBm, which is indeed better than the specified value of −21 dBm.

The interference behavior has been measured according to the Bluetooth specification based on 10K data bits in the wanted channel and a GFSK-modulated interferer with random data. The results are listed in Table II for channels 0, 48, and 78. For the various interferers at various carrier-to-interferer (C/I) ratios, the BER values are smaller than 0.001, as specified. It should be noted that the co-channel and adjacent channel specifications do not depend on the implementation of the receiver chain. The mirror specifications are dependent on the used IF frequency. Since we use an IF frequency of 500 kHz, the "mirror + 1 MHz" specification coincides with the co-channel specification, but is a lot more stringent since a C/I ratio of

TABLE II
MEASURED INTERFERENCE BEHAVIOR

Specification (incl. C/I ratio)	BER (ch. 0)	BER (ch. 48)	BER (ch. 78)
Co-channel (C/I=11 dB)	0	0	0
Adjacent±1 MHz (C/I=0 dB)	0	0	0
Adjacent±2 MHz (C/I=-30 dB)	0	0	0
Adjacent±3 MHz (C/I=-40 dB)	0	0.0003	0.0007
Mirror (C/I=-9 dB)	0.0001	0.0006	0.0001
Mirror-1 MHz (C/I=-20 dB)	0	0	0

TABLE III
PERFORMANCE SUMMARY OF THE RECEIVER CHAIN

Characteristic	Value	Bluetooth specification
Power consumption	31.7 mW	-
Sensitivity	-71 dBm	-70 dBm
Maximum input power	-19 dBm	-20 dBm
Linearity: IIP3	-11 dBm	-21 dBm
Interference behavior	See Table II	BER<0.001
Process	0.18-μm CMOS	-
Area	3.5 mm^2	-

−20 dB should be used. It is allowed to adhere to the most relaxed specification in this case. Therefore, the "mirror+1 MHz" specification has not been listed in Table II. The "mirror-1 MHz" specification coincides with the "adjacent-2 MHz" specification. In principle, the "adjacent-2 MHz" is less relaxed than the "mirror-1 MHz" specification, but since both are easily met, they have both been listed in Table II. The "adjacent±3 MHz" and mirror specifications are met only with a small margin in applicable C/I ratio.

The measured behavior and main characteristics of the receiver chain have been summarized in Table III. It can be concluded that all measured specifications comply with the Bluetooth standard. This means that apparently the crosstalk between the digital block and analog blocks is not a problem. This has been confirmed by measurements at the substrate "sensors" located inside the region labeled "Analog block" in Fig. 12 and available at dedicated pins. Switching on the digital block had no or hardly any effect on the noise level in the IF frequency band. Spurious tones at multiples of 8 MHz, i.e., the main clock frequency in the digital block, appear on the substrate inside the analog block with an attenuation of 20 dB or more compared to the substrate at the edge of the digital block. Future experiments have to reveal how much more attenuation can be achieved when a trench is etched between analog and digital [14].

VII. CONCLUSION

A 32-mW highly digitized receiver for GFSK applications in the 2.4-GHz ISM band has been realized in 3.5 mm^2 in 0.18-μm CMOS. The power consumption is at least a factor of two lower than for state-of-the-art CMOS receivers. The only external components are an antenna filter and a crystal. The main advantages of the highly digitized architecture are the simplicity and low power of the RF front-end, the flexibility toward new wireless standards, and the scalability of the digital back-end.

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