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InP-based Photodetector bonded on CMOS with Si_3N_4 interconnect waveguides

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***Abstract*—We developed an InP-based photodetector which was bonded on a CMOS wafer containing a Si_3N_4-wiring photonic circuit. The detector fabrication is compatible with wafer scale processing steps, guaranteeing compatibility towards future generation electronic IC processing. Integration technology and experimental results are presented in this paper.**

I. Introduction

THE integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution to face the bandwidth bottleneck expected at the interconnect level for future generation electronic ICs. This solution would provide bandwidth increase, immunity to EM noise and reduction in power consumption [1]. In our previous work, we demonstrated an InP-based photodetector (PD) structure suitable for optical interconnects on electronic ICs, processed on top of an SOI wafer containing Si interconnect waveguides [2]. In this paper, we show the integration of this type of PD with a real CMOS wafer, on top of which Si_3N_4 optical interconnect waveguides are patterned. The choice of a Si_3N_4 interconnect layer is driven by an easier integration with the CMOS circuitry underneath. The photodetectors are fabricated on top of the Si_3N_4 layer in a way compatible with wafer scale processing steps. In our example, the CMOS circuitry does not perform any specific task: it is only used to demonstrate the feasibility of integrating an optical interconnection layer on a real electronic IC topology and the use of our PD structure for such application. In this paper, we focus on technology aspects and experimental results.

II. Design and Fabrication

In our approach, the PD structure consists of a 700 nm InGaAs absorption layer sandwiched between an n-doped InP layer, which hosts the n-side contacts, and a p-doped InGaAs layer, on top of which the p-side electrode is defined (see Fig. 1). The PD has a footprint of 5×10 μm^2 and a thickness of 950 nm. This geometry is chosen to balance the trade-off between device efficiency and speed, as we reported in [2]. The active photonic devices are realized on top on a Si_3N_4 interconnect waveguide layer, defined on top of the last metallization layer in the CMOS circuitry. More specifically, a buffer layer of SiO_2 is first deposited by PECVD on top of the 8" CMOS layer and flattened by chemical-mechanical polishing (CMP). Then, a 400 nm thick Si_3N_4 layer is deposited by PECVD and patterned with 193 nm deep UV (DUV) lithography. The waveguides are subsequently dry-etched through the Si_3N_4 layer. In this way, 800 nm wide Si_3N_4 interconnect optical waveguides are defined. Details about design, fabrication and characterization of the Si_3N_4 waveguides are extensively presented in [3]. For manufacturing this chip, a 2" InP wafer with the detector layer stack was grown by MOVPE and molecular-bonded upside down on the 8" CMOS wafer. We refer to [4] for the details about this bonding technique. The InP substrate was then removed by a combination of CMP and HCl wet-chemical etching. The bonding layer thickness is 500 nm, which allows for evanescent coupling of the optical field from the interconnect Si_3N_4 wire to the PD absorption region. Even though our processing steps are compatible with wafer scale fabrication, after bonding the wafer was sawn in 3×3 cm^2 dies to allow for processing in the COBRA clean room. The PD structure was defined using III-V conventional wet-etching and dry-etching techniques. A polyimide layer was used to planarize the chip and provide electrical isolation and a Ti/Pt/Au metal stack was evaporated and patterned by lift-off. The photodetectors are aligned over Si_3N_4 structures as shown in Fig. 1. The input

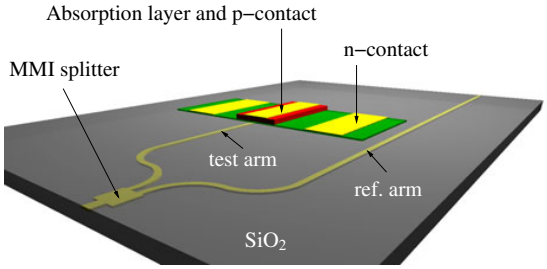

Fig. 1. Photodetector structure. The input optical signal carried by the Si_3N_4 interconnect waveguide is equally split by an MMI splitter into a test arm, on top of which the PD is aligned, and a reference arm.

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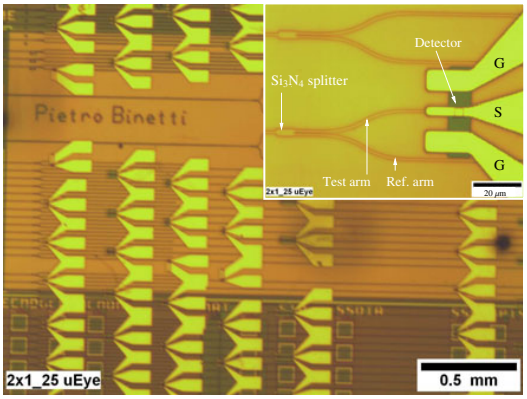

Fig. 2. Picture of the chip. RF pads and Si_3N_4 waveguides are indicated. In the close-up box, a PD and the initial part of the Ground-Signal-Ground (GSG) RF metal pads are shown.

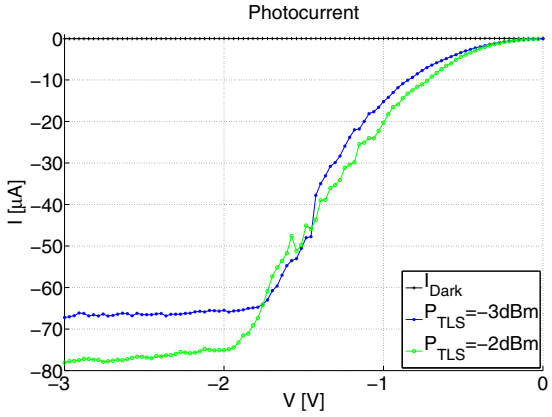

Fig. 3. Measured photocurrent for 0, −2 and −3 dBm TLS optical output power as a function of the detector applied bias voltage.

optical signal carried by the interconnect waveguide is split into two branches by a 3 dB MMI splitter. The PD is aligned over the test arm of the MMI splitter, while the remaining arm is used as a reference for the measurements. After the device processing, the samples were sawn from the backside to create facets that would allow for low-loss fiber-to-waveguide edge-coupling for the chip characterization. Fabricated devices are shown in Fig. 2.

III. Experimental Results

The detector DC characterization was performed by using an external HP8168A TLS and a Keithley 2400 source-meter unit to reversely bias the device and read out the generated photocurrent. Dark current values around 2 nA were registered at −4 V. The optical signal was edge-coupled into the waveguide and guided towards the detectors. The detector generated photocurrent as a function of the applied bias voltage was measured for TLS output powers of −2 and −3 dBm. The measurement results are shown in Fig. 3. To evaluate the detector efficiency, the following factors were considered. Firstly, the fiber connections from the TLS to the PC and to the coupling input fiber caused a loss of 0.7 dB. Secondly, an

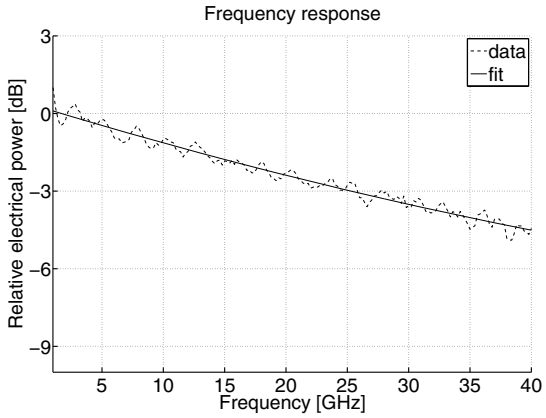

Fig. 4. Detector frequency response.

additional 3 dB loss caused by the integrated MMI splitter had to be taken into account. The insertion loss of the MMI splitter was neglected, as it was within the 0.1 dB accuracy of the measurements performed. Thirdly, the waveguide propagation loss was measured to be around 6 dB/cm at 1550 nm, as reported in [3]. That caused an additional 0.5 dB loss in the 1 mm long path to the detector. Lastly, a 3 ± 0.5 dB loss was estimated for the fiber-to-chip edge-coupling, determined by the fiber-waveguide mode matching and the Fresnel reflections at the chip facet, which were estimated to be around 10%. The responsivity of the PD structure was thus calculated to be 0.68 ± 0.1 A/W at 1550 nm, which corresponds to a quantum efficiency $55 \pm 8\%$ Dynamic measurements were performed in the range of 100 MHz to 40 GHz with an Agilent HPN4373B 67 GHz lightwave component analyzer (LCA), used for small signal modulation of the input optical power from the 1550 nm laser source integrated in the LCA optical module and for reading out the photogenerated RF electrical signal. Results are presented in Fig. 4, showing a 3 dB bandwidth of 25 GHz.

IV. Conclusion

We demonstrated a 50 μm^2 InP/InGaAs photodetector integrated via wafer-bonding technique with Si_3N_4 interconnect waveguides defined on top of a CMOS wafer. Photodetector measurements recorded a dark current of 2 nA, a responsivity of about 0.7 A/W and a 3 dB frequency response of 25 GHz.

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