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All-optical wavelength conversion at 160 Gbit/s using SOA and silicon-on-insulator photonic circuit

F. Gomez-Agis, O. Raz, S.J. Zhang, E. Tangdiongga, L. Zimmermann, K. Voigt, C. Vyrsokinos, L. Stampoulidis and H.J.S. Dorren

Error-free operation of an all-optical wavelength converter at 160 Gbit/s based on a semiconductor optical amplifier and a silicon-on-insulator photonic circuit, consisting of two cascaded Mach-Zehnder delay interferometers, is demonstrated.

Introduction: All-optical wavelength converters (AOWCs) are essential blocks for future optical communication networks [1]. A key component for their implementation is the semiconductor optical amplifier (SOA), which has received special attention because of its capability for photonic integration and low power consumption [2]. Silicon-on-insulator (SOI) based devices provide a possible migration to a strategy towards the convergence of integrated electronics and photonics on a single substrate [3], because this offers low cost of fabrication and high yield. Moreover, it is possible to match the silicon waveguide mode size to that of III–V active devices [4] to enable hybrid integration.

Error-free wavelength conversion based on cross-phase modulation (XPM) in a single SOA assisted by filtering at 320 Gbit/s using discrete components [5] and a monolithically integrated AOWC at 80 Gbit/s [6], consisting of an SOA and an arrayed-waveguide grating, have been demonstrated. In these experiments, the converted signal at the SOA output had the inverse polarity compared to the input signal. An optical filter with a central frequency slightly blue shifted with respect to the wavelength of the converted signal was placed at the SOA output to utilise XPM induced by the SOA to speed-up the AOWC nearly one order of magnitude. Subsequently, a delay interferometer (DI) is employed to obtain a non-inverted version of the converted signal by suppressing the carrier. Here, we present for the first time, error-free operation of an SOA-based AOWC at 160 Gbit/s using a single SOI photonic circuit carrying two functions: conversion of phase-modulation in amplitude modulation and polarity inversion on the converted signal.

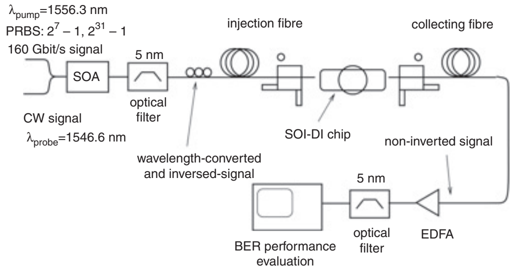

Fig. 1 *Experimental setup for wavelength conversion at 160 Gbit/s*

Experimental setup: The experimental procedure is depicted in Fig. 1. Optical pulses generated by a fibre modelocked laser (FMLL) with duration of 1.2 ps at 1556.3 nm and 40 GHz repetition rate, are amplitude modulated to form a $2^7 - 1$ return-to-zero on-off keying (RZ-OOK) PRBS signal and time-multiplexed to constitute a 160 Gbit/s bitstream, hereafter to be referred to as the pump. This signal is coupled into an SOA in combination with a CW light at 1546.6 nm, hereafter referred to as the probe, to use wavelength conversion through XPM. The employed SOA holds a 10–90% gain recovery time of 10 ps while pumped with an injection current of 500 mA. The SOA has a saturation output power of 15 dBm and a small-signal gain of 30 dB. The average optical power at the SOA input was −5 and −0.9 dBm for the pump and the probe, respectively. At the output of the SOA, an optical bandpass filter (OBF) with a 3 dB bandwidth of 5 nm is used to select the probe and reject the pump signal. The SOA output is coupled into the SOI photonic circuit, which converts XPM into amplitude modulation and suppresses the carrier to produce a non-inverted version of the wavelength converted signal. Finally, the output of the SOI photonic circuit is amplified by a low noise erbium-doped fibre amplifier (EDFA) and filtered for bit error rate (BER) performance evaluation.

The SOI chip consists of two periodic filters implemented as two concatenated passive Mach-Zehnder DIs integrated into a substrate area of 10 × 25 mm^2. The waveguide-based DIs hold a delay of 1 and 2 ps with a mode size area of the order of 3 μm^2 and were fabricated using SOI rib waveguide technology on substrates with a top silicon layer of 4 μm [4]. Light was carefully coupled in and out of the chip by means of micro-lensed fibres, which hold a spot diameter of the order of 3.5 μm attaining a fibre-to-fibre loss of 14 dB, indicating a per facet loss of 5.5 dB.

Results: The transfer characteristic of the SOI-DI is shown in Fig. 2. The light-grey trace represents the amplified spontaneous emission (ASE) of an EDFA used as input to the chip, covering the spectral range from 1530 to 1570 nm. The response of the chip to such input is shown in grey. From the normalised frequency response (black trace), one can observe an inner and an outer periodicity of 4 and 8 nm associated with the time delay introduced by each interferometer with a corresponding extinction ratio of 7 and 22 dB. In order to perform as a chirp filter and as a polarity inverter, it is necessary that one of the largest notches of the SOI-DI frequency response coincide with the probe's wavelength, either by tuning the chip response (e.g. by temperature control) or by assigning the correct wavelength to the probe.

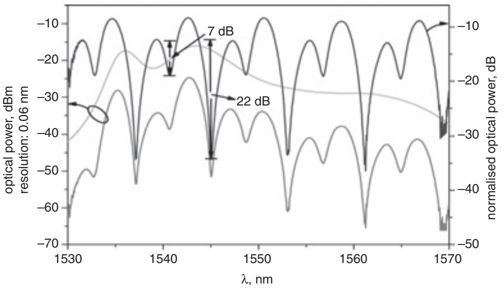

Fig. 2 *Frequency response of SOI-DI photonic circuit*

Light-grey trace: input; grey trace: frequency response; black trace: normalised frequency response

To investigate the chirp filtering properties of the SOI-DI chip, a 40 Gbit/s wavelength conversion experiment was carried out to illustrate the improvement performed by the chip on the recovery time of the SOA-based AOWC. In Fig. 3, we can observe that the recovery time of the AOWC is reduced from 12 to 4 ps, leading to the conducting of experiments at 160 Gbit/s.

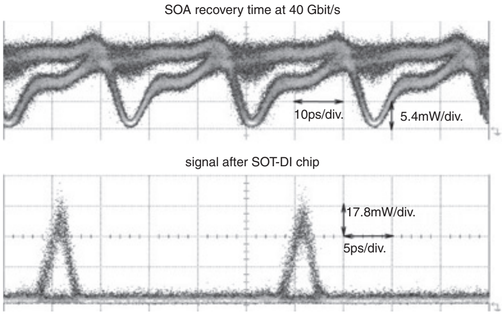

Fig. 3 *Chirp-filtering properties of SOI-DI at 40 Gbit/s*

The produced spectra and eye diagrams using different PRBS signals ($2^7 - 1$ and $2^{31} - 1$) at the input and output of the chip are shown in Fig. 4. The carrier of the input signal (light grey trace) holds an extinction ratio of more than 15 dB over the harmonics at 160 GHz. At the output of the chip, the spectrum of the probe is modified (grey trace): the extinction ratio between the carrier and the spectral lines at 160 GHz varied from 15 to −10 dB with respect to the first spectral line on the left and from 23 to 13 dB with respect to the first spectral line on the right. This carrier suppression is translated into a non-inverted version of the input signal. The output of the chip is then amplified and filtered (black trace) to perform BER measurements. From the eye diagrams we can verify that no patterning effect exists.

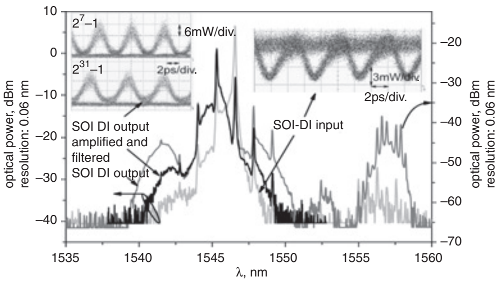

Fig. 4 *Input/output spectra and eye diagrams for SOI-DI photonic circuit*

Light-grey trace: SOI-DI input; grey trace: SOI-DI output; black trace: SOI-DI output amplified and filtered

The BER performance of the system is shown in Fig. 5. The circles illustrate the error-free operation of a single 40 Gbit/s channel that corresponds to the case without wavelength conversion. The squares represent the 160-to-40 Gbit/s without wavelength conversion used as a reference, whereas the stars represent the wavelength converter channels using the SOA-based AOWC. Error-free operation is achieved on all the channels with an average optical receiver power of −7.5 dBm. This value corresponds to an average power penalty of 5.5 dB. This penalty is due to a reduction of the signal-to-noise ratio introduced by the light coupling in the SOI device. Signal-to-noise ratio can be improved by using a pigtailed device, leading to reduced penalties.

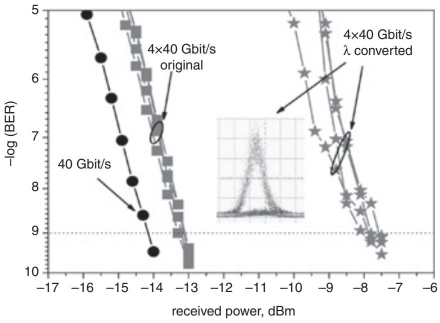

Fig. 5 *BER curves of SOA-based AOWC*

Circles: single channel without wavelength-conversion; squares: 4 × 40 Gbit/s without wavelength-conversion; stars: 4 × 40 Gbit/s with wavelength-conversion

Conclusion: This Letter represents the first report on a successful AOWC at 160 Gbit/s employing a photonic integrated circuit, based on silicon-on-insulator technology, providing two functionalities: chirp filtering and polarity inversion. Error-free operation was achieved for all the channels attaining an average power penalty of 5.5 dB. The results outlined here, demonstrate the potential of SOI chips in ultra-high-speed optical signal processing.

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