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A Spot-Defect to Fault Collapsing Technique

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1. Abstract

Knowing the effects of process induced spot defects on an IC circuit design is very important for both IC testing and IC process diagnosis. Based on a new method of extracting "multilayer" critical areas from a circuit layout, we present a new technique capable of collapsing defects to circuit faults by establishing a simple probabilistic model between them. This way of modeling supplies accurate results for ranking the failure probability of nodes and the probability of occurrence of faults.

2. Introduction

Spot defects, as a major disturbance in IC manufacturing, can cause quite complex faulty behaviors of ICs. The conventional fault models established at the gate-level, such as line stuck-at faults, are no longer sufficient when a high quality test is desired [1]. The basic problems are 1) the faults may not be physically present, and 2) the faults that occur physically may not be detected by the tests generated for such a fault model [2]. Hence, the possible faults should be extracted from their real origin: the layout, and be weighted according to the defect conditions prevailing in the manufacturing line. In normal designs, we encounter situations where more than one different defect mechanism induces the same fault, or vice versa only one defect mechanism induces more than one fault. Therefore, there is a need to perform a defect to fault collapsing in order to weight the probability of occurrence of each different fault or the probability of failure of each different node. Faults may be weighted as a function of their critical areas [3], the size(s) of the defects involved, and the corresponding defect densities of the manufacturing line. Our analysis distinguishes from others [4, 5] in that we first extract the critical areas from the layout for each different defect mechanism, then perform a defect collapsing per fault on each circuit's node, and finally apply a simple probabilistic method to weight the fault.

3. Critical Areas and Circuit Sensitivities

Spot defects are conceptualized as missing or extra materials on a specific layer of the layout. They may cause fatal bridges or breaks among patterns [4]. Spot defects can be characterized by a defect size distribution and a defect density, namely the probability of occurrence of each different defect size, and the number of defects per unit area [6].

The combination of layers of an IC, let us call it "structure", corresponds to certain electrical elements, like a transistor or a via. Therefore, whenever a defect is present on some layer of a structure it may induce an electrical faulty behavior on the entire structure. Thus, the "multilayer critical area" is the area where the center of a defect must occur in order to introduce a fault to the whole structure. For instance, the structure "transistor" will not function if a portion of the diffusion or polysilicon or thin oxide layers are missed. From this observation, we can infer that it is possible to have as many critical areas per layer as the number of defect mechanisms affecting each one of the layers of the structure.

As an example, consider a spot of polysilicon capable of bridging another polysilicon pattern, and at the same time also capable of spanning over a diffusion pattern. Clearly the bridge between the patterns creates a short circuit fault, and the spanning creates a parasitic transistor. Therefore we can establish two different critical areas, one for the bridge and one for the spanning. Furthermore, if the critical areas intersect, we will encounter three different sections imposed on them, one section for the "bridge critical area", another for the "spanning critical area", and the last for both "bridge-spanning critical area". According to this observation we can have three different situations on which a fault can occur. Namely, if the center of the defect falls in the "bridge critical area" the short circuit fault arises, if the center of the defect falls in the "spanning critical area", a parasitic transistor is created, and if the center of the defect falls in the "bridge-spanning critical area" both faults can occur. For every defect mechanism, the multilayer critical areas can be extracted as it is illustrated in [7].

4. Defect-Fault Collapsing

Before further discussions we first introduce some notations. Let $M=\{m_1, m_2, \ldots, m_I\}$ be the set describing all possible independent defect mechanisms, i.e. extra metal, missing polysilicon, etc. Assume that the occurrence of a defect mechanism is a stochastic independent process, e.g. every defect mechanism has the same probability of occurrence. As defects from every defect mechanism occur with a stochastic size and number, let $D_m(x)$ represent their size distribution and γ_m their density, where x denotes the defect size, confined from *min* to *max*, and m, $m \in M$, the defect mechanism. Let also $F=\{f_1, f_2, \ldots, f_J\}$ be the set describing all possible distinct fault types, i.e. bridge, line open, transistor stuck-on, etc, and let $N=\{o_1, o_2, \ldots, o_K\}$ be the set containing all the electrical nodes of the design. Since one defect mechanism can induce more than one fault on one or more nodes, we express a *fault item*, $<f,n>$, as a subset of faults f on a subset of nodes n, where $f \subset F$ and $n \subset N$.

The sensitivity of a fault item $<f,n>$ due to a defect of size x from a defect mechanism m, or probability that such a fault item occurs, is related to its multilayer critical area by

$$A_m^{<f,n>}(x) = S_m^{<f,n>}(x)\, A_{layout} \tag{1a}$$

where $A_m^{<f,n>}$ is the multilayer critical area, and $S_m^{<f,n>}$ the sensitivity, due to a defect mechanism m, both as a function of a defect size x. A_{layout} is the total layout area. Further, with the assumption of stochastically independent defect mechanisms, the following equation can be obtained

$$W_S^{<f,n>}(x) = \sum_{\forall m \in M} S_m^{<f,n>}(x) \tag{1b}$$

Eq.(1b), represents the likelyhood of occurrence of a fault item $<f,n>$ due to one defect of size x from every possible defect mechanism.

This sensitivity (eq.(1a)) is in fact a measure of the design's vulnerability to different defect mechanisms and to each different defect size. However, in a manufacturing environment the

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probability of occurrence of each different defect size is not the same. Therefore, the average probability of occurrence of a fault item $<f,n>$ due to a defect from a defect mechanism m is computed as

$$\Phi_m^{<f,n>} = \int_{min}^{max} S_m^{<f,n>}(x) D_m(x) dx \qquad (2a)$$

where $S_m^{<f,n>}(x)$ is obtained from eq.(1a) and $D_m(x)$ is the defect size distribution existing in the manufacturing line. Eq.(2a) represents in fact a defect collapsing for all defect sizes from the same defect mechanism. Similar to eq.(1b), the collapsing for all possible defect mechanisms results in eq.(2b) as

$$W_\Phi^{<f,n>} = \sum_{\forall m \in M} \Phi_m^{<f,n>} \qquad (2b)$$

This equation represents the likelyhood of occurrence of a fault item $<f,n>$ due to a defect, with its size possibly ranging from min to max, from every possible defect mechanism.

Since more than one defect from a defect mechanism m may occur, we obtain the average number of times that $<f,n>$ occurs as

$$\lambda_m^{<f,n>} = \gamma_m A_{layout} \Phi_m^{<f,n>} \qquad (3)$$

where $\Phi_m^{<f,n>}$ is computed from eq.(2a). As mentioned before, more than one defect mechanism can induce the same fault item. Therefore, the weight of each fault item $<f,n>$ due to defects from all possible defect mechanisms is expressed as

$$W_\lambda^{<f,n>} = \sum_{\forall m \in M} \lambda_m^{<f,n>} \qquad (4a)$$

where each $\lambda_m^{<f,n>}$ is obtained from eq.(3). This weight represents the likelyhood of occurrence of the fault item $<f,n>$. It also reflects the defect collapsing for all defect mechanisms taking into account the defect density. After substitution of eq.(1a), eq.(2a) and eq.(3) into eq.(4a), we get the final weight as

$$W_\lambda^{<f,n>} = \sum_{\forall m \in M} \gamma_m \int_{min}^{max} A_m^{<f,n>}(x)\, D_m(x) dx \qquad (4b)$$

Following a similar development it is possible to find the total weight of failure for a particular node. This weight is obtained as

$$W_\lambda^{o_i} = \sum_{\forall m \in M} \gamma_m \int_{min}^{max} A_m^{o_i}(x)\, D_m(x) dx \qquad (5)$$

where the $A_m^{o_i}(x)$ is the critical area of an electrical node o_i, $o_i \in N$. This critical area is the area where the center of a defect with size x from a defect mechanism m must occur so that node o_i will fail to function. Indeed, eq.(5) reflects also the collapsing of different types of faults.

Based on a system capable of extracting multilayer critical areas, a post-processor has been constructed to process the extracted critical areas and to compute the weights developed above. Our system for critical area extraction constructs the critical areas per defect mechanism deterministically. As a result, the collapsing phase is independent of the critical areas extraction. With such a modular feature, further analysis, for example, to verify the same design for different defect conditions, can be done without performing the whole extraction procedure. Consequently, our technique can save a lot of CPU time as compared to the full simulation method of [4, 5].

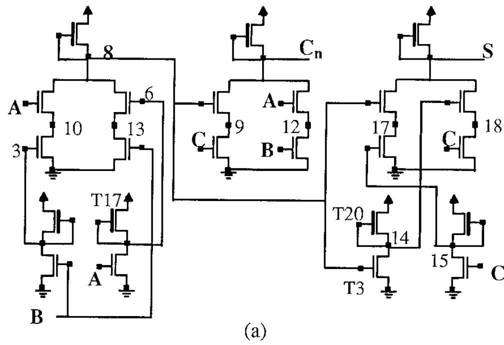
The defect to fault collapsing phase is implemented in two steps. First, the post-processor groups all the possible defect mechanisms for each fault item, i.e. if defects of extra metal and extra contact both cause a bridge fault on the same nodes, then the critical areas for each defect size of both defect mechanisms will be put in a group. This process is repeated for every different mechanism of each fault item $<f,n>$. After such a grouping, the total number of faults for every type of fault is reduced to the total number of distinct fault items. In the second step, the weight for each fault item is computed. In this step, the defect size distribution and defect densities are taken into account so that the real weight can be obtained. The weight of each fault item is computed one at the time. First, different defect sizes are collapsed by applying eq.(2a) for each possible defect mechanism. Then eq.(4a) is operated to obtain the total weight by collapsing different defect mechanisms. Noticing that the critical area of every fault item $<f,n>$ is also the partial critical area for any related electrical node o_i, where $o_i \in n$, $n \subset N$, the weight of each node is also computed with the collapsing formula of eq.(5) at the same time.

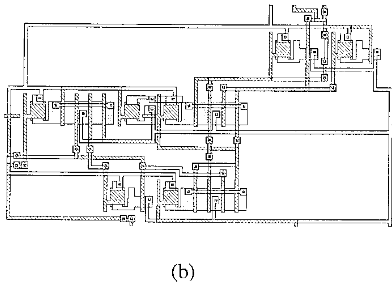
5. The Results of Collapsing

In order to show the effectiveness and applications of this collapsing technique, we analyzed an example circuit by using our system. The circuit chosen is a full adder implemented in a Standard Cells Place and Route approach. The technology used is NMOS of 6μ of minimum resolution features consisting of the following layout masks: diffusion, polysilicon, buried contact, metal, implant, and normal contact. The circuit consists of twenty three transistors with three primary inputs and two primary outputs. Fig. 1 (a) and (b) illustrates the schematic diagram and layout, respectively. The first action towards the defect to fault collapsing consists in extracting the multilayer critical areas of each possible fault item from the layout. For simulation purposes, missing (extra) spots of material of the buried and contact masks are used to simulate spot defects of extra (missing) material in the thin and thick oxide layers of the IC, respectively. The critical areas are extracted for defect sizes ranging from 6μ to 20μ with incrementing steps of 2μ.To give an idea about the critical areas, two examples are shown in Fig. 2 for defects of missing polysilicon of 10 μ and extra metal of 16 μ. All considered defect mechanisms are listed in the first column of Table 1, the type and number of faults due to each individual defect mechanism are listed as well. The last row of Table 1 shows the results of defect to fault collapsing without fault equivalence and without considering the manufacturing conditions. We can see that around half of the extracted faults, 124 out of 234, are multiple faults. From the whole list of faults we found that 86 of them, including single and multiple, were bridges, from which 41 were bridges to *vdd* or *vss*. The multiple faults indicate that more than one fault can be induced by one defect. As an example, a missing metal defect may result in two different nodes being opened, or an extra polysilicon defect may cause one node to be opened and two other different nodes to be bridged at the same time.

In order to observe the dependence of the extracted faults to possible variations of the manufacturing line, the same collapsing technique is conducted for three different defect characteristics. We characterized the defect size distributions according to the model presented in [8]. Every defect size distribution was forced to peak at a defect size of 6 μ. In our analysis, we assume that every defect mechanism has the same defect size distribution. The three cases are:

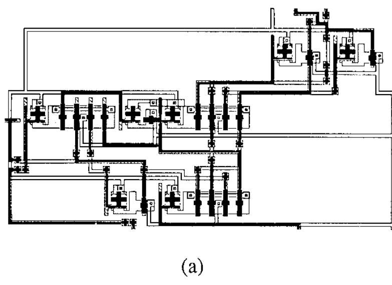
- **Case 1**: The defect size distribution obeys a $1/x^3$ law and the defect density for each defect mechanism has the same value of 2 $defects/cm^2$.
- **Case 2**: The defect density distribution remains the same as in case 1, while the defect size distribution is constrained by $1/x^2$.
- **Case 3**: The defect size distribution is the same as in case 1, but only the defect density of extra metal is increased to 6 $defects/cm^2$, the rest of the mechanisms remains with the same value of 2 $defects/cm^2$.



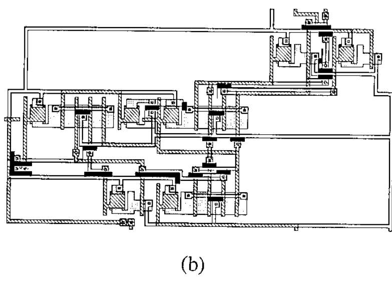


(b)

Figure 1. Full adder. (a) Schematic diagram. (b) Layout.



(a)



(b)

Figure 2. Critical areas are highlighted in black. (a) Missing polysilicon. (b) Extra metal.

Case 1 represents a mature process, case 2 is chosen to show the effects of a defect size distribution allowing a higher probability of occurrence for large defect sizes, and case 3 is used to discover which fault item's weight and which node's weight are sensitive to a change in the density of a particular defect mechanism.

It is inconvenient to list the weight variation for all the extracted faults because of the large volume of the fault list. Instead only the weights of 9 faults are shown in Table 2. By inspecting the weighted fault list in each case, we can conclude that the weights of multiple faults are smaller than the ones of single faults. However, though their respective weights are relatively low, the weights of some multiple faults can be bigger than the weights of some single faults. As an example, we can find for case 3, in Table 2, that the weight of the multiple fault $F6$ is bigger than the one of the single fault $F5$. Therefore, multiple faults should not easily be neglected when testing is being done. Comparing the weighted fault lists of case 1 and case 2, we also observed, as it is expected, that for case 2 all the faults have higher likelyhood of occurrence than the ones of case 1, as it is partially illustrated in Table 2. Moreover, the weight increase is not uniform for every fault. This indicates that under different manufacturing environments the

TABLE 1. Extracted Faults

Defect mech.	Number of faults					
	lop	bri	tsop	tson	newt	multiple
miss buried.	7	-	-	-	-	-
extra buried.	-	7	-	16	-	1
miss contact	10	-	-	-	-	4
extra contact	-	28	-	-	-	31
miss diffu.	9	-	-	-	-	1
extra diffu.		8			-	1
miss implant	-	-	7	-	-	-
extra implant	-	-	-	16	-	-
miss metal	10	-	-	-	-	17
extra metal	-	19	-	-	-	4
miss poly.	10	-	23	-	-	33
extra poly.	9	20	-	-	3	43
after collapse	12	56	23	16	3	124

lop=line open bri=bridge tsop=transistor stuck-open
tson=transistor stuck-on newt=parasitic-transistor.

TABLE 2. Weights of partial faults ($x\,10^{-6}$)

case	Single Faults					Multiple Faults			
	F1	F2	F3	F4	F5	F6	F7	F8	F9
1	24.4	13.8	9.72	5.18	0.025	0.228	0.019	0.014	0.004
2	29.6	22.2	12.4	7.84	0.065	0.450	0.049	0.037	0.011
3	25.8	13.8	9.72	6.99	0.025	0.608	0.055	0.014	0.004

F1 = bri *vss* 8
F2 = lop 6
F3 = tsop T17
F4 = bri *C S*
F5 = newt *S* 15 (Gate = *S*)
F6 = bri *vdd C S*
F7 = bri *vss C* 15
F8 = lop 3 6
F9 = tsop T3 T20

faulty behavior of the same design can have different impact. The effect of increasing the density of extra metal defects results in an increase of the weights of 23 faults, 5 of them are listed in Table 2.

The results for the weight variation of each node are shown in Fig.3. We can see that the weight per node, in case 2, changes considerably as compared to the one of case 1. It can also be found that only nodes $vss, B, 3, vdd, A, Cn, 8, C, 15, S$ are sensitive to extra

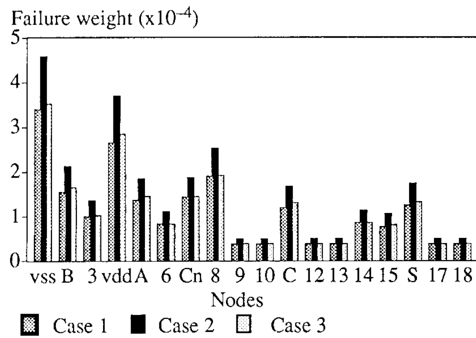


Figure 3. Weight variation of nodes.

metal defects. It is expected that for Standard Cell designs, this kind of weight spectrum will in general be observed. The reason is because nodes such as, power supply, primary inputs, primary outputs and the connections between different cells involve long connection patterns and large number of crossings among them. Therefore, more critical areas are extracted for these nodes than for the ones inside the cells, which are characterized by rather short connection patterns and where mostly transistors are directly abuted through the diffusion layer. This last kind of nodes are, for example, nodes 9, 10, 12 and 13 etc. in our full adder.

These results can supply several potential applications for both designer and manufacturer. For example, the designer can refine his design so that the likelyhood of certain faults or certain failing nodes can be minimized to an acceptable level. By comparing the simulated 'signature' (e.g. weight spectrum in Fig. 3) to the one obtained from the actual IC testing, which can be constructed as it is suggested in [9], the diagnosis of manufacturing process can be done as well.

Another result of our collapsing is to verify what is the impact of the weighted realistic faults on a test strategy. First, we generated seven patterns for this full adder using a D-algorithm. These patterns can achieve a 100% coverage for 46 assumed stuck-at faults at the gate-level. These patterns were used as a stimulus to simulate all the weighted single faults on a switch level fault simulator [10]. Since this simulator can not handle the multiple faults, they were not simulated in our analysis. Both weighted and unweighted fault coverages are illustrated in Table 3 only for the extracted faults which were collapsed according to the defect

TABLE 3. Simulation Results of the full adder

#Patterns	Fault Coverage	
	Weighted	Unweighted
1	0.2%	1.47%
2	23.4%	26.5%
3	57.3%	59.6%
4	68.5%	70.6%
5	74.3%	75.7%
6	81.4%	83.8%
7	96.4%	97.1%

characteristics specified in case 1. The results of the simulation show that even for single faults a 100% coverage cannot be reached by this unsequenced test pattern set. The undetected fault is $F3$ in Table 2. This fact indicates the inefficiency of conventional testing methods.

6. Conclusions

As it can be seen, the established probability model for defect to fault collapsing is quite comprehensive. Since it is independent of the multilayer critical area extraction, the collapsing and its related applications can be done effectively in a rather short CPU time. By applying this technique, the likelyhood of occurrence of faults, induced by defects, can be ranked accurately according to the conditions prevailing in the manufacturing line. The derivation of the weighted spectrums of nodes, or partial faults, can further be used for manufacturing debugging. The results of the analysis show that conventional testing methods concentrating on single stuck-at faults are insufficient, particularly, multiple faults need more careful treatment.

References

[1] F.J. Ferguson and J.P. Shen, "A CMOS Fault Extractor for Inductive Fault Analysis," *IEEE Trans. on Computer-Aided Design*, vol. CAD-7, no. 11, pp. 1181-1194, November 1988.

[2] W. Maly, "Realistic Fault Modeling for VLSI Testing," *24th IEEE/ACM Design Automation Conference*, pp. 173-180, 1987.

[3] C.H. Stapper, "Modeling of Integrated Circuit Defect Sensitivities," *IBM J. Res. Develop.*, vol. 27, no. 6, pp. 549-557, November 1983.

[4] W. Maly, F.J. Ferguson, and J.P. Shen, "Systematic Characterization of Physical Defects for Fault Analysis of MOS IC Cells," *Proc. of 15th Int. Test Conf., IEEE*, pp. 390-399, 1984.

[5] J.P. Shen, W. Maly, and F.J. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits," *IEEE Design and Test of Computers*, pp. 13-26, December 1985.

[6] W. Maly, M. Thomas, J. Chinn, and D. Campbell, "Characterization of Type, Size and Density of Spot Defects in the Metalization Layer," in *Yield Modeling and Fault Tolerance in VLSI*, , ed. W. Moore, W. Maly and A.J.Strojwas, pp. 71-91, Adam Hilger, 1988.

[7] J. Pineda de Gyvez and J.A.G. Jess , "On the Definition of Critical Areas for IC Photolithographic Spot Defects," *Proceedings of 1st European Test Conference*, pp. 152-158, April 1989.

[8] A.V. Ferris-Prabhu, "Role of Defect Size Distribution in Yield Modeling," *IEEE Tran. on Electron Devices.*, vol. ED-32, no. 9, pp. 1727-1736, September 1985.

[9] W. Maly and S.B. Naik, "Process Monitoring Oriented IC Testing ," *Proceedings of International Test Conference*, pp. 527-532, 1989.

[10] A.L. Oliveira and N.R. Rua, "SWIFT: Switch-level Fault Simulator with Timing Information ," User's Manual INESC, Portugal, 1988.