

Introduction to the Special Issue on the 2009 IEEE International Solid-State Circuits Conference

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Introduction to the Special Issue on the 2009 IEEE International Solid-State Circuits Conference

THE IEEE International Solid-State Circuits Conference (ISSCC) is the foremost global forum for presenting advances in solid-state circuits and systems-on-a-chip. Every year since its very first issue, the IEEE JOURNAL OF SOLID-STATE CIRCUITS has highlighted some well-received papers from the most recent ISSCC in special issues. This special issue is for the ISSCC conference held in San Francisco, CA, February 8–12, 2009. Session chairs and co-chairs initially recommended papers for publication, with final decision for inclusion based on peer review.

I. HIGH-PERFORMANCE DIGITAL PAPERS

Next-generation processors, SoCs, and their building blocks demonstrate continuous improvement in functionality and computing capability with increased efficiency and flexibility. Smaller transistors help, but it is evident that future progress in microelectronics will more and more rely on efficient circuits and system architectures. This can be also seen in the three papers in this section, chosen from the ISSCC 2009 session on microprocessor technologies.

The first paper, by Rusu *et al.*, describes a 2.3 B transistor processor with eight dual-threaded 64-bit cores and 24 MB shared L3 cache in a 45 nm 9-metal process. Multiple clock and voltage domains are used to reduce power consumption. Long channel devices and cache sleep mode are used to minimize leakage. Core and cache recovery improve manufacturing yield and enable multiple product flavors from the same silicon die.

In the second paper, Saito *et al.* demonstrate an efficient solution for management of the increasingly large on-chip memories in SoCs. The on-chip memory has been moved onto a separate and dynamically reconfigurable memory chip. The memory chip is then stacked on the logic chip by using a three dimensional packaging technology with high-bandwidth 10 μm -pitch micro-solder interconnects. This enables high-throughput inter-chip communication in a system-in-package, relieving the area penalty induced by large on-chip memory sizes.

The third paper, by Tokunaga *et al.*, presents an area- and power-efficient method to protect hardware encryption systems. A switched capacitor circuit equalizes the current and isolates the critical encryption activity from the external power supply. This eliminates the side-channel information leakage through the power supply, used by attackers to reveal the secret encryption keys. Utilizing this technique, a secure encryption system is implemented in a 0.13 μm CMOS technology with 7.2% area and 33% power overheads and 2 \times performance degradation. After ten million side-channel attacks, the secret encryption key still could not be revealed.

II. LOW-POWER DIGITAL PAPERS

The Low-Power Digital section consists of six papers describing advances in multimedia processors and digital wireless communication. The papers mainly focus on improving energy efficiency, to enable low-power applications like human body monitoring. Close combination of algorithm and hardware design, and scalable functionality such as multi-standard capabilities result in lower power dissipation and lower cost solutions. All these developments are paving the way to the Green IT era.

The first paper, by Kim *et al.*, describes a real-time multi-object-recognition processor featuring a multicastable network-on-chip (NOC), a biologically inspired neural perception engine (NPE), and a multi-object recognition algorithm based on human-like visual perception. This 201.4 GOPS processor can achieve 60 frame/sec recognition of up to 10 different objects for VGA video input while dissipating 496 mW.

The latest developments in display panels are driving High-Definition (HD) video into the mainstream. The handset is the most affordable and easily accessible device for capturing video. In the next two papers, SoCs conceived to make Full-HD video affordable to the consumer world are presented.

The second paper, by Ding *et al.*, introduces a scalable multi-view video-encoding which supports both multiple-HD and Full-HD resolution. The chip can decode video up to 1-view Quad Full-HD (4096 \times 2160), 3-view Full-HD or 7-view HD for multiple or 3 D-display applications. The chip achieves a 212 M pixel/sec throughput, which corresponds to a 3.4 to 7.7 times improvement on previous reports. Video resolution up to Full-HD is thus no longer limited to large or costly systems.

In the third paper, Iwata *et al.* describe the first Full-HD 1080p30 mobile application processor in 65 nm CMOS to support multi-standard video codec for handsets. The researchers apply a heterogeneous multiprocessor architecture to obtain high performance, flexibility, and low-power consumption in video codec processing using low-power DDR-SDRAM. This development is likely to lead at very short term to the first handset with Full-HD camcording capability.

The fourth paper, by Van Helleputte *et al.*, presents a fully integrated, flexible and ultra low power ultra-wide-band impulse radio (IR-UWB) receiver, capable of cm-accurate ranging. The first IR-UWB standard was defined in 802.15.4a as a competitor for Bluetooth and Zigbee able to provide better energy efficiency. A complete combination of RF front-end and baseband circuitry consumes 4.2 mW, resulting in an energy dissipation of 108 pJ/pulse. This kind of work promises to enable the creation of batteryless wireless sensor units for applications like on-body monitoring.

The signal processing in the low power digital domain is moving from full-hardware solutions to programmable ones. Flexible hardware and reusable software configurations, the

so-called “Hard Software and Soft Hardware,” are expected in the next generation of applications. The last two papers of this section focus on programmable hardware solutions for RF functions and heterogeneous architectures.

In the fifth paper, Busson *et al.* introduce programmability in RF functions by moving most of analog processing to the digital domain in a Digital Channel Multiplexer (DCM) for a satellite outdoor unit running at 1 GHz clock frequency and implemented in a mixed oxide dual voltage 65 nm CMOS technology. Using the DCM, it is not necessary to have a SAW filter for each channel. The chip consumes less than 1022 mW: a power reduction of more than $5\times$ versus existing state-of-the-art solutions.

In the last paper, Kaul *et al.* describe the design of a reconfigurable 4-way SIMD accelerator engine fabricated in 45 nm high-k/metal-gate CMOS. The main target is the acceleration of vector processing in power-constrained mobile microprocessors. The SIMD accelerator is reconfigured to perform 4-way 16 bit \times 16 bit multiplications, 32 bit \times 32 bit multiplications, 4-way 16 bit additions, 2-way 32 bit additions or 72 bit additions with a wide supply voltage range (1.3 V–230 mV). This accelerator computes at 2.8 GHz maximum frequency consuming 278 mW at 1.3 V. It reaches a maximum energy efficiency of 494 GOPS/W at 300 mV supply.

III. MEMORY PAPERS

Memory continues to play an essential role in all modern VLSI systems. As CMOS technology scaling has advanced well below 100 nm in feature size, many conventional memory technologies are facing severe challenges while new technologies are being explored for the future applications. In this section, five technical papers are chosen from the three memory sessions at 2009 ISSCC. These papers address a wide range of critical challenges facing today’s memory design.

The first paper, by Wang *et al.*, reports the industry’s first 32 nm SRAM design on a high-performance CMOS technology with high-k metal gate. The chip achieves up to 4 GHz operating frequency at 1.0 V along with a large voltage scaling window. The new design also introduces an integrated power management scheme that is able to reduce leakage power by over $2\times$.

The second paper, by Kang *et al.*, introduces an 8 Gb DRAM design by using Through-Silicon-Via (TSV) technology. This 4-stack 3-D design features master–slave architecture and significantly reduces both active (50%) and standby (25%) power consumption. By reducing the IO loading, this design also achieves over 1600 Mb/s speed using a DDR3 interface.

Memory bandwidth has become particularly important for graphics applications. The next paper, by Kho *et al.*, introduces a high-performance DRAM design in a 75 nm process. This design achieves IO speed of 7 Gb/s/pin for 1 Gb GDDR5 DRAM by using various circuit and architecture techniques, including array configuration and new IO interface design.

The following paper, by Saito *et al.*, presents a new wireless chip to chip IO interface in a NAND based flash stacking for Solid-State-Drive (SSD) applications. The design uses a programmable bus based on inductive-coupling to achieve up to 2 Gb/s data rate in a relayed transmission between 64 stacked NAND chips, while reducing both circuit area and power consumption.

The last paper, by Shiga *et al.*, presents an emerging memory. It describes the highest level of integration for a chain FeRAM architecture to date with a density of 128 Mb. This stand-alone design features a 1.6 GB/s DDR2 interface, new bitline architecture, and a small parasitic capacitance sensing scheme.

IV. TECHNOLOGY DIRECTIONS PAPERS

This section includes nine papers from the Technology Directions session of ISSCC 2009. The first three papers describe different implementations of networks of wireless sensor/actuators. The energy available in the each network node is severely limited by its physical dimensions and weight, making it especially important to realize energy-efficient circuit operation.

In the first paper, Daly *et al.* discuss a wireless node able to control the flight of a moth exploiting electric stimulation of the animal’s muscles. The main focus of the paper is on the highly duty-cycled pulsed-ultra-wideband receiver, which requires 0.5-to-1.4 nJ/bit and achieves a sensitivity of -76 dBm at a data rate of 16 Mb/s (10^{-3} BER). The second paper, by Flatscher *et al.*, describes a sensor node to be used in a wireless tire pressure monitoring system for automotive applications. Also in this case the paper mainly deals with the low-power transceiver designed for this system. The current consumption of the transceiver is 6 mA in transmit mode with a transmit output power of 1 dBm and 8 mA in receive mode with a sensitivity of -90 dBm, a data rate of 50 kBit/s and a bit error rate of 10^{-2} . The third paper, by Yoo *et al.*, discusses a body sensor network built using sensor nodes that can be embedded in adhesive bandages. The sensor nodes obtain the energy they need to work via electromagnetic coupling to the controller, which is attached to a relatively large battery. Details are given on the energy transfer system (which includes a rectifier with 54.9% efficiency), on the low-power sensing chain (which realizes electrocardiogram measurements while consuming 12 μ W), and on the network controller IC.

The following two papers discuss advanced solutions to provide miniature sensor nodes with energy. The work by Ramadass *et al.* focuses on rectifiers that can improve the transfer of power to the load when used together with piezoelectric energy scavengers. An improvement of more than $4\times$ in power extraction capability over conventional full-bridge rectifiers and voltage doublers is demonstrated. The contribution by Frank *et al.* presents a stabilized power supply exploiting a chip-integrated fuel cell based on hydrogen storage in a palladium layer. The fuel cell system delivers a maximum power output of 450 μ W/cm².

The next two papers present novel oscillators. Villard *et al.* discuss in detail a nano-sized oscillator based on spin momentum transfer torque and a dedicated wideband amplifier. This device shows a tuning range that can reach 100% for frequencies between 1 and 10 GHz, paving the way to innovative frequency synthesis solutions. The paper by Ruffieux *et al.* describes a temperature-stabilized silicon resonator achieving 3.2 μ W power dissipation at 1 V for real-time clock applications.

The paper by Young *et al.* discusses near-to-long-term optical interconnect solutions, forecasting an energy efficiency better

than 0.3 pJ/b for optical interconnects implemented in 16 nm CMOS and exploiting photonic components integrated in the backend.

Finally, the contribution by Ishida *et al.* presents a flexible electronic sheet integrating 2 V organic CMOS electronics and antennas with silicon LSI chips. This device is able to map the spatial distribution of EMI interference sources up to 1 GHz and demonstrates how silicon and organic electronics can be integrated to obtain at the same time mechanical flexibility, large area capability and performance.

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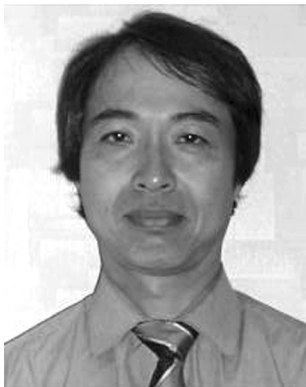
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