

# Trapping of electrons in metal oxide-polymer memory diodes in the initial stage of electroforming

**Citation for published version (APA):**

Bory, B. F., Meskers, S. C. J., Janssen, R. A. J., Gomes, H. L., & Leeuw, de, D. M. (2010). Trapping of electrons in metal oxide-polymer memory diodes in the initial stage of electroforming. *Applied Physics Letters*, 97(22), 222106-1/3. [222106]. <https://doi.org/10.1063/1.3520517>

**DOI:**

[10.1063/1.3520517](https://doi.org/10.1063/1.3520517)

**Document status and date:**

Published: 01/01/2010

**Document Version:**

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

**Please check the document version of this publication:**

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

**General rights**

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

[www.tue.nl/taverne](http://www.tue.nl/taverne)

**Take down policy**

If you believe that this document breaches copyright please contact us at:

[openaccess@tue.nl](mailto:openaccess@tue.nl)

providing details and we will investigate your claim.

## Trapping of electrons in metal oxide-polymer memory diodes in the initial stage of electroforming

Benjamin F. Bory,<sup>1</sup> Stefan C. J. Meskers,<sup>1,a)</sup> René A. J. Janssen,<sup>1</sup> Henrique L. Gomes,<sup>2</sup> and Dago M. de Leeuw<sup>3</sup>

<sup>1</sup>Molecular Materials and Nanosystems, Eindhoven University of Technology, P.O. Box 513, 5600 MB Eindhoven, The Netherlands

<sup>2</sup>Center of Electronics Optoelectronics and Telecommunications (CEOT), Universidade do Algarve, Campus de Gambelas, 8005-139 Faro, Portugal

<sup>3</sup>Philips Research Laboratories, Professor Holstlaan 4, 5656 AA Eindhoven, The Netherlands

(Received 8 September 2010; accepted 4 November 2010; published online 30 November 2010)

Metal oxide-polymer diodes require electroforming before they act as nonvolatile resistive switching memory diodes. Here we investigate the early stages of the electroforming process in Al/Al<sub>2</sub>O<sub>3</sub>/poly(spirofluorene)/Ba/Al diodes using quasistatic capacitance-voltage measurements. In the initial stage, electrons are injected into the polymer and then deeply trapped near the poly(spirofluorene)-Al<sub>2</sub>O<sub>3</sub> interface. For bias voltages below 6 V, the number of trapped electrons is found to be  $C_{\text{oxide}}V/q$  with  $C_{\text{oxide}}$  as the geometrical capacitance of the oxide layer. This implies a density of traps for the electrons at the polymer-metal oxide interface larger than  $3 \times 10^{17} \text{ m}^{-2}$ .

© 2010 American Institute of Physics. [doi:10.1063/1.3520517]

Metal-insulator-semiconductor-metal diodes incorporating a metal-oxide layer as an insulator show nonvolatile resistive switching<sup>1-5</sup> and can be used to store information.<sup>6-8</sup> Switching is an intrinsic property of metal oxides,<sup>1,4,9</sup> the semiconductor acts as a current limiting series resistance.<sup>10,11</sup> Currently such bistable diodes are being considered as possible replacement for standard NAND flash solid state memories.<sup>12</sup> For the memory functionality to become active, usually an electroforming step is required. In this step, the diode is subjected to a high bias voltage,<sup>13</sup> leading to soft breakdown of the oxide.

The microscopic mechanism of this electroforming process is still unknown. In a previous study, we have shown that the  $J$ - $V$  characteristic shows hysteresis before forming, indicating deep trapping of charges.<sup>10</sup> Here we investigate this trapping further using the voltage step quasistatic capacitance-voltage (QSCV) method.<sup>14,15</sup> In QSCV, the differential charge ( $\Delta Q$ ) required to change the capacitor voltage by a step  $\Delta V$  is measured and the capacitance  $C$  is calculated according to  $C = \Delta Q / \Delta V$ . The QSCV method is ideally suited to investigate traps that fill quickly but empty slowly because it does not rely on steady-state alternating currents. Also the transient current associated with irreversible charging of a capacitor with empty deep traps can be analyzed. The method has been used to investigate metal-oxide-semiconductor (MOS) capacitors,<sup>15</sup> and here we use it to derive the location of traps and their density in metal-oxide polymer diodes.

The diodes consist of an aluminum bottom electrode on which a thin layer of aluminum oxide is sputtered. On top, a thin film of the organic semiconductor poly(spirofluorene)<sup>16</sup> is spin coated. The top electrode is made by vacuum sublimation of barium followed by aluminum. The nominally electron-only diodes with an active area of 9 mm<sup>2</sup> are encapsulated with a getter in order to maintain an oxygen and water free atmosphere. Previously, we have shown that the

diodes can be converted into bistable resistive switches in high yield after an electroforming process.<sup>10,17,18</sup> Electrical characterization was performed using an Agilent 4155C semiconductor analyzer. Positive bias is defined as the Ba/Al top electrode being charged negative.  $J$ - $V$  sweeps were recorded with 10 mV step and 40 ms integration time. In QSCV measurements, an integration time of 4 s and a step of 100 mV were used.

The electroforming process for a pristine Al/Al<sub>2</sub>O<sub>3</sub>/poly(spirofluorene)/Ba/Al diode is presented in Fig. 1(a). Here we show cyclic  $J$ - $V$  scans where the maximum bias is increased stepwise. The arrows indicate the direction of the voltage scans starting at 0 V, scanning forward and then backward to 0 V.<sup>10</sup>

We discern three stages in the electroforming process. In the first stage, for voltages in the range between 0 and 8 V, we observe a pronounced hysteresis in the current-voltage characteristics. In the forward scan, the current increases with bias. However, in the backward scan the current is negligible. Actually the current level on the return scan is approximately equal to the displacement current associated

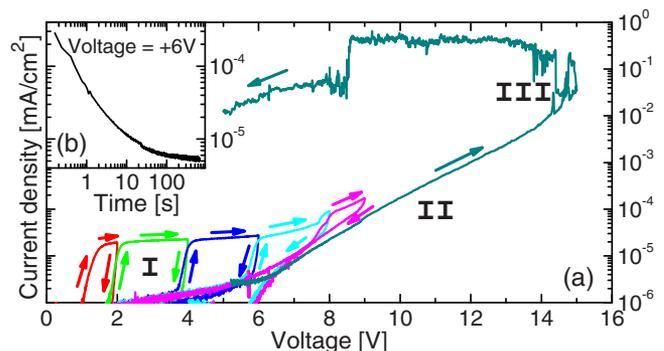


FIG. 1. (Color online) (a) Sequential current density-voltage characteristics of a pristine Al/Al<sub>2</sub>O<sub>3</sub> (20 nm)/polymer (50 nm)/Ba/Al diode. (b) Current density as a function of time upon application of a voltage step from 0 to 6 V at time  $t$  equal to zero.

<sup>a)</sup>Electronic mail: s.c.j.meskers@tue.nl.

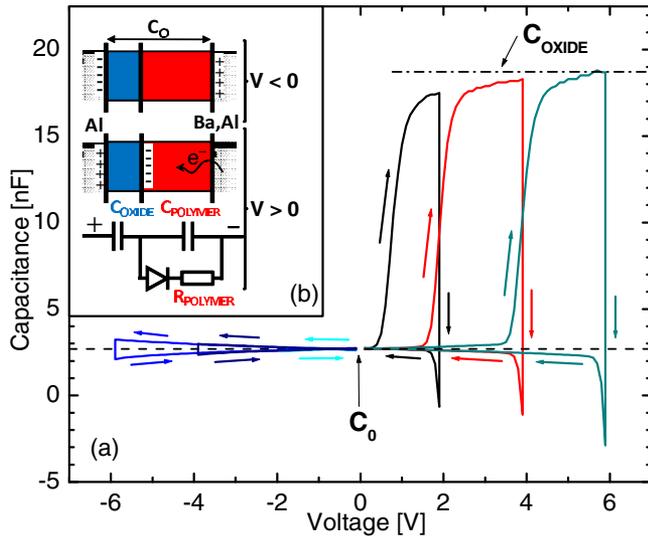


FIG. 2. (Color online) (a) Quasistatic capacitance-voltage characteristic of a pristine Al/Al<sub>2</sub>O<sub>3</sub> (40 nm)/polymer (80 nm)/Ba/Al diode. (b) Schematic representation of the diode and equivalent circuit. For negative bias voltage  $V$ , no charge is injected into the polymer. Both oxide and polymer act as insulators. For positive bias, electrons are injected into the polymer and trapped near the oxide-polymer interface.

with the device geometrical capacitance  $C_0$ , assuming that both oxide and polymer layer are insulators. If the subsequent  $J$ - $V$  loop is recorded using the same bias conditions, the hysteresis is not present and the measured current equals the displacement current. Then, scanning forward to a higher bias voltage that has not been applied before, the current shows a large increase. Backward scans give the same low current value and are independent of the previous scans. The original hysteresis loops are only restored after resting for a few hours. The hysteresis strongly depends on the scanning speed and is only observed when charging the top Ba/Al electrode negatively. Figure 1(b) shows the electrical current as a function of time, applying a bias step from 0 to 6 V. In the first 10 s after the bias step, the current decreases sharply and approaches an asymptotic value, interpreted as residual leakage current. The leakage is more than an order of magnitude smaller than the initial charging current. This behavior suggests that the observed hysteresis results from traps that fill in a time scale of seconds but empty slowly, on a time scale of hours.

In the second stage of electroforming, for biases from 8 to 14 V, the amount of hysteresis decreases with increasing bias. The magnitude and voltage dependence of the current can be tentatively modeled as being due to Fowler-Nordheim tunneling through the oxide<sup>19</sup> using a barrier height of approximately 1 eV and assuming a potential drop over the oxide layer equal to the applied bias. In the third stage of electroforming, occurring at biases larger than 14 V, a sharp and irreversible increase of the current density is observed, indicative of soft breakdown. The resistance of the diode is now bistable and can be switched reversibly between a high and a low level.<sup>10</sup>

The hysteresis observed in the first stage of forming can be studied in more detail using the QSCV method. Figure 2(a) shows cyclic  $C$ - $V$  scans under the same bias conditions as for the  $J$ - $V$  scans. Scanning in the reverse bias ( $V < 0$ ), a practically constant capacitance of 2.7 nF is recorded which

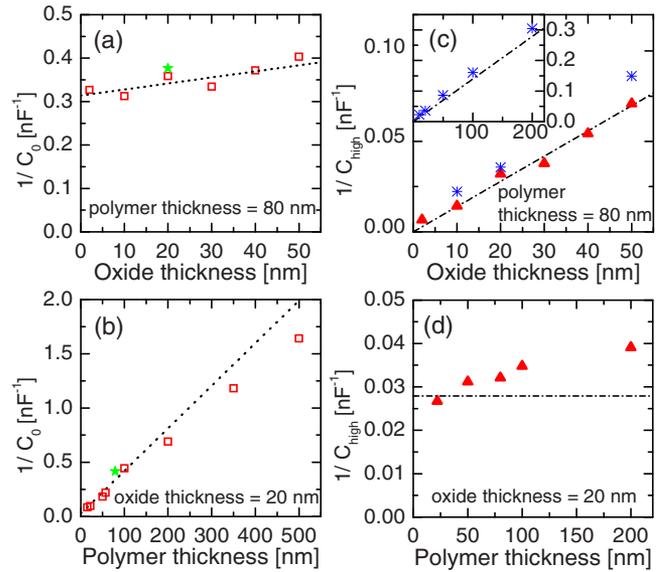


FIG. 3. (Color online) Capacitance for Al/Al<sub>2</sub>O<sub>3</sub>/polymer/Ba/Al diodes.  $1/C_0$  ( $\square$ ) as a function of (a) thickness of the oxide layer at constant thickness of polyfluorene layer (80 nm) and (b) thickness of the polyfluorene layer at constant oxide thickness (20 nm).  $1/C_{\text{high}}$  ( $\blacktriangle$ ) as a function of (c) oxide thickness with 80 nm polymer and (d) polymer thickness with 20 nm oxide (20 nm). Star ( $\star$ ) in (a) and (b) represents  $C_0$  for a Al/Al<sub>2</sub>O<sub>3</sub> (20 nm)/poly(styrene) (79 nm)/Ba/Al. Stars ( $\ast$ ) in (c) show capacitance for Al/Al<sub>2</sub>O<sub>3</sub>/Ba/Al diodes without any polymer. The dashed lines in (a) and (b) represent the theoretical geometrical capacitance. Dashed-dotted lines in (c) and (d) represent the oxide capacitance  $C_{\text{oxide}}$ .

we interpret as the geometrical capacitance  $C_0$ . The hysteresis is due to a small leakage current.

In forward bias, we observe capacitances exceeding geometrical capacitance by an order of magnitude when scanning over a bias voltage range to which the diode has not been subjected before. In the first cyclic scan (0 V  $\rightarrow$  2 V  $\rightarrow$  0 V), scanning forward to 2 V, the capacitance reaches up to 17.5 nF. Scanning back from 2 to 0 V, we again find the geometrical capacitance  $C_0$ . In the next scan to higher bias, we first observe  $C_0$  up to 2 V, but at higher bias up to 4 V, the capacitance again rises sharply to 18 nF as before. The capacitance in the backward scan is again similar to  $C_0$ . In the third cyclic scan up to 6 V, a maximum in the capacitance of 18.5 nF is recorded at 6 V. The reciprocal value of this high capacitance,  $C_{\text{high}}$ , is plotted in Fig. 3(b). For voltages exceeding 6 V, leakage currents significantly affect the capacitance measurement. Systematic variation of the oxide and polymer thickness yields a set of  $C_0$  and  $C_{\text{high}}$  values whose reciprocal values are plotted in Fig. 3.

We consider the diode as a double-layer structure comprised of an oxide layer (with capacitance  $C_{\text{oxide}}$ ) in series with a polymer layer ( $C_{\text{polymer}}$ ). As expected, the experimental  $C_0$  for diodes, as obtained from QSCV near zero bias [Figs. 3(a) and 3(b)], can be modeled accurately by the relation  $1/C_0 = 1/C_{\text{oxide}} + 1/C_{\text{polymer}}$  using relative dielectric constants  $\epsilon_{\text{Al}_2\text{O}_3} = 9$  and  $\epsilon_{\text{polymer}} = 3.2$ .<sup>20</sup>  $1/C_0$  is weakly dependent on the oxide thickness [Fig. 3(a)], but strongly varies with polymer thickness [Fig. 3(b)], because  $C_{\text{oxide}}$  is much higher than  $C_{\text{polymer}}$ . In contrast, the high capacitance from QSCV,  $C_{\text{high}}$ , varies strongly with oxide thickness [Fig. 3(c)] but is virtually independent of polymer thickness [Fig. 3(d)]. Moreover,  $C_{\text{high}}$  is essentially the same as the capacitance measured with QSCV on devices without polymer layer, and

matches with the calculated  $C_{\text{oxide}}$  [Fig. 3(c)].

The equality  $C_{\text{high}}$  and  $C_{\text{oxide}}$  can be explained as follows. Under sufficient forward bias, electrons are injected via the Ba/Al electrode,<sup>16</sup> drift through the polymer, and get trapped at the polymer/oxide interface. Representing the bilayer by the equivalent circuit in Fig. 2(b), injection of mobile electrons lowers  $R_{\text{polymer}}$  sufficiently to shunt  $C_{\text{polymer}}$ , and raises the bilayer capacitance to  $C_{\text{oxide}}$ . Irreversible trapping of electrons at the interface, symbolized by the diode, explains why  $C_{\text{oxide}}$  is only observed with the QSCV method in the first instance that a particular forward bias is applied. For instance, in the return path of the cyclic QSCV scan, there is no discharging current because of the trapping and the two layers behave again as pure insulators with overall device capacitance  $C_0$ . In a second scan, new electrons can only be injected into the polymer when the bias voltage applied exceeds the built-in voltage resulting from the trapped electrons. Hence,  $C_{\text{oxide}}$  is observed only if the applied bias voltage exceeds the maximum voltage of the previous scan. Under negative bias, a high injection barrier prevents injection of holes into the polymer and the capacitance equals  $C_0$ .

From the observation that  $C_{\text{high}}$  matches with  $C_{\text{oxide}}$  for bias voltages up to 6 V [Fig. 3(c)], we conclude that the number of electrons stored at the oxide-polymer interface is determined by the capacitance of the oxide layer and the applied bias  $V_{\text{appl}}$ . This implies a density of trap states for electrons at the interface exceeding  $C_{\text{oxide}}V_{\text{appl}}/(Aq_e)=3 \times 10^{17} \text{ m}^{-2}$  with  $A$  as the surface area of the capacitor, and  $q_e$  as the electron charge using  $C_{\text{oxide}}=70 \text{ nF}$  as determined at 6 V for 10 nm oxide thickness. For very thick polymer layers,  $C_{\text{high}}$  is slightly smaller than  $C_{\text{oxide}}$  [Fig. 3(d)]. A possible explanation is that the carrier trapping becomes slow with respect to the integration time because of the long transit time of electrons across the thick polymer layer with low electron mobility. In a diode with a layer of insulating polystyrene instead of semiconducting poly(spirofluorene), we do not observe any hysteresis loops in either  $J$ - $V$  or  $C$ - $V$  scans, indicating that electron injection into this insulating polymer is not possible.

We conclude that in Al/Al<sub>2</sub>O<sub>3</sub>/poly(spirofluorene)/Ba/Al diodes, electrons injected through the Ba/Al electrode are trapped at the internal oxide-polymer interface in the first stage of forming. The chemical nature of the traps is still unknown, yet, phenomenologically, they behave as border traps known from MOS devices.<sup>21</sup> The trapping leads to a maximization of the potential drop over the oxide layer. This enhances tunneling currents through the oxide, stage two of

the electroforming. Trapping of electrons also brings the electric field in the oxide closer to the threshold for dielectric breakdown at relatively low applied bias voltage, thus promoting the final stage of electroforming.

The work forms part of the research program of the Dutch Polymer Institute (DPI), Project No. DPI 704. We gratefully acknowledge the financial support received from the Fundação para Ciência e Tecnologia (FCT) through the research Unit No. 631, Center of Electronics Optoelectronics and Telecommunications (CEOT). We thank Ton van den Biggelaar for preparing the devices and the financial support from the European Community Seventh Framework Programme FP7/2007-2013 (Project No. 212311), ONE-P.

<sup>1</sup>S. Karthäuser, B. Lüssem, M. Weides, M. Alba, A. Besmehn, R. Oligschlaeger, and R. Waser, *J. Appl. Phys.* **100**, 094504 (2006).

<sup>2</sup>R. Müller, J. Genoe, and P. Heremans, *Appl. Phys. Lett.* **95**, 133509 (2009).

<sup>3</sup>T. Chang, Y. Cheng, and P. Lee, *Appl. Phys. Lett.* **96**, 043309 (2010).

<sup>4</sup>T. Oyamada, H. Tanaka, K. Matsushige, H. Sasabe, and C. Adachi, *Appl. Phys. Lett.* **83**, 1252 (2003).

<sup>5</sup>B. Cho, S. Song, Y. Ji, and T. Lee, *Appl. Phys. Lett.* **97**, 063305 (2010).

<sup>6</sup>R. Waser, R. Dittmann, G. Staikov, and K. Szot, *Adv. Mater. (Weinheim, Ger.)* **21**, 2632 (2009).

<sup>7</sup>A. Sawa, *Mater. Today* **11**, 28 (2008).

<sup>8</sup>M. Lee, Y. Park, D. Suh, E. Lee, S. Seo, D. Kim, R. Jung, B. Kang, S. Ahn, C. Lee, D. Seo, Y. Cha, I. Yoo, J. Kim, and B. Park, *Adv. Mater. (Weinheim, Ger.)* **19**, 3919 (2007).

<sup>9</sup>J. G. Simmons and R. R. Verderber, *Proc. R. Soc. London, Ser. A* **301**, 77 (1967).

<sup>10</sup>F. Verbakel, S. C. J. Meskers, R. A. J. Janssen, H. L. Gomes, M. Cölle, M. Büchel, and D. M. de Leeuw, *Appl. Phys. Lett.* **91**, 192103 (2007).

<sup>11</sup>H. L. Gomes, A. R. V. Benvenho, D. M. de Leeuw, M. Cölle, P. Stallinga, F. Verbakel, and D. M. Taylor, *Org. Electron.* **9**, 119 (2008).

<sup>12</sup>J. Hutchby and M. Garner, Assessment of the Potential and Maturity of Selected Emerging Research Memory Technologies Workshop and ERD/ERM Working Group Meeting, 6–7 April 2010, p. 1 (ITRS Edition, 2010).

<sup>13</sup>T. W. Hickmott, *J. Appl. Phys.* **88**, 2805 (2000).

<sup>14</sup>T. J. Mego, *Rev. Sci. Instrum.* **57**, 2798 (1986).

<sup>15</sup>K. Ziegler and E. Klausmann, *Appl. Phys. Lett.* **26**, 400 (1975).

<sup>16</sup>S. L. M. van Mensfoort, J. Billen, S. I. E. Vulto, R. A. J. Janssen, and R. Coehoorn, *Phys. Rev. B* **80**, 033202 (2009).

<sup>17</sup>M. Cölle, M. Büchel, and D. M. de Leeuw, *Org. Electron.* **7**, 305 (2006).

<sup>18</sup>F. Verbakel, S. C. J. Meskers, R. A. J. Janssen, H. L. Gomes, A. J. van den Biggelaar, and D. M. de Leeuw, *Org. Electron.* **9**, 829 (2008).

<sup>19</sup>Y. L. Chiou, J. P. Gambino, and M. Mohammad, *Solid-State Electron.* **45**, 1787 (2001).

<sup>20</sup>S. L. M. van Mensfoort, S. I. E. Vulto, R. A. J. Janssen, and R. Coehoorn, *Phys. Rev. B* **78**, 085208 (2008).

<sup>21</sup>D. M. Fleetwood, M. R. Shaneyfelt, and J. R. Schwank, *Appl. Phys. Lett.* **64**, 1965 (1994).