A 30 to 44 GHz divide-by-2, quadrature, direct injection locked frequency divider for sliding-IF 60 GHz transceivers

A 30 to 44 GHz Divide-by-2, Quadrature, Direct Injection Locked Frequency Divider for Sliding-IF 60 GHz Transceivers

Hammad M. Cheema, Reza Mahmoudi, Arthur van Roermund

Department of Electrical Engineering, Mixed-signal Microelectronics group,
Eindhoven University of Technology, 5600 MB,
Eindhoven, The Netherlands

***Abstract*—This paper presents a wideband 40 GHz divide-by-2 quadrature injection locked frequency divider (Q-ILFD) as an enabling component for sliding-IF 60 GHz transceivers. The design incorporates direct injection topology and input power matching using interconnect inductances to enhance injection efficiency. This results in an excellent input sensitivity and a wide locking range. Fabricated in a 65nm bulk CMOS technology, the divider operates from 30.3 to 44 GHz (37% locking range) while consuming 9mW from a 1.2V supply. The measured phase noise is -131 dBc/Hz at 1-MHz offset whereas the phase error between I-Q outputs is less than 1.44°.**

Index Terms — Injection locked frequency divider, Direct injection, Frequency synthesizer, 60 GHz sliding-IF

I. INTRODUCTION

The availability of high f_T silicon IC technologies capable of operating at millimeter wave (mm-wave) frequencies and the extraordinary interest for high data rate (>1Gbps) applications has motivated research and development of 60 GHz transceivers in recent years. The 7 GHz of contiguous bandwidth available at 60 GHz, though very useful, poses circuit design challenges especially for components like VCOs, prescalers and PLLs in a direct conversion transceiver. Therefore, alternative synthesizer friendly architectures based on double-heterodyne, sliding-IF, low-IF and half-RF architectures are being investigated.

Conventionally, prescalers in frequency synthesizers were flip-flop based CML circuits [1]-[2]. However, these are difficult to design reliably for 60 GHz owing to large RC time constants of the devices which limit high frequency performance. On the other hand, injection locked frequency dividers can operate at very high frequencies but are inherently narrowband due to their LC-tanks. Fig.1 shows the system architecture of a sliding-IF 60 GHz transceiver. In this system, the RF signal is converted to baseband in two steps. The first mixing operation with the VCO transfers the RF signal from 60 GHz to 20 GHz. The second mixing using quadrature outputs from the prescaler down-converts the 20 GHz signal to baseband. This approach relaxes the synthesizer specifications and also avoids VCO pulling which is an issue for direct conversion architectures. In this paper, feasibility of ILFDs for 60 GHz sliding-IF transceivers is investigated by implementing a 40 GHz divide-by-2 quadrature ILFD. In addition, techniques to enhance locking range of the divider are proposed which yield good measured results.

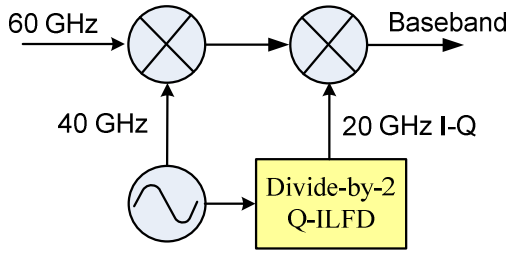

Figure 1. Quadrature ILFD usage in a sliding-IF 60 GHz receiver

Section II describes the circuit design of the ILFD, followed by a brief discussion, in section III, about layout and technology used. Section IV includes the measurement results and comparison with earlier published results and conclusions are drawn in section V.

II. THEORY AND CIRCUIT DESIGN

In conventional ILFD's the RF input signal is injected at the common-source node of the oscillator which is inherently running at double the fundamental frequency. However, the transistor parasitic capacitances at this node "eat-up" significant part of the high frequency injection signal. To counter this issue, shunt-peaking techniques have been utilized, albeit at the cost of extra chip area [3]. In contrast, the input signal, in this design, is directly injected across the tank which improves injection efficiency considerably, thus improving the locking range of the divider.

Majority of the published high frequency (above 30 GHz) ILFDs, either based on conventional [3] or direct-injection [4]

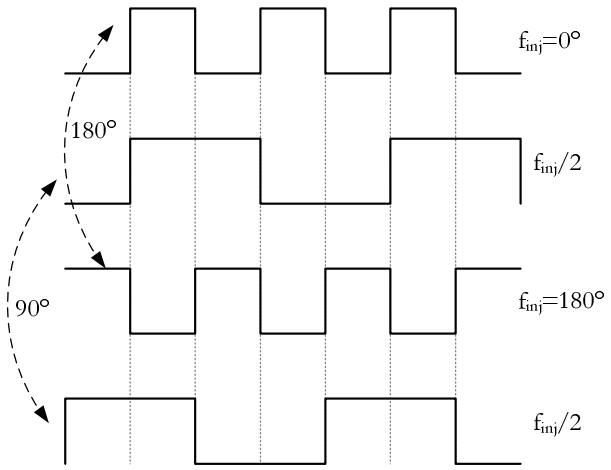

Figure 2. Operation princple for quadrature operation of an ILFD

topologies provide differential outputs only. Therefore, the need of quadrature outputs, especially for the system in Fig. 1, is naturally felt. One option is to employ a passive poly-phase filter after the ILFD to generate the quadrature outputs. This approach has two main drawbacks. Firstly, a power hungry buffer would be needed between the ILFD and filter to avoid loading affects and this would result in phase noise degradation. Secondly, variations in the RC values (in order of 15-25%) of the filter would require many tuning stages to achieve acceptable quadrature accuracy. An alternative to the poly-phase filter approach, used in this work, can be understood by Fig. 2 (square pulses are used for simplicity). It can be noted that a phase change of 180° at a frequency f_{inj} corresponds to a phase change of 90° at $f_{inj}/2$, as the signal width is double at the latter frequency. Therefore, using this concept at circuit level, the quadrature outputs can be obtained by injecting the differential (180° spaced) VCO outputs (or external injection signal) to two identical direct-injection ILFD stages. The differential injection achieved by using V_{inj}+ for one ILFD core and V_{inj}- for the second one also ensures perfect loading symmetry for the VCO outputs.

The concern which still remains is the accuracy of the I-Q outputs. Although, both ILFD stages can be designed and laid-out identically, still the relative PVT variations for one stage (or active/passive components) could be different from the other resulting in I-Q mismatch. To address this issue, the two ILFD stages are coupled to each other to force them to run in quadrature as shown in Fig. 3. The coupling, called parallel or anti-phase coupling, is achieved by connecting one ILFD output to the other ILFD with transistors M7-M10 in parallel to the cross coupled transistors M1, M2 and M4, M5. To understand the forced quadrature operation of this setup, it can be noted that each ILFD stage can be modeled as a gain stage. Also, for any oscillator structure with feedback, the loop phase must be 0° or 360°. Since the crossed connection (due to anti-phase coupling) between the ILFD's represent a phase shift of 180°, the two stages must have an additional phase shift of 180°. Hence, the phase shift across one stage is 90° ensuring quadrature operation.

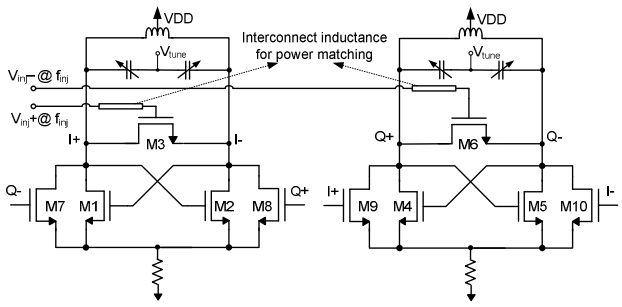

Figure 3. 40 GHz Q-ILFD circuit schematic

The Q-ILFD design is based on two identical free running oscillators, each formed by two NMOS transistors (M1-M2 & M5-M6) cross-coupled together to compensate the loss of the resonator. The inductors of the two ILFD stages are single turn, top-metal symmetric octagonal structures. The width of the metal trace is 9µm with an inner radius of 63µm. The guard-ring around the inductor is placed 10µm away from the signal trace and area of the inductor is 209x188 μm^2. The resulting inductance at 20 GHz is 310pH with a Q-factor of ~25. The varactors are accumulation MOS (AMOS) type and two of them are connected back-to-back to provide a common-mode node for tuning. To decrease the series resistance, the varactors are chosen to have multiple fingers. The width and length per finger is 2.1µm and 300nm respectively with 14 fingers in total. The resulting capacitance and Q-factor for a tuning voltage of 0 — 1.2V is 128 — 34fF and 5—18, respectively.

The dimensions of transistors M7-M10 determine the coupling strength between the two stages. If they are chosen too large, considerable parasitic capacitance is added to the tank. On the contrary, if they are chosen too small the coupling between the stages is weak and quadrature accuracy is degraded. Therefore, an optimized width of 7.5µm is chosen which is one-fourth of the cross-coupled transistors M1-M4 (30µm). The injection transistors M3 and M6 are 9µm wide with minimum channel length. The 150Ω poly-silicon based resistors in the tail node provide common-mode rejection and define the DC current through the ILFD. Differential common-source output buffers are employed for measurement purpose and matched to 50Ω environment.

The use of inductors makes it unavoidable to use long interconnects from the bond-pads to the injection transistors. As shown in Fig. 5, transmission lines are used where space is available, however, close to the core, the interconnect has to be an un-avoidable metal strip which in this case is ~78µm long. Due to capacitive input of the injection transistors, there is an inherent power mismatch between the gate input and the signal generator equipment. Consequently, at high frequencies, part of the injection signal is lost in the parasitic capacitance. A useful solution adopted in this work, is to utilize the required interconnect for power matching at the input of injection transistor. The interconnect is implemented as a micro-strip transmission line and shielded in a cavity-like structure (for isolation). Cadence parametric simulations are

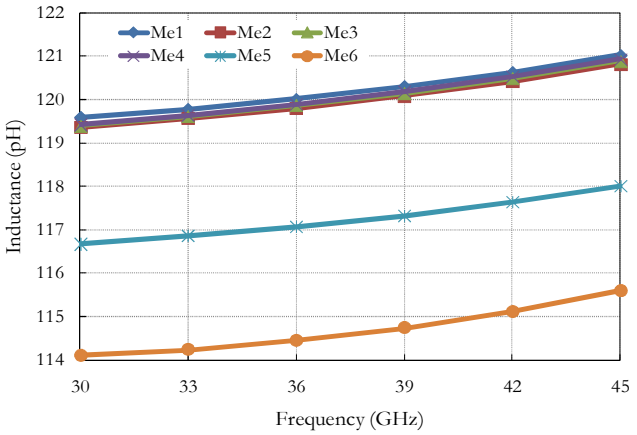

Figure 4. Inductance of a 2.5µm wide, 78µm long interconnect in different metal layers

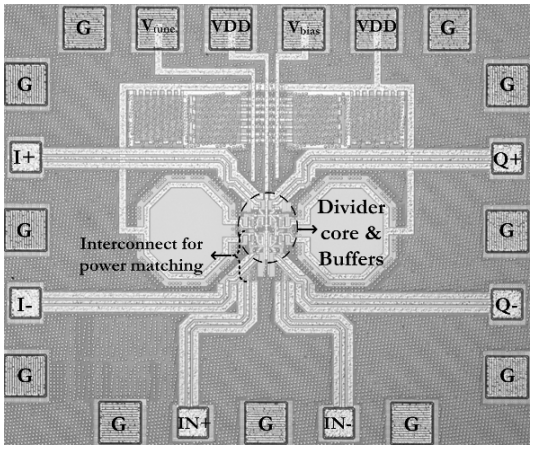

Figure 5. Die Micrograph of the 40 GHz Q-ILFD

used to determine the required inductance for maximum power matching. After optimization, EM simulations are done in ADS Momentum to determine the inductance per unit length for different metals in the technology stack as shown in Fig. 4. The metal layer Me3, which is closest to the required value is used for the interconnect layout. Due to this injection enhancement technique, input sensitivity is improved and for the same output power, the required input signal power is almost halved. This is proved by the measured low sensitivity discussed in section IV.

III. Layout and Technology

The layout of the divider is done carefully and compactly to reduce unnecessary parasitics. The RF signal paths between the tank and negative gm-cells are kept short and narrow lines are avoided to reduce resistive losses. The coupling transistors (M7-M10) are perfectly matched to ensure identical oscillation frequencies for both stages. In addition, ground meshing is used under the RF paths and decoupling capacitors are included for the voltage supplies. The differential input and outputs use 50Ω transmission lines (TLs) to the bond-pads. These TLs are coplanar waveguide based with lateral ground plane consisting of all metal layers "sandwiched" together using large number of vias, thus providing excellent noise isolation. The width of the signal path of the TL is 5µm and spacing from the ground plane is 4.22µm.

The dividers are fabricated in TSMC bulk CMOS 65nm LP (low-power) process having six metallization layers. The process offers MIM capacitors and poly-silicon resistors. The measured f_T of NMOS and PMOS transistors is 140 GHz and 80 GHz, respectively. As shown in Fig. 5, the area of the divider is bond-pad limited and occupies 900x750µm^2 in which the complete core is located between the two coils and occupies 80x100 µm^2.

IV. Measurement Results

The 40 GHz ILFD was measured on-wafer. The input 40 GHz signal from an Agilent signal generator is applied to a single-to-differential converter (180° hybrid) and then passed on the RF probe. The output differential signal is converted to single-ended using a similar hybrid and observed by an Agilent spectrum analyzer (E4446A). The phase noise is also measured by the spectrum analyzer.

The free-running frequency of the ILFD is first measured by switching "off" the injection signal. It starts oscillating at 1V supply whereas the maximum tuning range from 17 to 20.5 GHz is obtained with a 1.2 V supply. After fixing the tuning voltage of the varactor to a certain value, the injection signal is then switched "on" close to double the self-oscillating frequency for that particular V_{tune}. The input power is reduced to determine the minimum value for which the ILFD still locks to the input signal. Similarly, input sensitivity for different varactor tuning voltage is measured, three of which are plotted in Fig. 6. The ILFD can operate from 30.3GHz to 44 GHz (14 GHz or 37% locking range). The locking range for one tuning voltage is about 6 GHz, thus only three V_{tune} values are required to cover the complete operating range. The improved injection efficiency due to direct injection topology and input power matching technique, results in the required input power close to free-running frequency of the ILFD to be as low as -38 dBm. The simulated sensitivity curves are also plotted for reference and match closely to the measured curves. The low voltage operation of the ILFD is also verified by reducing the supply voltage. The divider can operate with a reduced supply of 1V resulting in a locking range of 8 GHz.

The phase noise of the ILFD is -131.6 dBc/Hz at 1-MHz from a 18.95 GHz output frequency (Fig. 7). The phase noise of the signal generator at double the frequency is -125 dBc/Hz which is close to the theoretical 6 dB difference due to frequency division. The phase noise variation over the complete operating range is $\pm$ 2.5 dB. The combined power consumption of the I-Q dividers is 9mW from a 1.2V supply. The output buffers used for measurement purpose consume 12mW. The locked spectrums at minimum and maximum operating frequencies are shown in Fig. 8. Due to usage of considerable number of cables (six in total), hybrids and needed connecters, considerable power loss is observed in the measured spectrum. However, after de-embedding these losses the output power of the ILFD is between -4 and -8 dBm. The I-Q phase error could not be measured reliably due to the absence of a stable trigger signal during oscilloscope measurements; however, post-layout simulations based on RC

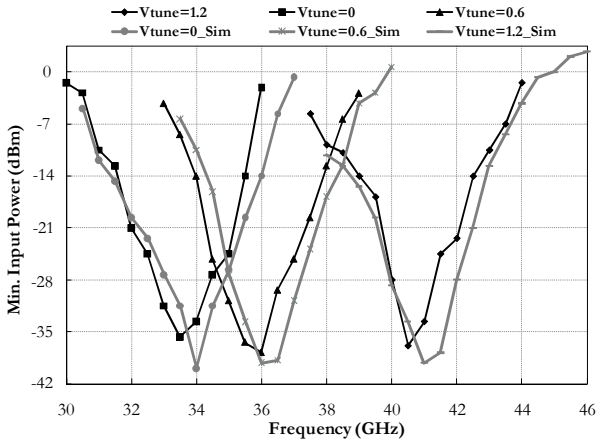

Figure 6. Input sensitivity curves of 40 GHz Q-ILFD

extraction demonstrate a phase error less than 1.44° over the complete locking range.

Table I shows a comparison of the presented frequency divider with published results. As frequency dividers with identical operating frequencies could not be found, the divide-by-2 Q-ILFD of this work is compared with ILFDs operating at higher and lower frequencies. It offers the second-highest locking range with lowest power of -2 dBm required at the locking range corners. Due to the input matching technique, the input power of -38 dBm is lower than the designs in [4-5][7]. As the only quadrature divider in the table, the power consumption is comparable to non-quadrature designs in [4]-[5]. The measured phase noise is also lower than all cited works in Table I.

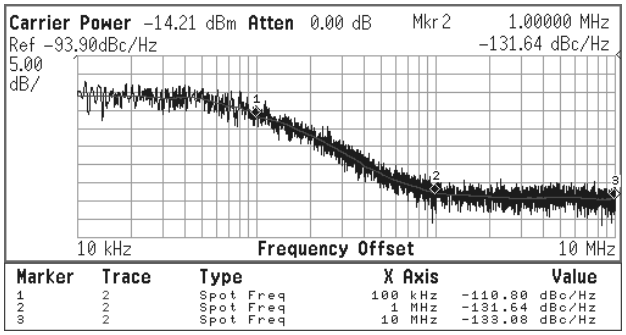

Figure 7. Phase noise for a 18.95 GHz divided output

V. CONCLUSIONS

We have presented a mm-wave quadrature injection locked frequency divider as an enabling component for a 60 GHz sliding-IF systems. The measured locking range of the ILFD is 14 GHz (37 %) while consuming 9 mW from a 1.2 V supply. The phase noise for a 18.95 GHz divided output is -131 dBc/Hz at 1 MHz offset. The minimum input injection power required is as low as -38 dBm. The low input sensitivity is achieved by employing direct injection and input power matching. The latter technique utilizes interconnect inductance to cancel the parasitic capacitance of the input injection transistor, thus no area or performance penalty is introduced.

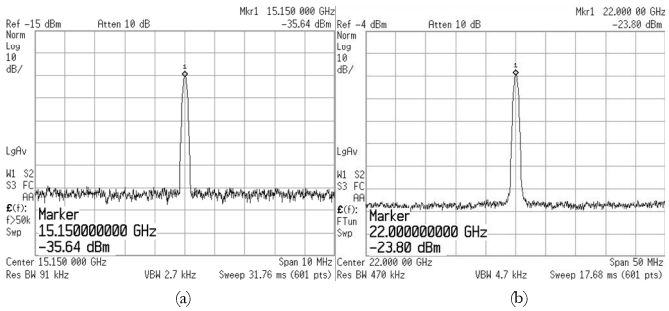

Figure 8. Output spectrum for (a) Min. input frequency (30.3 GHz) (a) Max. input frequency (44 GHz)

TABLE I. COMPARISON WITH PUBLISHED RESULTS

Ref	Process (nm)	Op. Freq (GHz)	L. R. (%)	Pin (dBm)	Power (mW)	Ph. Noise (dBc/Hz @ 1 MHz)
[4]	180	43 - 49	13	0	8	-120
[5]	130	50 - 62	21.42	0	10.8	-124.9
[6]	130	25 - 31.2	22	0	1.86	-130
[7]	90	35.7 - 54.9	42.3	5	0.8	-118.4
This work	65	30.3 - 44	36.9	-2	9*	-131.6
	* Total consumption including both I-Q divider					

ACKNOWLEDGMENT

The authors would like to thank Philips Research Eindhoven for technology access.

REFERENCES

[1] H. M. Cheema, R. Mahmoudi, M. A. T. Sanduleanu, and A. van Roermund, "A Ka Band, Static, MCML Frequency Divider, in Standard 90nm-CMOS LP for 60 GHz Applications," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, pp. 541-544, June 2008.

[2] Y. Mo, E. Skafidas, R. Evans, and I. Mareels, "50 GHz static frequency divider in 130 nm CMOS," *Electronics Letters*, vol. 44, no. 4, pp. 285-286, 2008.

[3] H. Wu, A. Hajimiri, "A 19GHz 0.5mW 0.35µm CMOS Frequency Divider with Shunt-Peaking Locking-Range Enhancement," *ISSCC Dig. Tech. Papers*, pp. 412-413, Feb., 2001.

[4] Yi-Jan Emery et.al.,"A Wide Operation Range CMOS Frequency Divider for 60 GHz Dual-Conversion Receiver," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC),* June 2006.

[5] Yu-Hang Wong, Wei-Heng Lin, Jeng-Han Tsai, Tian-Wei Huang, "A 50-to-62GHz Wide-Locking-Range CMOS Injection-Locked Frequency Divider with Transformer Feedback," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC),* pp. 435-438, June 2008.

[6] Hsien-Ku Chen, Da-Chiang Chang, Ying-Zhong Juang, Shey-Shi Lu, "A 30-GHz Wideband Low-Power CMOS Injection-Locked Frequency Divider for 60-GHz Wireless-LAN," *IEEE Microwave and Wireless Components Letters,* pp. 145-147, Feb. 2008.

[7] Tang -Nian Luo, Yi-Jan Emery et.al.,"A 0.8-mW 55-GHZ Dual-Injection-Locked CMOS Frequency Divider," *IEEE Transactions on Microwave Theory and Techniques,* vol. 56, no. 3, pp. 620-625, March 2008.