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Depletion-type thin-film transistors with a ferroelectric insulator

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We present a study of electrical characteristics of ferroelectric field-effect transistors made of PbZr0.2Ti0.8O3 and SnO2:Sb thin films. Due to properly chosen semiconductor parameters, the transistor channel can be totally depleted by the ferroelectric charge displacement. The observed remnant on/off ratio of the channel current amounts to $7 \times 10^7$. Pulse response measurements give information on data retention, device speed, and the occurrence of charge injection. The results lead to important design considerations for ferroelectric transistors. © 1997 American Institute of Physics. [S0003-6951(97)04204-6]

Recent years have shown an increasing effort in the development of electronic devices utilizing complex oxide thin films. From the point of view of physics and materials technology, one of the most challenging devices is the thin-film field-effect transistor with a ferroelectric insulator. Its non-volatile ferroelectric polarization, low programming voltage, and nondestructive readout make the ferroelectric transistor interesting for memory applications. Recently, considerable progress has been made with thin-film depletion-type transistors. However, total depletion of the semiconductor channel has not been achieved so far, resulting in a memory effect with a remnant on/off ratio close to unity. In this letter we report complete channel depletion in thin-film ferroelectric transistors made of PbZr0.2Ti0.8O3 and SnO2:Sb thin films, leading to an on/off ratio well in excess of $10^7$. In addition, we clarify important electronic constraints that apply to the design of ferroelectric transistors (semiconductor parameters, device speed, and maximum on/off ratio).

First we discuss the optimization of a transistor based on channel depletion, considering the semiconductor doping density and layer thickness. In the linear regime of operation the drain current in a field-effect transistor is given by

$$I_D = \mu \overline{Q} V_D W/L,$$

where $W$ and $L$ are the width and length of the semiconductor channel, respectively, $\mu$ is the charge mobility, and $\overline{Q}$ (units $C/cm^2$) is the areal charge density in the channel (the influence of interface states or contact resistance is neglected). When the transistor is operated, the modulation of the charge density in the channel results from the variation of the electrostatic potential at the semiconductor surface (band bending). Due to the memory effect in a ferroelectric transistor, the drain current can attain different values at zero gate voltage. At zero gate voltage we define two remnant states, namely the on-state of high drain current ($I_D^{on}$), and the off-state of low current ($I_D^{off}$). We would like to maximize the on-state current as well as the on/off ratio ($I_D^{on}/I_D^{off}$). For a given transistor geometry ($W/L$), carrier mobility, and drain voltage, the on-state current can be maximized by increasing the areal charge density in the channel. However, in order to be able to achieve total depletion of the channel in the off state, two constraints apply. First, $\overline{Q}$ should be smaller than or equal to the available remnant charge displacement of the ferroelectric material. Second, the band bending involved in totally depleting the semiconductor channel ($V_{bb}$) should not be so large as to cause depolarization of the ferroelectric layer. When the carrier concentration is determined by the dopant density $N_d$, $\overline{Q}$ and $V_{bb}$ are given by

$$\overline{Q} = e N_d t_s, \quad V_{bb} = \frac{e N_d}{2 \epsilon_0 \epsilon_r} t_s^2,$$

where $e$ is the electronic charge, $N_d$ is the dopant density, $t_s$ is the semiconductor layer thickness, and $\epsilon_r$ is the relative dielectric constant of the semiconductor. Fig. 1 serves to illustrate the implications for the range of values allowed for $N_d$ and $t_s$. As a realistic example, assume a transistor with a ferroelectric insulator having a remnant polarization of the order of $20 \mu C/cm^2$ and a coercive potential of 2 V. Lines of constant charge density and constant band bending are shown in Fig. 1. Complete semiconductor depletion can only be reached if the point with coordinates $t_s$ and $N_d$ is located on the left-bottom side of the indicated lines. Using practical layer thicknesses (larger than 5 nm) and dopant concentrations (larger than $\sim 10^{18} cm^{-3}$), we are left with a semiconductor parameter window that is roughly indicated by the shaded area. Note that our parameter window is limited by the coercive potential of the ferroelectric layer and not by the

![FIG. 1. Curves for a constant areal charge density of 20 $\mu C/cm^2$ and a constant band bending of 2 V [cf. Eq. (1), $\epsilon_r$=10], for a semiconductor thin film with carrier density $N_d$ and thickness $t_s$. The shaded area indicates the parameter window of practical interest for a transistor based on complete channel depletion; the dark triangle gives the maximum on-state channel conductance.](image-url)
SnO$_2$:Sb films were grown with a thickness of 10 nm and a dopant density of $4 \times 10^{19}$ cm$^{-3}$. These films have a sheet resistance of $2 \times 10^4$ $\Omega/\square$. Using $R_{\square}^{-1} = \phi \mu$ and Eq. (1), we deduce a charge mobility of 8 cm$^2$/Vs. Hall measurements yield similar values for the carrier mobility, while the measured field-effect mobility is of the order of 1 cm$^2$/Vs.

Panel (b1) of Fig. 2 shows the measured displaced areal charge density. The charge displacement shows a hysteresis behavior with a remnant charge density of 17 $\mu$C/cm$^2$ and a coercive voltage of 2.5 V. Hysteresis is observed in the transfer characteristic (panel b2) with the same sense of rotation; this proves that the memory effect is driven by the ferroelectric charge displacement. The gate leakage current ($I_G \leq 0.5$ nA) disturbs the transfer characteristic below $-3$ V. At zero gate voltage, the high-current on state and low-current off state are indicated in the figure. The on-state current is limited by the resistance of the source and drain contacts.

When varying the semiconductor parameters, different types of transfer characteristics are observed. Extreme cases (low and high sheet resistance) are shown in Fig. 3. Curve type (a) is observed for semiconductor films with a thickness above 10 nm. The transistors show a proper hysteresis, however with a low on/off ratio. This is due to the fact that the semiconductor film contains too much charge, so that total depletion cannot be reached. Curve (b) shows the maximum on/off ratio achieved at present. Curves of type (c) are observed for thin semiconductor films with a high sheet resistance (of the order of a M$\Omega/\square$ or larger). For these transistors, the hysteresis behavior is strongly reduced in the transfer characteristic as well as in the charge displacement curve. We attribute this behavior to an insufficient field sweep in the ferroelectric material. For negative gate voltages (channel depletion) the applied voltage essentially drops across the semiconductor channel instead of across the ferroelectric insulator; as a result, the ferroelectric material does not pass through a saturated loop, but effectuates a minor hysteresis loop with low coercivity. Instead of comparing the characteristics of different wafers under the same measurement conditions (cf. Fig. 3), one can also compare the characteristics of one sample for different conditions of data acquisition. Interestingly, we could weakly observe the same trends as shown in Fig. 3 by cooling down a sample to cryogenic temperatures [shift towards type (c) due to a loss of free carriers] or by exciting with radiation of sufficient energy [shift towards type (a) due to an increase of the free carrier density].

Fig. 4 demonstrates the memory retention of our transistors. We observe an increase of the off-state current and a decrease of the on-state current with time, i.e., converging time evolution curves. The off-state drain current increases by a factor of 1.6 every time decade; after a relaxation time of 3 h, the off-state drain current is still more than two orders of magnitude smaller than the on-state current. We attribute
where $D$, applied gate voltage, and $R$ to the required switching speed, described by Eq. \ref{eq:tau}.

In our devices the switched charge density is about $50 \, \mu C/cm^2$, the maximum off-state resistance equals the off-state resistance.

For applications, it is important to consider operational limitations of ferroelectric transistors. The maximum on-state channel conductance is given by $\mu \bar{W}L$. On the other hand, the minimum off-state conductance is related to the required switching speed, described by Eq. \ref{eq:tau}.

As a result, the on/off ratio is subject to the following upper limit:

$$\frac{I^{on}}{I^{off}} \leq \frac{\mu \bar{W}L}{\Delta \bar{Q}WL/V} = \frac{\mu \nu \tau}{R^2}.$$  \hspace{1cm} \text{(3)}

Here we assumed that $\bar{Q}$ equals $\Delta \bar{Q}$, which applies for a transistor based on total depletion. As an example, using a carrier mobility of $20 \, cm^2/V \cdot s$, and a switchable areal charge density of $50 \, \mu C/cm^2$, we find a maximum channel conductance of $1\, mS$ per square; using $L=1 \, \mu m$ and $V=2 \, V$, we find a maximum on/off ratio of $4 \times 10^5$ for $\tau=1 \, \mu s$, and a maximum on/off ratio of $40$ for $\tau=10 \, ns$. Clearly, the optimum design should be determined by the application envisaged.

In summary, we have fabricated ferroelectric transistors with different values of channel conductance, leading to strongly different transfer characteristics. The maximum remnant on/off ratio observed amounts to $7 \times 10^3$. The low off-state current is caused by total depletion of the semiconductor channel; the required band-bending potential is delivered by the coercivity of the ferroelectric charge displacement. Finally, the present study has clarified important design rules for depletion-type ferroelectric transistors.

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\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{fig4}
\caption{Time evolution of the drain current, recorded with $V_G=0.1 \, V$ and $V_G=0 \, V$. At $t=0$ a gate voltage pulse was applied, with an amplitude of $+6 \, V$ for the on state and $-6 \, V$ for the off state.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{fig5}
\caption{On-state and off-state current (a) as a function of pulse height for fixed pulse width, and (b) as a function of pulse width for constant pulse height; recorded with $V_G=0.1 \, V$ and $V_G=0 \, V$. Note that the current scales are equal.}
\end{figure}

\begin{thebibliography}{10}
\bibitem{1} Some device applications of oxide thin films are described in Mater. Res. Bull. 21, (1996).
\bibitem{6} When charge injection is the cause of the memory effect, the transfer characteristic has a sense of rotation opposite to the sense of rotation of the charge displacement. This is described in Refs. 7 and 8, for example.
\bibitem{9} Previously, large memory effects were reported in ferroelectric transistors with a bulk constituent, i.e., made of a semiconductor thin film on a ceramic ferroelectric substrate (e.g., Ref. 10) or made of a ferroelectric thin film on a crystalline Si substrate (e.g., Ref. 11). In all-thin-film ferroelectric transistors, memory effects were reported with a remnant on/off ratio slightly above unity (see Refs. 2 and 3) (note that we quoted the results of Watanabe incorrectly in our publication (Ref. 3)).
\end{thebibliography}