Average leakage current estimation of CMOS logic circuits

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José Pineda de Gyvez
Philips Research Labs
5656 AA Eindhoven
The Netherlands

Eric van de Wetering
Philips Semiconductors, MOS4YOU
6534 AE Nijmegen
The Netherlands

Abstract

In a product engineering environment there is a need to know quickly the average standby current of an IC for various combinations of power supply and temperature. We present two techniques to do this estimation without resorting to involved simulations. We use a bottom-up methodology that propagates the effect of process variations to higher levels of abstraction. In one approach, the leakage current of any given circuit is computed by adding up individual cell currents indexed from a statistically characterized library of standard cells. The second method is based on empirical formulae derived from results of the standard cell library characterization. In this approach the total leakage current is estimated without the need of any simulations and using only the circuit's equivalent cell-count. We present here the statistical foundation of our approach as well as experimental results on actual ICs.

1. Introduction

Leakage current levels in deep submicron circuits are high. This is due to the exponential behavior of the transistor's drain current in the subthreshold regime[1]. An estimation of this leakage current is not only necessary for Iddq testing purposes[2], but also for estimating the power consumption of circuits operating in standby mode, especially for those used in mobile applications[4]. In a product engineering environment there is a need to know in a quick way the average standby current of the circuit for various combinations of power supply and temperature. This information is used for instance to determine worst-case limits, to pre-condition the testing environment, to correlate the impact of process variability, etc. From a product engineering standpoint there is a need for accurate results without resorting to time consuming simulations. In this industrial environment the use of detailed VLSI circuit simulations could become a productivity bottleneck for the engineer who has to prepare the simulation setup of a complex chip with, say, multiple domain clocks, IP cores, memory, and 100 million transistors. Several approaches have been suggested in the literature to estimate the total leakage current of a circuit primarily under nominal conditions[4, 5]. Essentially, these works neglect the importance of within the wafer and wafer to wafer leakage current variations[6, 7]. To view the importance of process variations, Fig. 1(a) shows the simulated current of a 2-input NAND cell with input state 01 as a function of the threshold voltage difference (mismatch) of its NMOS transistors and taking into account process variability. Fig.1(b) in turn shows the corresponding distribution of the leakage current. Observe here the large current spread due to process variations! In summary, in this paper we present two statistical methods to estimate the average leakage current of a complex circuit addressing the concerns of computational speed and process variability.

2. Statistical Formulation

Let us model the current of a given cell as $I_{leak} = I_{leak}(X,s,p)$ where X is the cell type, s is the cell's input state and p is a random variable describing the variability of the process. From a statistical standpoint the average leakage current of a circuit can be calculated as follows

$$\langle I_{leak} \rangle = \sum_i \sum_j \mathrm{E}\left[I_{leak}(X_i, s_j, p)\right] \qquad (1)$$

where E[·] denotes the expected value of the cell's leakage current. Observe that I_{leak} is evaluated for every input state s_j of every cell X_i. Evaluating (1) requires a switch level simulator to investigate the input state of each cell[3]. This could be very time consuming especially for very large circuits. Rather than estimating the leakage current per input state, we compute an average leakage current for all possible inputs. Let us consider a cell X_i with input state s_j. Let the average and standard deviation of the leakage current for input state s_j be given as $\mu_{i,j}$ and $\sigma_{i,j}$, respectively. We denote the probability that the cell's input state is s_j as q_j, with $\sum_j q_j = 1$. Obviously, in a complex circuit different input states have different probabilities depending upon the cell's switching activity. Now, let us assume that we want to find the probability that the cell's leakage current is within the current interval $I_A < I_{leak} < I_B$. Without loss of generality assume the situation depicted in Fig. 2. Then, this probability is the probability that the cell is in input state s_j or s_{j+1} times the probability of finding the current in the desired interval for either of the input states. Considering that the input state of the cell is randomly distributed, the former can be expressed as

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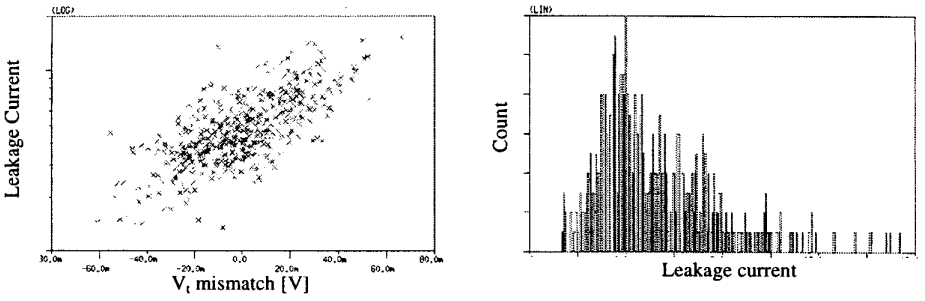

(a) (b)

Fig. 1. Effect of process variability on the leakage current of 2-input NAND with input state 01. (a) Leakage current vs. V_T mismatch. (b) Distribution of leakage current.

$$P(I_A < I < I_B) = \sum_j q_j \int_{I_A}^{I_B} f_{i,j}(I)dI \qquad (2)$$

where $f_{i,j}(\cdot)$ represents the p.d.f. of the leakage current of cell X_i for input state s_j. By interchanging the integral with the summation it is possible to interpret the integrand as a composite p.d.f. made up from the sum of individual p.d.f.'s, i.e. $f_i(I) = \sum_j q_j f_{i,j}(I)$. By doing so, we eliminate the dependence on the particular input state and move one level of abstraction higher, i.e. we compute now the equivalent leakage current at the cell level.

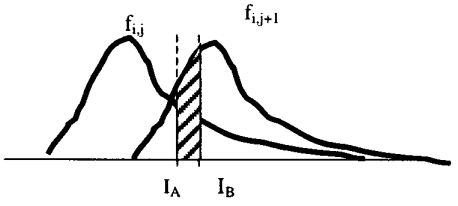

Fig. 2. Leakage current distributions of a cell, and probability of finding the cell's leakage current within an interval (I_A, I_B) for any two input states.

Rather than dealing with the p.d.f. itself it is more convenient to deal with its mean and standard deviation. As the cell's switching activity is not known in advance and since we will not perform an exhaustive switch level simulation, let us further assume that the probability of occurrence of each input state is the same, i.e. for N input states this probability is $1/N$. Then, from the definition of expected value we have

$$\begin{aligned}\mu_i &\equiv \int_{-\infty}^{+\infty} I \cdot f_i(I)dI \\ &= \int_{-\infty}^{+\infty} I \cdot \left(\frac{1}{N}\sum_j f_{i,j}(I)\right)dI \\ &= \frac{1}{N}\sum_j \int_{-\infty}^{+\infty} I \cdot f_{i,j}(I)dI = \frac{1}{N}\sum_j \mu_{i,j}\end{aligned} \qquad (3)$$

This simply states that the mean μ_I of the cell-level p.d.f. is the weighted sum of state-dependent means. Similarly, from the definition of variance we have that

$$\begin{aligned}\sigma_i^2 &\equiv E[I^2] - E^2[I] \\ &= \int_{-\infty}^{+\infty} I^2 f_i(I)dI - \left[\int_{-\infty}^{+\infty} I\ f_i(I)dI\right]^2 \\ &= \int_{-\infty}^{+\infty} I^2 \frac{1}{N}\sum_j f_{i,j}(I)dI - \left[\frac{1}{N}\sum_j \mu_{i,j}\right]^2\end{aligned} \qquad (4)$$

Noting that

$$\sigma_{i,j}^2 \equiv \int_{-\infty}^{+\infty} I^2 f_{i,j}(I)dI - \mu_{i,j}^2 \qquad (5)$$

and leaving the integral term alone, then by substituting (5) in (4) we have that the cell's variance is given as

$$\sigma_i^2 = \sigma_{mi}^2 + \frac{1}{N}\sum_j \sigma_{i,j}^2 \qquad (6)$$

where σ_{mi}^2 denotes the variance of the mean for cell i

$$\sigma_{mi}^2 \equiv \frac{1}{N}\sum_j \mu_{i,j}^2 - \left[\frac{1}{N}\sum_j \mu_{i,j}\right]^2 \qquad (7)$$

This is an interesting result because it takes into account the spread due to the different (means of) input-states as well as the spread of the leakage current distribution for each input-state. In summary, an equivalent current spread at the cell level can now be estimated. With the results obtained in (3) and (6) we can redefine (1) to predict the average leakage current of a complex circuit by adding up the means of the current of every cell

$$I_S = \sum_i \mu_i \qquad (8)$$

Estimating the spread of the leakage current of a complex circuit requires investigating the correlation among cells. Since the total leakage current of a circuit is computed by adding up the current of each cell, the variance of the total leakage current can be expressed as

$$\sigma_S^2 = \sum_i \sigma_i^2 + 2\sum_{i<k} r_{ik}\sigma_i\sigma_k \qquad (9)$$

where r_{ik} is the correlation coefficient of any two cells i and k. Assuming a common correlation factor $r_{ik} = r$ for all pairs of cells, and using the identity

$$\left[\sum_i \sigma_i\right]^2 = \sum_i \sigma_i^2 + 2\sum_{i<k} \sigma_i \sigma_k \qquad (10)$$

the next simplified expression for the total variance of the circuit leakage current can be derived

$$\sigma_S^2 = (1-r)\cdot \sum_i \sigma_i^2 + r \cdot \left[\sum_i \sigma_i\right]^2 \qquad (11)$$

Typically the correlation among adjacent cells is high, in the order of 0.8. The difference from cell to cell lies primarily due to intra-die variability.

3. Bottom-Up Statistical Average-Iddq Estimation

The general flow of our approach is outlined next.

Step 1. Transistor-level statistical simulations per cell i and per input state j to capture the effect of process variations and to obtain $\mu_{i,j}$ and σ_{ij}.

Step 2. Computation of the equivalent mean current μ_i and spread σ_i per cell.

Step 3. Summation of the equivalent mean current and spread for all cells in the circuit.

Steps 1 and 2 are typically applied once to characterize an entire library of cells. This is usually done every time there is a new technology release or every time that the library is updated. Once every cell is characterized, computing the total leakage current of any circuit is done by applying Step 3.

Notice that the average $\mu_{i,j}$ and variance $\sigma_{i,j}$ of the leakage current per cell X_i and per input state s_j can be obtained through Monte Carlo simulations. At Philips we have a statistical circuit simulator that can simulate intra-die, inter-die or simultaneously both types of process variations[8]. Fig. 3 shows an example of these statistical simulation results for an AND of three inputs. The equivalent mean current μ_i per cell is obtained numerically from (3). Finally, the total current of a circuit is obtained by indexing every cell type in the library of cells, retrieving the equivalent mean current and adding up this current to make up the circuit's total leakage current.

To understand the pervasiveness of process variability it is worth taking a closer look at the results shown in Fig. 3. In general, we can see that the predicted nominal current is about 20% lower than the one taking into account both inter and intra-die variations. Also, notice that for most input states, except states 100 101 110, the leakage current taking into account both inter and intra-die variations is lower than the one simulated only with inter-die variations. This stems from the fact that the cell benefited from local variability that yielded a lower than average total leakage current. Similar trends were observed in [2].

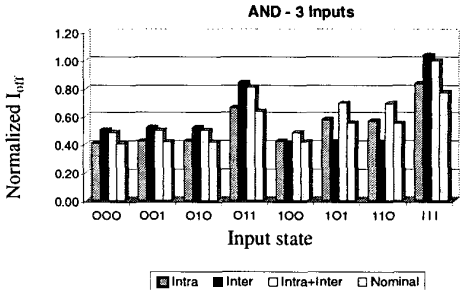

Fig. 3. Leakage current of a 3-input AND cell. Histogram shows the nominal current and the ones calculated due to process variability.

4. Standard-Cell Library Characterization

Fig. 4 shows partial characterization results of a CMOS 0.25μm standard cell library. The histogram shows the number of standard cell types having a specific normalized equivalent quiescent current relative to its total number of transistors. The transistor-level statistical simulations were carried out at 32°C and taking into account both intra and inter-die variations. Furthermore, this normalization yields a partitioning of cells based on their leakage current properties. The properties and differences from group to group lies in the current driving capability of the cell. While it is not possible to have a spatial correlation among cells because their placement in the layout is not known in advance, cells in a group have a correlated behavior with respect to their leakage current, e.g. the same equivalent transistor width, the same gain or β factor, etc.

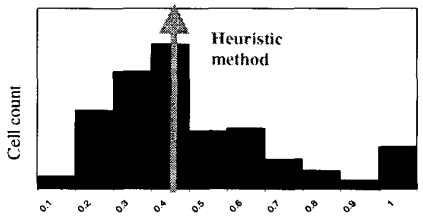

Fig. 4. Classification of library of cells into groups of leakage current per transistor.

5. Heuristic Fast Average-Iddq Estimation

Within Philips an empirical model developed by P. van de Wiel and P. Janssen is commonly used for a fast raw-prediction of the leakage current[9]. This model assumes that all cells in a complex circuit belong to either of two

classes: 2-input NANDs and NORs. The virtual NAND class describes the leakage for N transistors and the NOR class the one of P transistors. Furthermore, the model assumes that one can compute an equivalent transistor width for each class and that one of the stacked transistors is on and the other off. Thus, dividing the total number of transistors by 4 we have an equivalent cell count and the assumption made is that half of the cell count goes into each class. The sum of both equivalent leakage currents I_N and I_P gives the total circuit's leakage current. The previous can be formulated as follows

$$I_H = \frac{\#transistors}{4}\left(\frac{I_N}{2}+\frac{I_P}{2}\right) = N_{EQ}I_L \quad (12)$$

where N_{EQ} and I_L are the equivalent cell count and mean leakage current, respectively. Although the original model has an empirical basis, we found that to have a good prediction (compared to the cell method), the leakage current per transistor of these two NAND and NOR cells has to be aligned with the group that has the largest count of cells in the characterized library. In our case this corresponds to a current in group 0.4, see Fig. 4. Fig. 5 shows the leakage current predicted by both the heuristic and the statistical methods for a large set of standard cells. One can see that except for a few cells, there is a very good agreement between both approaches. In general the accuracy of the heuristic approach depends very much on what cell types are used in the actual circuit. For instance, looking at Fig. 4, if the majority of the cells of a given circuit fall in group 1, then the predicted average current will be off by a factor of approximately 2.5. On the other hand, if the majority of the cells belong to the 0.4 group, the error will be negligible.

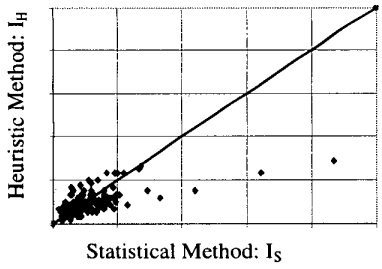

Fig. 5. Comparison of leakage current prediction by both heuristic and statistical approaches for a set of about 200 different cells.

Let us estimate now the accuracy of the heuristic approach. For the analysis consider that we have N_T transistors in N_G cells, i.e. $N_T = kN_G$ where k is just a proportionality factor. Further, assume that all cells in the circuit belong to one class only. Therefore, the total current obtained from the statistical approach can simply be computed as $I_S = N_G\mu$ where μ is the equivalent leakage current of that class. This yields the following formulation for the ratio of the leakage current calculated by both methods

$$\frac{I_H}{I_S} = \frac{N_{EQ}I_L}{N_G\mu} = \frac{k}{4}\frac{I_L}{\mu} \quad (13)$$

Let us further assume that the current calculated from the statistical approach is a multiple factor of the heuristic one, e.g. $\mu = nI_L$, then we have

$$\frac{I_H}{I_S} = \frac{k}{4n} \quad (14)$$

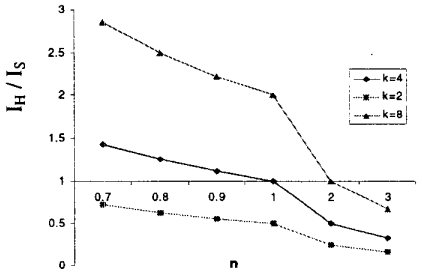

Fig. 6. Accuracy of the heuristic vs. the statistical approach. n represents the worst case current ratio, k indicates the average number of transistors per cell.

From (14) we see that essentially there are two sources of inaccuracies. One is due to the average number of transistors per cell relative to the fixed number of transistors in the heuristic approach, e.g. k/4, and the other is due to the ratio between the chosen average current of the heuristic approach, I_L, and the worst case scenario of the circuit's actual current, i.e. $\mu = nI_L$. Fig. 6 shows plots of (14) for various values of k and n. From this figure we can expect the worst case prediction to be off by a factor of 3.

6. Experimental Results

We now show in detail the analysis of three identical DSP modules implemented in a 0.25µm CMOS technology and integrated into one single chip. Each module has about 39000 cells with 198 different cell types. Fig. 7 shows the (3x)combined Iddq measurements

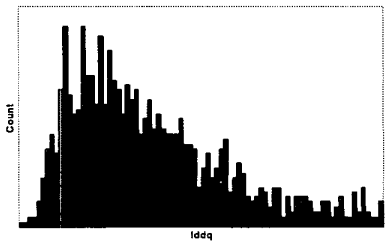

Fig. 7. Combined Iddq measurements of three identical DSP modules.

obtained from 1223 screened devices.

Fig. 8 shows the cumulative distribution of each cell's contribution to the total average-Iddq current. The horizontal axis shows the number of cell types, the left vertical axis shows the cumulative contribution of each cell type to the total leakage current, and the right vertical axis the contribution of each cell type to the total current.

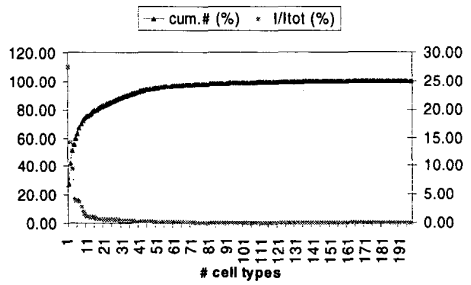

Fig. 8. Cumulative Distribution of the total leakage current.

From this figure we can see that about 56 out of 198 types contribute 95% of the total current. Furthermore, only a few of the cell types have a significant current contribution, e.g. there is one cell type that contributes 28% of the total current. This scenario is typical of actual ICs, e.g. there is a preference in the use of cells.

Application of the statistical approach to the three DSPs matched the experimental results within 3%, while the heuristic approach was within 11%. The good result agreement between both methods is due to the fact that the DSPs use cells whose predicted current is about the same as for the statistical one, see Fig. 9.

A deeper analysis into the DSP module shows that the gross of the current comes from the group that has the majority of the cells. Since we aligned the heuristic current per transistor with this group, the current prediction is good. Fig. 10 shows plots with these observations. The left axis shows the number of cells per

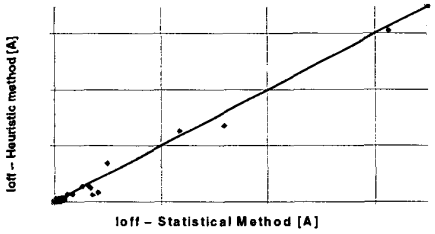

Fig. 9. Comparison for the expected cell's leakage current contribution to the total leakage of one DSP

group, the right axis shows the group's current contribution to the total current.

7. Conclusions

We have presented two methods, suitable for a product engineering environment, to estimate the average leakage current of a circuit taking into account the variability of the semiconductor process.. One of the methods is based on a circuit's "inventory" of cells to add up the individual cell's current to the circuit's total current. The other method makes use of an empirical formula and does not require any simulations. Both methods show a very good agreement with actual experimental results.

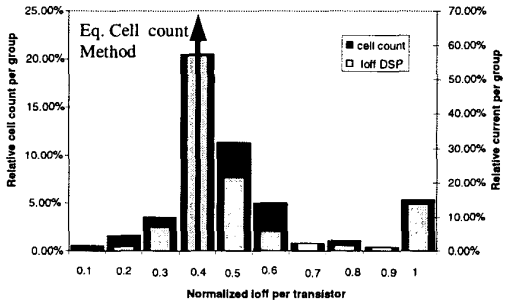

Fig. 10. Comparison of one DSP-module's leakage current per group of the library of cells.

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