RDC Converter for Battery Buffered Fast EV Charging

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RDC CONVERTER FOR BATTERY-BUFFERED FAST EV CHARGING

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CONTENTS

ABSTRACT

Current fast EV charging is facing challenges due to grid insufficiency and high operation costs. A battery-buffered fast EV charging is a possible solution to provide high charging power regardless of grid insufficiency. Besides, it can also reduce the operation costs of a fast-charging station. However, an additional DC/DC converter is needed for such a battery-buffered EV charging system. The efficiency of the state-of-the-art DC/ DC converter is limited to about 97%. The DC/DC converter wastes lots of energy and needs an additional cooling system.

The reduced dissipation converter (RDC) converter using partial power processing idea is then proposed. It can significantly increase the efficiency and reduce the cost of the DC/DC conversion subsystem. Several DC/DC topologies have been analyzed. To provide sufficient regulation for wide voltage variations of electric vehicles, a multi-level DC/DC topology is proposed to provide wide voltage regulation as well as maintain partial power processing.

Regarding the efficiency and power density of the proposed topology in the RDC converter, a hardware optimization method is analyzed and illustrated to find the optimal operating point. A constant current (CC) closed-loop control is designed and implemented in the RDC converter.

Finally, a 20 kW RDC prototype has been built in the lab. Experiments show that the RDC converter can achieve 99.4% efficiency and about 5 kW/L power density. In addition, the output current ripple of the RDC converter is about 4% (less than 5% in CCS and CHAdeMO standards). The designed control system works stably at the steady state. The dynamic response experiments show that the control system performs well on overshot and tracking time.

Keywords: Fast EV charging; Battery-buffered charging; Partial Power Processing; Multilevel converter; Constant current control.

Table of Abbreviations/Symbols

Abbreviations/Symbols	Description
RDC	Reduced Dissipation Converter
EV	Electric Vehicle
BESS	Battery Energy Storage System
AC	Alternating Current
DC	Direct Current
MV	Medium Voltage
LV	Low Voltage
B1	Battery One
B2	Battery Two
PWM	Pulse Width Modulation
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
SOC	State of Charge
NMC	Nickel Manganese Cobalt
LFP	Lithium Iron Phosphate
CC	Constant-current
CV	Constant-voltage
PI	Proportion and Integral
MCU	Microcontroller Unit
P_{B2}	Direct Power from B2
P_{EV}	Total Power to the Electric Vehicle
P_{RDC}	Partial Power Processed by the RDC Converter
RMS	Root-mean-square
L_1	Main Inductor
L_2	Second Inductor
C	Output Capacitor
L_{f1}	Input inductor of the input filter for B1
L_{f2}	Input inductor of the input filter for B2
C_{f1}	Input capacitor of the input filter for B1
C_{f2}	Input capacitor of the input filter for B2
S1	Power Switch 1
S2	Power Switch 2
S3	Power Switch 3
S4	Power Switch 4
f_{sw}	Switching Frequency
T_{sw}	Switching Period
f_s	Sampling Frequency
T_s	Sampling Period
v_{B1}	Real-time value of the voltage of B1
V_{B1}	DC value of the voltage of B1

Abbreviations/Symbols	Description
$\hat{v}_{B1}$	Small signal of the voltage of B1
v_{B2}	Real-time value of the voltage of B2
V_{B2}	DC value of the voltage of B2
$\hat{v}_{B2}$	The small signal of the voltage of B2
v_{EV}	The voltage of the electric vehicle
V_{EV}	The average voltage of the electric vehicle
$\hat{v}_{EV}$	The small signal of the voltage of the electric vehicle
v_a	Mid-point voltage of the leg a in the full-bridge
v_b	Mid-point voltage of the leg b in the full-bridge
V_a	The DC value of v_a
V_b	The DC value of v_b
D	The duty cycle (big signal)
v_1	The output voltage of the RDC converter
V_1	The DC value of the output voltage of the RDC converter
i_1	The inductor L1 current
Δi_1	The peak-to-peak ripple current of the inductor L1 current
I_1	The average value of the L1 current
i_2	The inductor L2 current
I_2	The average value of the L2 current
i_{EV}	The electric vehicle current
I_{EV}	The average value of the electric vehicle's current
v_s	The switching voltage across S2
v_L	The voltage on the inductor L1
Ap	Area product of magnetic cores
i_{s1}	The current of the switch S1
i_{s2}	The current of the switch S2
i_c	The current of the output capacitor C
v_c	The voltage of the output capacitor C
ESR	Equivalent series capacitance of the output capacitor
DCR	DC resistance of the inductor
$DCR1$	DC resistance of the inductor L1
$DCR2$	DC resistance of the inductor L2
P_{con}	Conduction loss of power MOSFETs
R_{dson}	On-resistance of power MOSFETs
I_{RMS}	The root-mean-square value of the conducting current
$I_{RMS_{S1}}$	The root-mean-square value of the current i_{s1}
$I_{RMS_{S2}}$	The root-mean-square value of the current i_{s2}
$P_{S1_{con}}$	The conduction losses of S1
$P_{S2_{con}}$	The conduction losses of S2
V_{GS}	Gate-to-source voltage of MOSFETs
I_{DS}	The drain-to-source current of MOSFETs
V_{DS}	The drain-to-source voltage of MOSFETs

Abbreviations/Symbols	Description
V_{TH}	The turn-on threshold voltage of MOSFETs
V_{PL}	The Miller-plateau voltage of MOSFETs
$E_{on_{s1}}$	The turn-on energy loss of S1
$E_{off_{s1}}$	The turn-off energy loss of S2
$P_{S1_{sw}}$	The switching losses of S1
dT	Dead time
G1	Gate drive signals for S1
G2	Gate drive signals for S2
$P_{S2_{DT}}$	The body diode loss during the dead time of S2
P_{rr}	The body diode reverse recovery loss
V_{SD}	The conducting forward voltage of the body diode
Q_{rr}	The reverse recovery charge of the body diode
$P_{S2_{sw}}$	The transient losses of S2
α	The temperature coefficient on resistance of copper
T_j	The junction temperature of MOSFETs
P_{loss}	The total loss of a MOSFET
A_c	The cross-section area of the magnetic core
l_c	The length of the core
g	The length of the air gap
Φ	The total magnetic flux in the core
A_w	The core window winding area
MLT	The mean length per turn of the core
B_{sat}	The saturation magnetic flux density of the magnetic core
μ_r	The initial permeability of magnetic material
I_p	The peak current of the inductor L1 current
B_{max}	The maximum flux density in the magnetic core
k_u	The window winding utilization factor of the magnetic core
I_{rms}	The RMS current in the winding
J_{rms}	The current density in the winding
A_{con}	The conductor cross-section area of the Litz wire
u_{opt}	The optimal effective permeability
K_i	The ratio of I_{rms}/I_p
μ_0	The permeability of the free space
P_{cu}	The winding loss (copper loss) of the inductor L1
ρ_w	The resistivity of the conductor (copper)
g_m	The optimal length of the air gap
A_L	The inductance per turn squared
N	The number of winding turns in the inductor L1
P_{DC}	The DC winding loss of the inductor L1
RMS_{AC}	The RMS value of AC current of the triangular ripple
P_{fe}	The core loss per unit volume

Abbreviations/Symbols	Description
ΔB	The peak-to-peak value of the alternating flux density
$P_{C_{loss}}$	The power loss of the capacitor ESR
I_{cRMS}	The RMS current flowing into the output capacitor C
P_{RDC}	The total converter loss
P_{ind}	The total inductor loss
$P_{S3_{con}}$	The conduction loss of S3
P_{all}	The total calculated loss of the RDC converter
v_{ab}	The output voltage generated by the switching network
V_c	The DC voltage on the output capacitor C
i_{HS}	The ripple current flowing into the high-side switch S1
i_{GND}	The ripple current flowing into the ground
i_{B1}	The ripple current flowing into B1
i_{B2}	The ripple current flowing into B2
i_{LS}	The ripple current flowing into the low-side switch S2
Δi_c	The peak-to-peak ripple capacitor current
ΔV_{cESR}	The additional voltage ripple by the ESR of the capacitor
V_{pp}	The total voltage ripple across the capacitor
T_c	The temperature of the case of the MOSFET
T_h	The temperature of the heatsink
T_a	The temperature of the ambient
R_{jc}	The thermal resistance of from the junction to the case
R_{ch}	The thermal resistance of the thermal pad
R_{ha}	The thermal resistance of the heatsink
Q	The total loss of dissipation
v_{pi}	The control output signal of the controller
$\hat{v}_{pi}$	The small signal of the control output signal
V_{pi}	The DC value of the control output signal
I_{ref}	The control reference current
d	The real-time duty cycle
$\hat{d}$	The small signal of the duty cycle
v_{tri}	The triangular carrier waveform
V_{tri}	The magnitude of the triangular carrier waveform
$\hat{v}_{ab}$	The small signal of the switching network output voltage v_{ab}
V_{ab}	The DC value of the switching network output voltage v_{ab}
$G_{pwm}(s)$	The transfer function of the PWM module
$G_{iv}(s)$	The transfer function of the LCL filter from the $v_{ab}(s)$ to $i_1(s)$
$G_{vd1}(s)$	The transfer function from $\hat{d}(s)$ to $\hat{v}_{ab}(s)$ under mode 1
$G_{vd2}(s)$	The transfer function from $\hat{d}(s)$ to $\hat{v}_{ab}(s)$ under mode 2
$G_{pi}(s)$	The transfer function of the PI controller
$G_{op1}(s)$	The open loop gain of the RDC converter under mode 1
$G_{op2}(s)$	The open loop gain of the RDC converter under mode 2

Abbreviations/Symbols	Description
f_r	The resonance frequency of the LCL filter
Z_C	The impedances of C
Z_{L1}	The impedances of L_1
Z_{L2}	The impedances of L_2
k_p	The proportion parameter of the PI controller
k_i	The integration parameter of the PI controller
f_c	The cross-over frequency
f_L	The frequency when the PI controller introduces 45^0 delay
Z_s	The output impedance of a power supply with a filter
Z_{in}	The input impedance of the converter under control
Z_{f2}	The impedance of the input filter at B2
$Z_{L_{f2}}$	The impedance of L_{f2} of the input filter at B2
$Z_{C_{f2}}$	The impedance of C_{f2} of the input filter at B2
$\hat{v}_{in}(s)$	The input voltage of the RDC converter, see Fig.4.17
$\hat{i}_{in}(s)$	The input current of the RDC converter, see Fig.4.17
$G_{iv_{EV}}(s)$	The transfer function from $\hat{v}_{EV}(s)$ to $\hat{i}(s)$
$Z_{in\_op}(s)$	The open-loop input impedance of the RDC converter
$G_{iv_{in}}(s)$	The transfer function from $\hat{v}_{in}(s)$ to $\hat{i}(s)$
$G_{iv_{B2}}(s)$	The transfer function from $\hat{v}_{B2}(s)$ to $\hat{i}(s)$
$G_{id}(s)$	The transfer function from $\hat{d}(s)$ to $\hat{i}(s)$
$Z_{in\_}cl(s)$	The closed-loop input impedance of the RDC converter
R_{dc}	DC resistance of the winding
R_{ac}	AC resistance of the winding

1. INTRODUCTION

1.1 Business Case

1.1.1 Motivation

The slow available rates of electric vehicle (EV) charging are an obstacle to the wide adoption of EVs. Typical battery capacities and the associated maximum allowed charging powers are summarized in Table 1.1. These maximum charging powers are specified by the car manufacturers. However, it is often the case that there is not a local charger available at this high-power rate. The technology is there to provide higher power chargers – but these are not readily available (see below). A typical home charger with a power of 7.2 kW (@220V, 35 A) takes 5-14 hours to replenish an EV's battery. This is much slower than refilling a gasoline tank: our goal is to make EV charging comparable with gasoline refilling without incurring very high costs often associated with high-power chargers. This will be discussed later.

Table 1.1: Battery capacity and charging time of a home charger [1]

Model	Battery Capacity (kWh)	Maximum charging power (kW)	Charging time (hr) (home charger)
Volkswagen(e-golf)	36	40	5
Mercedes	85	110	12
Audi (e-torn)	95	265	>13
Tesla (Model 3)	102	150	>14

In addition, the average battery capacity is estimated to grow fast in the coming 10 years, from 66.5 kWh to 100 kWh [2]. Thus, the future charging time of EVs with slow home chargers will be even longer. This makes the 7.2 kW home charger unacceptable in the future.

Thus, fast charging is urgently needed for the wide adoption of EVs and to make it competitive with gasoline refilling [3]. Now, EV owners often do not know that they will encounter a fast charger within the more limited travel distance of an EV – so-called "range anxiety". The current challenges for fast charging are summarized below.

- The fast chargers are not easily available for EV drives. The ultimate goal is to make fast-charging stations easily accessible like gas stations.
- The grid capacity is not sufficient for wide adoption of fast charging. This will be discussed in detail later.

- The operation cost of a fast-charging station is currently very high (charged by the utilities), due to the peak power demand from the grid.

The current situation of fast charging is illustrated in detail regarding to the above-mentioned three aspects below.

1.1.2 Current Situation

1） Current fast chargers

Nonetheless, there are currently a range of chargers available on the market. First of all, we summarize the current categories and then proceed to describe current state-of-the-art high-power chargers. Table 1.2 summarizes the current definitions of AC slow and DC fast chargers (>22 kW) and the associated charging time to 60 kWh of different types of chargers.

AC slow chargers require on-board AC/DC rectifiers, the power rates of which are limited to 7.2 kW, due to the space limits and safety requirements of EVs. DC fast chargers are further categorized into DC fast chargers (22-100 kW), DC super-fast chargers (100-250 kW), and DC ultra-fast chargers (>250 kW), according to the power rating level. A typical 50 kW DC fast charger and a typical 150 kW DC super-fast charger (as described in Table 1.2) can accomplish the same task in 75 and 25 minutes respectively. Recently introduced DC ultra-fast chargers (350 kW) reduce the refilling time to about 10 minutes, which makes it much more comparable with gasoline refilling.

Table 1.2 Definitions and time to 60 kWh of different types of chargers [3]

Parameters	**AC Slow Chargers**		**DC Fast Charger**	**DC Super-Fast**	**DC Ultra-Fast**
	Level 1	Level 2	22-100 kW	100-250 kW	>250 kW
Typical Power /kW	1.4	7.2	50	150	350
Time to 60 kWh /mins	2400	500	75	25	10

Such high-end chargers are, however, by no means generally available on a geographical basis from an EV owners' perspective. The reasons for this are twofold:

- The high operation cost of these systems prohibits the charging service providers from rolling out fast chargers.
- The current grid infrastructure is not able to support the power provision required.

We will return to these restrictions later. For now, we note that fast charging is not widely publicly accessible due to the restrictions mentioned above. We now describe some of these regional limitations.

2） Low public accessibility

Now there is a significant lack of publicly accessible high-power chargers in the Netherlands. Not only is the number of fast chargers too small to satisfy the wide adoption of EVs but also the power rating of currently available fast chargers is limited.

In the Netherlands, the number of public chargers has grown quickly in the past five years, leading in Europe with more than 100,000 slow chargers by 2022. However, only ca. 3% of chargers have a capability of over 22 kW charging (fast chargers) [4], as shown in Fig.1.1.

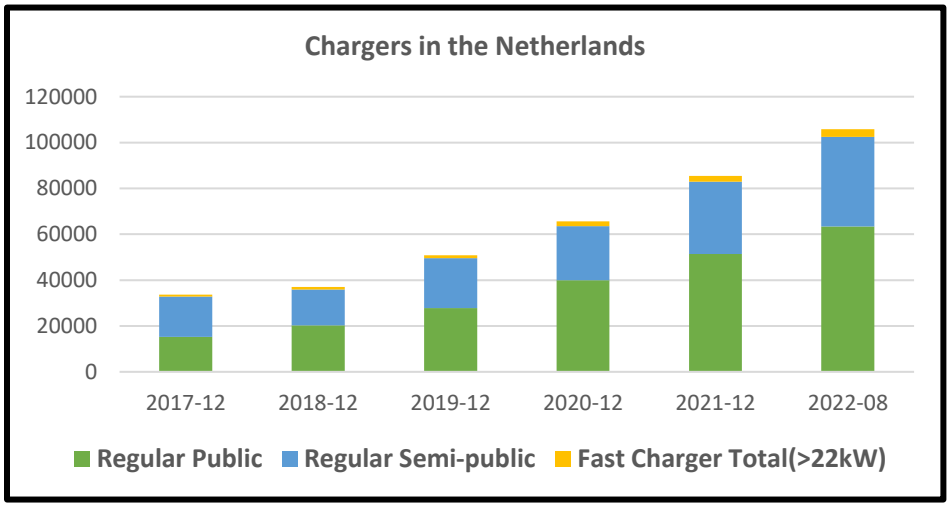


Figure 1.1: Public chargers in the Netherlands by 2022 [4].

The definition of "fast" charging as anything > 22 kW is very arbitrary. It takes nearly 3 hours to replenish a 60-kWh battery with a 22-kW charger, which is definitely not comparable with gasoline refilling. As shown in Table 1.2, a 150-kW fast charger can recharge an EV's battery up to 80% of state-of-charge (SOC) in about 25 minutes, but there are very few stations with this capability in the Netherlands. According to IDTechEx [5], in 2022, only 19% of total fast chargers have a capability of >100 kW charging globally, we can roughly estimate that the number of >100kW fast chargers is only 0.6% of total public chargers and DC fast chargers (power rating >100 kW) will double to 44% of total fast chargers (>22 kW) in 2032 [5].

Overall, both the number of fast chargers and power rating are limited and need to be developed for a growing EV charging market. Furthermore, governments are implementing policies to drive fast charging to higher power levels and larger numbers.

- Germany requires that all gas stations offer EV charging [6] and that the fast charging provides sustained 200 kW charging for two vehicles simultaneously.
- USA provides a $5 billion program aimed at a minimum of four 150kW+ chargers every 50 miles along major transportation routes [7].

To conclude, the fast EV charging market is underdeveloped and it indicates mega-trends towards much higher-power fast chargers (>100 kW) in the coming years.

1.1.3 Restrictions and Challenges

As we have discussed in the above section, though fast chargers up to 350 kW are available on the market, fast charging is not actually widely rolled out. There are two major challenges: distribution network limitations and high operational costs [1].

1） Distribution Network Limitations

Charging multiple EVs simultaneously requires extremely high peak power from the distribution grid. This can impact the distribution systems, including system stability and voltage imbalances [8], especially in areas where a strong grid is not accessible, such as highways between cities and rural areas.

Fig. 1.2 shows the most common configuration of the current electric grid to provide a fast-charging station with sustainable electricity. The electricity, generated from a power plant, goes through transmission lines to sub-stations, and sub-stations usually step down the high voltage to medium voltage (6kV-21 kV AC). Distribution lines transfer the electricity to charging stations, and distribution transformers step down the medium voltage to a lower voltage (480V AC). Fast chargers convert the 480V AC to the desired DC power for EVs.

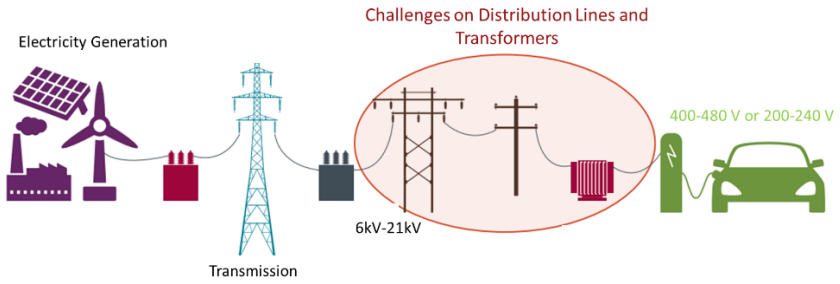


Figure 1.2: Technical challenges on distribution systems of conventional fast charging

Research shows that current distribution systems cannot sustain such a high peak power demand extracted by fast chargers, therefore most of them need to be updated globally [9].

High instantaneous power demand can result in economic issues, including large capital investments to upgrade distribution systems [10] and large monthly operational bills. Table 1.3 summarizes some of the estimated capital investment for upgrading distribution systems per charger in the US, UK, and EU. For example, in the EU, a 150-kW fast charger needs 150,000 dollars to build up.

Table 1.3 Estimated capital investment to upgrade distribution systems

Locations	Charger power	Grid Upgrade cost/charger
Ottawa, US	150 kW	$6 K-$15 K
UK (National Grid)	350 kW	$20 K- $40 K
EU (Mckinsey [10])	>150 kW	$150 K in total

There are two elements here. Grid upgrading is extremely expensive in rural areas and in addition, takes time. One way to address this problem is to have local energy storage systems for fast chargers. This will be discussed in Section 1.2.

2）High Peak Demand Charge

Large monthly operational costs due to high peak demand can make EVs fast charging very expensive [11], and EV drivers may pay a lot more than home chargers.

In a monthly billing period, apart from the electric energy consumption cost, measured in cost per kilowatts-hours ($/kWh), a peak demand charge is charged by utility companies to non-residential customers, including charging stations, for the compensation of the potential deterioration of electricity grid, including power plants, power lines, transformers.

The demand charge is a fee based on the highest rate, measured in cost per kilowatts ($/kW), at which electricity is drawn during any 15- to 30-minute interval in a monthly billing period. It is calculated by $Demand\ charge = peak\ power\ used(kW) \times rate(\$/kW)$, regardless of how often you hit your peak demand–whether it's for five minutes or five hours per day.

According to the National Renewable Energy Lab (NREL), in the U.S., the demand charge rate can range from $2/kW to $90/kW [12]. This depends on the states and regions of charging sites, utility providers, tariffs, etc. Paradoxically, it tends to be higher in states where EVs are more popular, such as California, Massachusetts, and New York. They tend to be higher along the highway and countryside roads, at which the DC fast charging stations are the most needed, i.e., between cities, due to weak grid connections.

Let us assume the following for comparison where two 150 kW charging points are available at a retail point.

- Electricity energy charge = $0.1 per kWh
- Demand charge = $6 per kW

Scenario A: *2 EVs charge separately for 20 mins/day.* This corresponds to a transfer of 100 kWh in a day. The highest rate at which energy is drawn is 150 kW. The operation cost in a month (30 days) is calculated as follows:

- Consumption: 100 kWh*30*0.1 $/kWh=300$
- Demand: 150kW*6 $/kW=900 $

Scenario B: *2 EVs charge simultaneously for 20 mins/day.* In this case, the consumption is the same as in scenario A. But the highest rate (peak power) increases to 300 kW, so the associated demand charge increases to 1800 $ - double that in scenario A.

The monthly bills of the two different scenarios are summarized in Fig.1.3. For the same amount of kWh used- at the same consumption cost level, Scenario B costs significantly more. Demand charges account for a significant fraction of consumers' electric bills and can make EV-charging stations unprofitable.

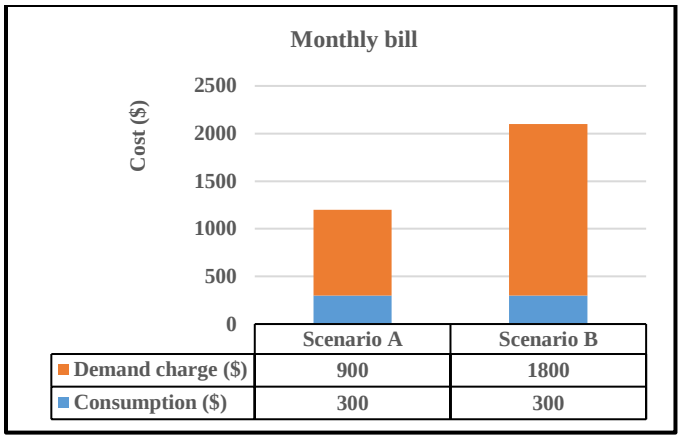


Figure 1.3: Operational cost comparison of two scenarios in a monthly bill

As long as coincidental charging happens, this high-demand charge bill cannot be avoided. Some smart charging techniques and IoT can help arrange the charging events to avoid simultaneous charging. However, when the fleet of EVs expands in the near future, coincident charging can always happen, so as to cause a high monthly bill, which then needs to be passed on to the EV drivers. Currently, most DC super-fast charging stations are now losing money.[13]

The work in this Eng.D. is concerned with developing a novel battery-buffered DC fast charging station to address the aforementioned challenges. With such a battery energy storage system (BESS), high peak power demand from the grid can be significantly reduced. Thus, large investments in grid upgrading can be avoided and operational costs can be reduced. This will be discussed further in Section 1.2. First of all, we need to describe the current state of the art for high-power chargers – this forms our technology base case on which we wish to build.

1.2 Technology Base Case

As we have discussed above, conventional fast EV charging requires very high peak power directly from the grid. On one hand, this requires a costly upgrade for the current distribution networks. It takes a long time to upgrade the distribution networks, which could slow down the wide adoption of EVs due to the charging inconvenience. On the other hand, conventional fast EV charging results in very high operational costs as we have demonstrated in the previous section. Most of the current fast charging stations are now losing money. Recently, a battery energy storage system (BESS) buffered fast EV charging solution has been proposed to provide very high-power charging to EVs, while reducing the direct high peak power from the grid, to solve the mentioned challenges.

1.2.1 Conventional DC Fast Chargers

The state-of-the-art DC fast chargers convert the three-phase AC voltage up to 480 V into the desired DC voltage by the galvanic transformer and power electronics-conversion stages, including an AC/DC rectification stage [1]. The basic configuration of the conventional DC fast charger is shown in Fig.1.4. A transformer steps down the medium AC voltage (6-21 kV) to low AC voltage (480V). The AC/DC power converter transforms the AC power to the desired DC power for EV batteries. Usually, multiple identical AC/DC modules are connected in parallel to increase the output power, so as to reduce EV charging time. As shown in Fig.1.4, this DC fast charger directly connects to the grid when charging an EV. Though high-power AC/DC converters can be designed, the local grid and transformer may not have such a high capacity to provide peak power.

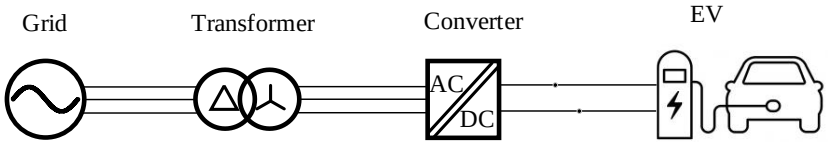


Figure 1.4: Basic structure of conventional DC fast chargers (on-grid)

Table 1.4 summarizes some of the conventional DC fast chargers on the market. These DC fast chargers can reduce typical charging time to around 10 minutes, which can provide EV drivers with satisfactory charging speed. For example, the Tesla Supercharger V3 can provide 250 kW charging power. The time to refill a 60-kWh battery is reduced to about 14 minutes.

However, as explained, these chargers directly extract extremely high power from the grid. They thus need strong grid connections and associated capital investments to upgrade the local grid, especially in rural areas and along highways between cities.

Table 1.4: Some of the best commercial fast chargers worldwide

Manufacturer	Model	Power(kW)	Time to 60kWh	Peak Efficiency
SIEMENS	SICHARGE D	160-300	12 mins	95.5%
EFACEC	HV 350 G2	350 (2*175)	10 mins	95%
ABB	TERRA HP GEN3	175-350	15 mins	95%
BENY	480 kW DC	480	7.5 mins	95%
TESLA	Supercharger V3	250	14 min	91%

Moreover, as we have seen, high-peak-power charging from the grid can cause an extremely high electricity bill from utilities, especially when coincident charging happens in the charging station, as discussed above.

1.2.2 Battery Buffered Charging.

Battery-buffered charging [14] is a possible solution to tackle the challenges of high peak power availability. This is known as a battery energy storage system (BESS) integrated fast charging. The basic configuration of a state-of-the-art battery-buffered charging station is illustrated in Fig.1.5.

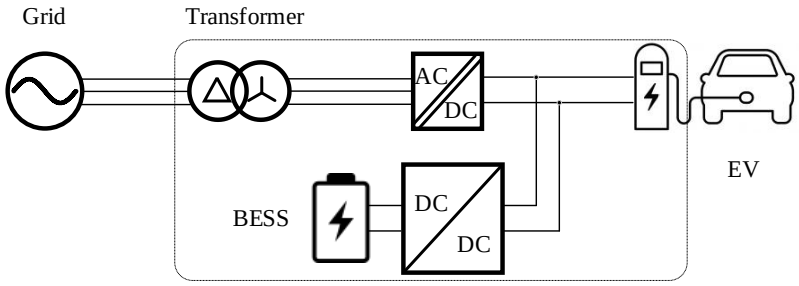


Figure 1.5: State-of-the-art BESS buffered fast charging station.

Like Fig.1.4, an AC/DC converter connects to the transformer and grid, directly providing DC power to EVs. A battery (BESS) buffered charger, with an additional battery and a DC/DC converter, can provide extra instantaneous high DC power to EVs reducing grid requirements. The working principles are illustrated as follows:

1) When there are no EVs charging in the station, the grid will continuously charge the BESS with a relatively low power. Such a low power rating depends on the capability of local distribution networks: e.g. 20-50 kW.
2) When EVs come into the station, the BESS will provide very high power (> 150 kW) through a DC/DC converter to the EVs. The charging power can be further increased with simultaneous use of the on-grid AC/DC converter. This further reduces the charging time.

Overall, with a BESS installed in a charging station, the grid recharges the BESS at the low-power level (20-50 kW), while the BESS can charge EVs at a power level larger than 150 kW.

Since the battery-buffered charging system only requires relatively low power from the grid, the grid does not need to be upgraded. In addition, the associated capital investment can be avoided, and operational costs can be reduced due to the reduced peak power from the grid.

Some recently introduced BESS buffered DC fast chargers are summarized in Table 1.5. Current battery-buffered DC fast chargers can provide up to 2*150 kW (Volkswagen) power to

EVs while requiring 7-40 kW from the grid. This represents a solution to solve the grid challenges mentioned above.

Table 1.5: Current models of DC fast chargers integrated with BESS

Manufacturer	Model	BESS Capacity	Recharge power	Power	Time to 60kWh
DU_POWER	AFC-200D	193.5kWh	7-40 kW	2*120 kW	30 mins
Volkswagen-E.ON	E.ON Drive Booster	193.5kWh	20 kW	2*150 kW	24 mins
Phillips 66 & Freewire	Boost Charger 150	160 kWh	27 kW	2*75kW	48 mins

However, current BESS buffered DC fast chargers still need a high power (up to 150 kW) DC/DC converter to charge EVs and recharge the BESS. This requires considerable additional capital investments for the DC/DC converter. Besides, lots of energy will be wasted due to the efficiency limitation of the DC/DC converter. Taken Volkswagen-E.ON [15] as an example, the current efficiency of the additional DC/DC converter is about 97%.

1.2.3 The Proposed RDC Concept

The RDC concept, shown in Fig. 1.6, is proposed to improve the efficiency and reduce the cost of the additional DC/DC converter. Different from the conventional DC/DC converter (handle full power >150 kW) connected in parallel between BESS and EVs, as shown in Fig.1.5, the proposed RDC converter is connected in series between the local BESS and the EV.

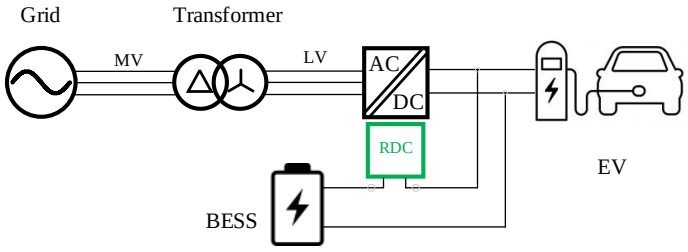


Figure 1.6: The proposed RDC concept of DC fast charger integrating BESS

With such a configuration, the RDC converter only handles the voltage difference between the BESS and EVs and controls the output current to support EV charging. Therefore, the RDC converter only processes the partial charging power instead of the conventional DC/DC converter which handles full charging power. Most of the power will flow directly from the BESS to EVs with nearly 100% efficiency.

Since the RDC converter only handles a small portion of the charging power, the converter losses (which cannot be avoided) can be significantly reduced, so as to increase the

total charging efficiency. Furthermore, given the fact that the converter cost is closely correlated to the power it processes, the cost of the RDC converter can be significantly reduced.

Overall, the proposed RDC converter is to further increase the efficiency and reduce the cost of such a battery-buffered EV charging system. This development supports the wide adoption of fast EV charging (>150 kW), which can accelerate the process to a net-zero goal in the Netherlands and worldwide. The detailed configuration of the RDC converter will be discussed in Section 2.

1.3 Structure of the Report

This study is organized as follows: Section II discusses the possible topologies for the RDC concept and their working principles. Section III investigates the hardware design and implementation of the RDC converter with the proposed topology. Section IV introduces the dynamic model of the RDC converter and its control method. Section V describes the laboratory setup and summarizes the key experimental results. Possible future works are summarized in Section VI.

2. TOPOLOGY INVESTIGATION

As discussed in the above section, the RDC converter is connected in series between BESS and EV. Fig. 2.1 illustrates the detailed implementation of the RDC converter. The local buffering battery (BESS) is split into two units, B1 and B2, and the input of a DC/DC converter is connected to the B1. The output of the DC/DC converter is connected in series between B2 and EV.

Though BESS is split into two units, these two units are integrated in the same location. By fully utilizing the local BESS in such a way, the DC/DC converter can achieve extremely high efficiency, which will be discussed below.

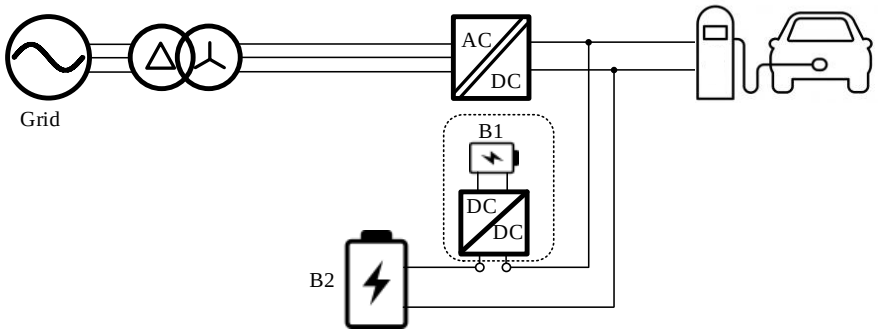


Figure 2.1: Implementation of RDC concept with a DC/DC converter

Take the buck converter as the example of a DC/DC converter, one possible implementation is shown in Fig. 2.2.

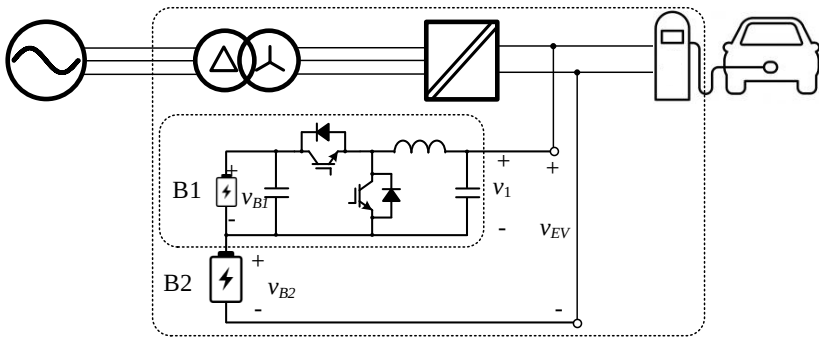


Figure 2.2: RDC converter using Buck Topology

In Fig. 2.2, the output voltages of B1 and B2 are v_{B1} and v_{B2}, respectively. v_1 is the output voltage of the RDC converter, which can be regulated by the RDC converter with B1. This will be discussed in Section 2.1. The EV battery voltage is v_{EV}, and the charging current is i_{EV}. According to Kirchhoff Voltage Law (KVL), we have

$$v_1 + v_{B2} = v_{EV} \tag{2.1}$$

Multiply charging current i_{EV} at both sides of equation (2.1), we get

$$\underbrace{v_1 \cdot i_{EV}}_{P_{RDC}} + \underbrace{v_{B2} \cdot i_{EV}}_{P_{B2}} = \underbrace{v_{EV} \cdot i_{EV}}_{P_{EV}} \tag{2.2}$$

As seen in equation (2.2), the RDC converter only processes a small portion of total charging power (P_{RDC}), while most of the power P_{B2} flows directly from B2 to EV. Thus, the power rating of the RDC converter is significantly reduced so is its cost.

2.1 Buck Topology

2.1.1 Buck Converter Principles

The buck (step-down) topology [12] has been used for decades, and it is the most fundamental topology in power electronics. It is composed of two power switches (S1, S2), an input capacitor in parallel with B1, an inductor, and one output capacitor, as shown in Fig.2.3.

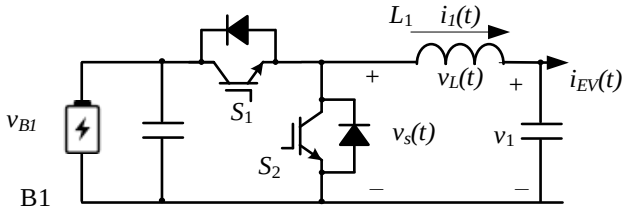


Figure 2. 3 The main circuit of the power stage for Buck topology

1) PWM switches

The two power switches are driven by a couple of complementary gate-drive PWM signals at duty cycle D and 1-D. The voltage of the node between the mid-point of switches and ground, v_s, alternates between V_{B1} and 0, as shown in Fig. 2.4. The switching network output voltage $v_s(t)$ has a DC component that is less than input voltage V_{B1}. The DC component is given by its average value as the following equation:

$$< v_s(t) > = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_s(t) dt \tag{2.3}$$

The integral is given by the area under the curve $DT_{sw}V_{B1}$, so the average value of $v_s(t)$ is derived as equation (2.4)

$$< v_s(t) > = \frac{1}{T_{sw}} DV_{B1}T_{sw} = DV_{B1} \tag{2.4}$$

, where D is between 0 and 1. The DC component of $v_s(t)$ equals the duty cycle D times the input voltage V_{B1}. The switches S1 and S2, driven by PWM signals, reduce the input voltage V_{B1} by a factor of D. Since $0<D<1$, the output voltage v_1 will always be larger than 0 and less than V_{B1}.

The limited voltage range of v_1 will be one of the limitations of buck topology, and this limitation makes buck topology unsuitable for the RDC concept when regulating a wide EV voltage range (274-403V). We will discuss the reason in detail in Section 2.2.

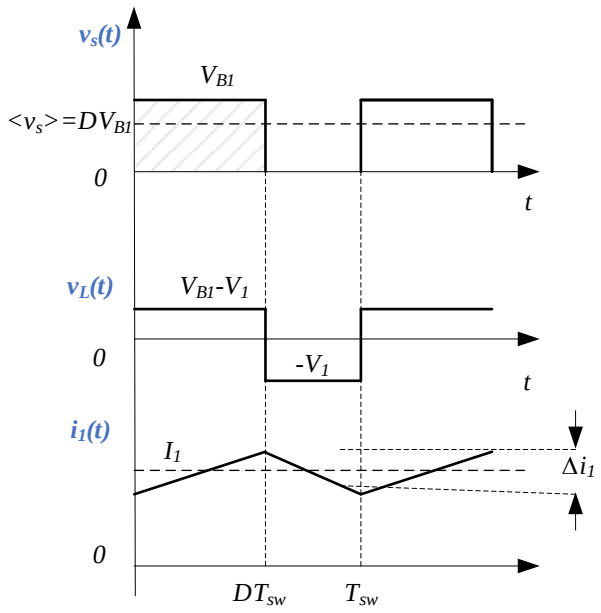


Figure 2. 4: Operational waveforms of buck topology at the steady state.

2) LC low-pass filter

As we have discussed above, the two switches generate the rectangular waveform $v_s(t)$ with a reduced DC component (DV_{B1}). An LC filter, shown in Fig.2.3, is to block the high-frequency harmonics (known as ripples) from flowing into the load, so as to provide a DC output voltage with a very small ripple. Usually, the output voltage ripple is less than 1% of its DC component. So, it is always a good approximation to assume the output voltage v_1 is a DC voltage V_1. This approximation is well-known as a small-ripple approximation in power electronics modeling in Section 4

Next is to analyze the inductor current waveform $i_1(t)$. The inductor current variation depends on the voltage applied to it. The voltage applied on the inductor during one switching period T_{sw} is shown in Fig. 2.4. According to Lenz's law, the relationship between inductor current $i_1(t)$ and its applied voltage $v_L(t)$ is illustrated as equation (2.5).

$$v_L(t) = L_1 \frac{di_1}{dt} \tag{2.5}$$

- When S1 is on and S2 is off ($0 < t < DT_{sw}$), the voltage applied on the inductor is V_{B1}-V_1, so the inductor current $i_1(t)$ is increasing linearly with a slope of $(V_{B1}-V_1)/L_1$.
- When S1 is off and S2 is on ($DT_s < t < T_{sw}$), the voltage applied on the inductor is $-V_1$, and the inductor current $i_1(t)$ is now decreasing with a slope of $-V_1/L_1$.

The inductor current $i_1(t)$ waveform is illustrated in Fig.2.4. The inductor current ripple Δi_1 is very important for the design of the inductor. It is the peak-to-peak (p-p) value of such a triangular waveform. Since we know the slope of the inductor current when for $0<t< DT_{sw}$, we can calculate Δi_1 by the following equation.

$$\Delta i_1 = \frac{V_{B1} - V_1}{L_1} DT_{sw} \tag{2.6}$$

Solution for the inductance L_1 yields:

$$L_1 = \frac{V_{B1} - V_1}{\Delta i_1} DT_{sw} \tag{2.7}$$

This is the most used equation for the design of an inductor in the buck topology [4]. The designed inductance usually depends on the inductor current ripple. A typical value for inductor L_1 current ripple lies between 20% and 40% of the rated load value of the DC component.

According to equation (2.7), allowing a larger inductor current ripple, reduces the inductance L_1, so as to reduce the cost and volume of the inductor. However, it is not desirable to allow Δi_1 to be too large, for this will increase the peak value of the inductor current leading to larger ripples and higher inductor AC winding losses [5]. This will be further discussed in inductor loss analysis in Section 3.3.

As discussed, it is always a good approximation to assume the output voltage v_1 is a DC voltage V_1. This approximation can be applied to other variables (v_{EV}, v_{B2}) in the circuit.

2.1.2 Buck Limitations

Before designing the RDC converter, we first need to investigate the input and output specifications (voltage, current, ripples) for the converter. For the RDC converter, the input and output are both battery packs. Therefore, battery characteristics, including voltage variation versus state-of-charge (SOC), need to be investigated, otherwise the designed RDC converter will not be practical.

In this study, the Tesla EV battery was taken as an example. During EV charging, the voltage of EV battery v_{EV} can vary from 274 V to 403 V. The detailed voltage vs SOC curve is shown in Fig.2.5.

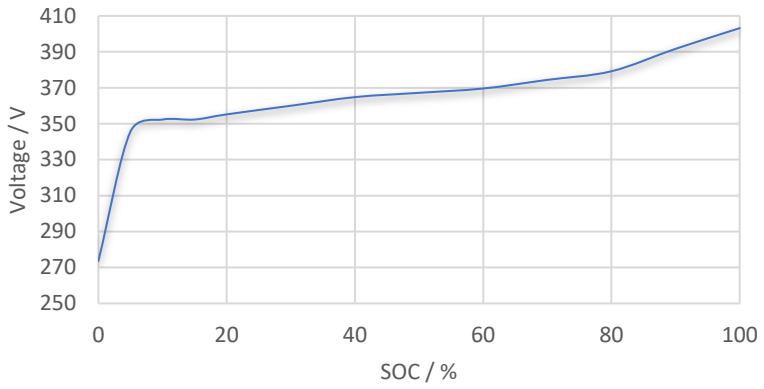


Figure 2.5: Voltage variation of Tesla EV battery versus SOC

In practice, the voltages of B1 and B2 will also change during their charging and discharging periods. The voltage range of B1 and B2 needs to be carefully designed to maintain partial power processing. The design process will be discussed in Section 3.1.

Fig. 2.6 shows the voltage variations of the EV and B2 for a single EV charging scenario. The blue curve shows the voltage variation v_{EV} of the Tesla EV battery vs SOC during EV charging, the orange curve shows an example of the voltage variation v_{B2} of B2 during one single EV charging scenario. Usually, the capacity of B2 (~200 kWh, see Table 1.5) is much larger than EV battery (average 60 kWh, see Table 1.1), and the voltage vs SOC of B2 during a single EV charging scenario is quite flat. v_1 is the required output voltage of the DC/DC converter. v_1 should be always controlled to compensate for the voltage difference between B2 and EV.

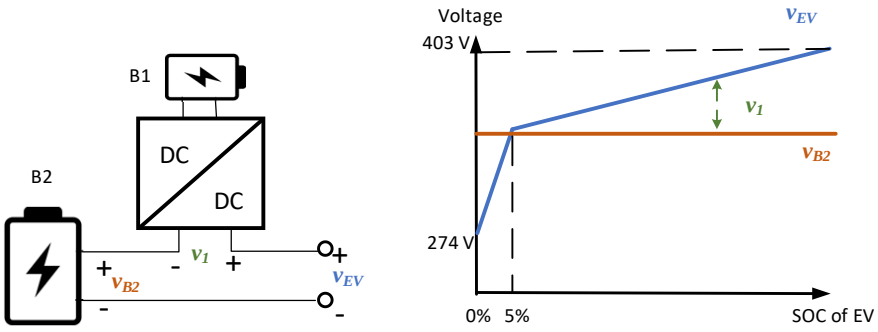


Figure 2. 6 Voltage variation of EV, Bat2 and output of DC/DC converter

According to equation (2.1), the output voltage (DC value) of the DC/DC converter is $V_1 = V_{EV} - V_{B2}$, as shown in Fig. 2.6. However, when EV is over-discharged ($SOC < 5\ \%$), V_{EV}

will go down rapidly and achieve a value $V_{EV} < V_{B2}$. This requires the polarity of V_1 to be inverted.

As discussed in the previous section, the output voltage buck converter $V_1=DV_{B1}$ ($0<D<1$) can only be regulated between 0 and V_{B1}, and the polarity of V_1 cannot be inverted, which means the buck topology loses the capability to control V_1 in this over-discharge region ($SOC<5\%$).

Therefore, the buck converter has limitations in controlling the voltage and current in the whole EV charging procedure. It is extremely important for commercial EV chargers to provide a measure for such unusual conditions. Other topologies to address this problem are now discussed below.

2.2 Full-bridge DC/DC Converter

Due to the output voltage polarity limitations of the buck topology, the RDC converter outlined in the previous section using a buck topology cannot regulate v_1 when the EV battery enters the over-discharge region (SOC < 5%).

However, a full-bridge topology [16] can regulate the output voltage v_1 ranging from $-v_{B1}$ to $+v_{B1}$. Fig. 2.7 shows the RDC configuration with full-bridge topology.

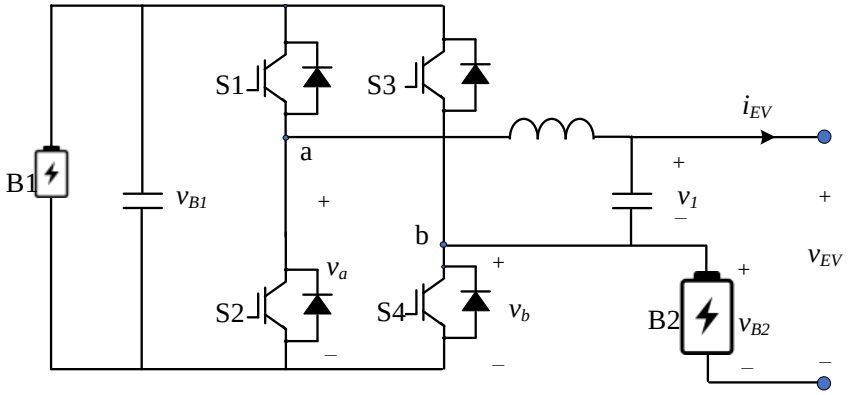


Figure 2. 7: Circuit of full-bridge topology for the RDC converter.

This full-bridge topology is composed of two half-bridge legs. For each leg, the operating principle is the same as the buck converter discussed in the previous section. The mid-point voltage of each leg is a pulsating waveform, the duty cycle of which can be controlled by a PWM switching signal. The average output voltage value of the mid-point of leg a (V_a)and leg b (V_b) are as follows:

$$V_a = \langle v_a \rangle = D_a V_{B1}, 0 < D_a < 1 \quad (2.8)$$

$$V_b = \langle v_b \rangle = D_b V_{B1}, 0 < D_b < 1 \quad (2.9)$$

As discussed, according to small signal approximation, the variables ($v_1, v_{B1}, v_{B2}, v_a, v_b, v_{EV}$) can be approximated as their DC components respectively.

Through the LC low-pass filter, the output voltage v_1 of the full-bridge converter is the difference between the average value of v_a and v_b, as follows.

$$v_1 = \langle v_a \rangle - \langle v_b \rangle = (D_a - D_b) v_{B1} \quad (2.10)$$

According to equation (2.10), the output voltage v_1 of the full-bridge converter can be regulated by PWM signals ranging from $-v_{B1}$ to $+v_{B1}$. Thus, the RDC converter using the full-bridge topology can overcome the polarity limitations of the buck converter.

v_1 can be regulated to $-v_{B1}$, when taking into account power equation (2.2), we have:

$$\underbrace{v_1 \cdot i_{EV}}_{P_{RDC}} = \underbrace{v_{B2} \cdot i_{EV}}_{P_{B2}} - \underbrace{v_{EV} \cdot i_{EV}}_{P_{EV}} \quad (2.11)$$

When $v_1 < 0$, equation (2.11) shows that B1 is extracting power from B2, this phenomenon is called power circulating, which will reduce converter efficiency and might undermine the life span of the total BESS (B1 and B2) system.

Furthermore, the full-bridge topology has other limitations:

- B1 is not grounded, which might affect the life span of B1.
- The protection is not sufficient. When an output short circuit happens, B2 cannot be immediately cut off from EV by adjusted power switches.

These drawbacks are addressed by the proposed topology in the next subsection.

2.3 Proposed Topology

To solve the limitations discussed above on the buck and full-bridge topologies, a novel topology should be designed to maintain wide voltage regulation, while providing enough protection to EV and BESS and avoiding power circulation. The novel topology for the RDC converter is shown in Fig. 2.8, it can be seen as two buck converters connected in series to increase the output voltage range, so as to control the voltage when the EV enters the over-discharge region (SOC<5%).

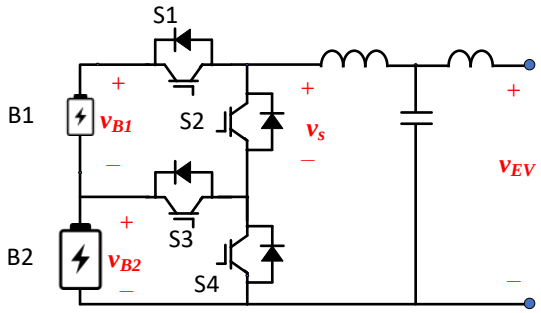


Figure 2.8 Circuit of proposed topology for RDC converter

The proposed novel topology works under two different modes. Under mode 1: when (SOC:5-100%) $v_{EV} > v_{B2}$; mode 2: when (SOC: 0-5%) $v_{EV} < v_{B2}$; The details of the working principle of the novel topology is illustrated below.

1) Mode 1: When $v_{EV} > v_{B2}$

In most scenarios, the voltage of EV v_{EV} is larger than B2 voltage v_{B2}, so that partial power processing can be achieved.

S4 is turned off, and S3 is now "permanently" on. B1 and B2 are now both charging EVs. The working circuit is shown in Fig. 2.9. This circuit is the same as the one shown in Fig. 2.2, where S1 and S2 are controlled by a PWM signal to regulate v_s. The average value of v_s is v_1. v_1 always compensates for the voltage difference between v_{B2} and v_{EV} during the whole charging process. The range of v_1 is limited to v_{B1}.

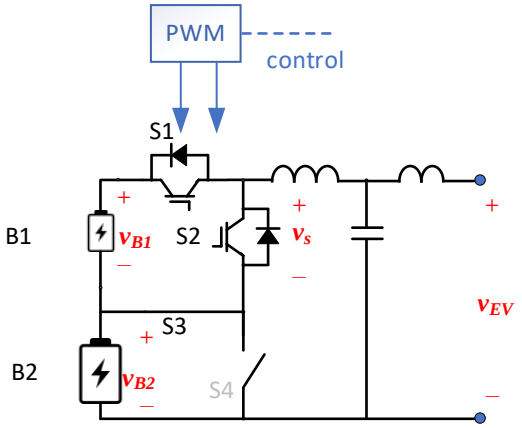


Figure 2.9: Circuit of the partial-power mode of the proposed RDC converter (Mode 1).

According to equations (2.1) and (2.2), most of the charging power flows directly from B2 to EV. S1 and S2 are now only processing partial power from B1. That is the RDC converter power P_{RDC} in equation (2.2).

The cost of a power converter correlates to power rating. Since we are processing part of the power, the power loss and cost of switches and inductors can be greatly reduced. In addition, the size of the inductor can also be reduced. This will be discussed in the hardware design of inductors in Section III.

2) Mode 2: When $v_{EV} < v_{B2}$ (SOC<5%)

As shown in Fig. 2.6, when EV is over-discharged (SOC < 5 %), v_{EV} will go down rapidly, and its value is smaller than v_{B2}.

S1 is turned off, B1 is cut off; S2 is now "permanently" on. The working circuit is shown in Fig. 2.10. v_1 is always zero, only B2 is now charging EV. The circuit is now working as a single buck converter, where the input is B2, and the output is the EV battery. The output charging voltage and current are regulated by S3 and S4 through PWM signals.

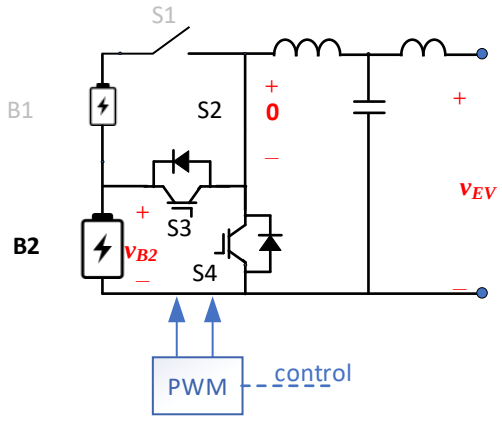


Figure 2.10: Circuit of full-power mode when EV enters an over-discharge region (Mode 2)

The disadvantage is that partial power processing is not maintained in this period. B2 is now charging EVs with full power processing. However, since EV manufacturers often recommend EV drivers not over-discharge their EVs, this situation rarely happens, so it will not enter this working condition in most scenarios. This circuit works as a necessary protection when an EV battery enters the over-discharge region.

2.4 Summary

Based on the discussion above, the comparison of different topologies has been summarized in Table 2.1.

Table 2.1: Comparison of different topologies for RDC converter

	Controllability	**Efficiency**	**Protection**
Buck	-	High	Weak
Full-bridge	++	Low	Weak
Proposed	+++	High	Strong

1) Though a single buck converter has the simplest circuit and high efficiency, it is not practical, due to the limitations of control when EV is over-charged and lack of sufficient protection between B2 and EV.
2) A full-bridge topology is then analyzed to provide enough controllability for EV over-discharge regulation. This causes power circulation between B2 and B1, which will significantly affect the efficiency of the RDC concept and may undermine the life span of BESS. In addition, protection between B2 and EV is weak. Thus, a full-bridge topology is still not enough from a practical perspective since protection is one of the most important issues for EV charging.
3) Therefore, a novel topology has been proposed to regulate charging voltage and current for all charge scenarios. For most of the fast EV charging period (SOC:5-100%), the proposed topology charges EVs with partial power processing. It can achieve high efficiency while reducing the cost. Under severe situations (EVs are unfortunately over-discharged, and their voltage drops down rapidly), the proposed topology can operate under mode 2 to guarantee the safe charging of EVs. Besides, the extra two switches in the novel topology can immediately cut down the BESS from EVs at the fault conditions, which can provide protection for EV and BESS.

3. HARDWARE DESIGN (20 kW)

In the previous section, the RDC concept has been designed to achieve very high efficiency, thanks to partial power processing [17]. A novel topology was proposed to provide wide voltage regulation (270-403V) while maintaining a low ratio of the power processed by the RDC converter (P_{RDC}/P_{EV}, as shown in equation (2.2)). In order to verify the proposed RDC concept and investigate the behavior of the associated novel topology, a small-scale (20kW) prototype is designed in this section. The hardware design is not trivial. For power converters, efficiency, and power density (power/volume) are two major aspects that need to be considered. An improper hardware design could lead to the following problems:

- An extremely compact design (small volume) can lead to very low efficiency (<96%), so the high efficiency due to partial power processing cannot be verified.
- On the other hand, one might design a very big converter. Though high efficiency can be achieved, the designed converter might be too big to be applicable. Besides, larger size usually means higher costs.

To design the RDC prototype properly, a hardware design procedure for the RDC converter is investigated, as shown in Fig.3.1.

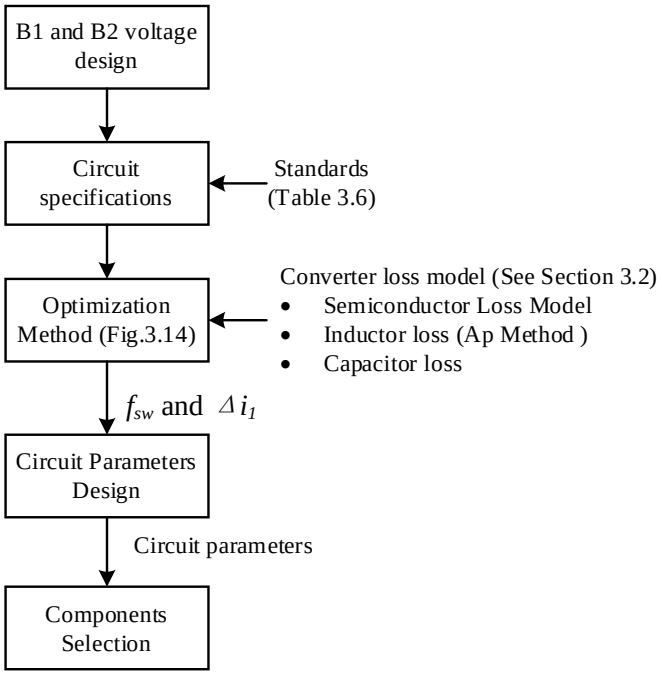


Figure 3. 1: The overview of the hardware design procedure of the RDC converter

As shown in Fig.3.1, the design procedure includes following:

- B1 and B2 voltage design
- Optimization of the converter with respect to switching frequency and current ripples
- Circuit parameters design
- Components selection

As shown in Fig.2.5, the EV voltage varies with respect to its SOC. The B1 and B2 voltage vs their SOC profile shows a similar behavior as the EV battery. Since the RDC converter incorporates the B1 and B2, the voltage of the B1 and B2 should be carefully defined first, this will be discussed in detail in Section 3.1.

After the B1 and B2 voltage ranges have been designed, the input (B1 and B2) and output (EV) voltage and current of the RDC converter are analyzed. With the current EV charging standard (CCS and CHAdeMO), the ripple requirements for the batteries (B1, B2, and EV) are derived. This forms the basic design requirements for the RDC converter.

An optimization method is then investigated to find an optimal operating point of the RDC converter, where the highest efficiency with the smallest volume can be found for the RDC converter. As shown in Fig.3.1, the optimization method highly relies on the converter loss model and Ap design method.

- Efficiency: calculated converter loss model (as shown in Section 3.2)
- Volume: determined by the Ap design method (as shown in Section 3.3.1)

Therefore, the converter loss model and inductor Ap design method were first investigated. Then, the optimization method is discussed in detail in Section 3.3.3.

Using the optimized optimal operating point (f_{sw} and Δi_1), the circuit parameters of the RDC converter can be designed. Based on the designed circuit parameters, the components can be selected from the market and assembled in the lab.

3.1 BESS Voltage Design

In the power converter parameters design process, circuit specifications should first be designed, including the input range and output range. For this RDC converter, the EV battery voltage range can be easily obtained from the EV manufacturer. However, the BESS (B1 and B2) is not designed yet. This means that the B1 and B2 voltage range is unknown.

On one hand, it is necessary to get the voltage range of the B1 and B2, so that the circuit specifications can be derived. The circuit parameters of the RDC converter will be designed to maintain input and output specifications for all operating ranges.

On the other hand, as shown in equation (2.2), the partial power processed by the RDC converter highly relies on the voltage difference between v_{B2} and v_{EV}. The Telsa Model Y EV battery is taken as an example of the v_{EV} voltage range (see Fig.2.5) as the design target. Two requirements for the B2 voltage design can be determined as follows.

1) To achieve partial power processing for all the normal cases of the EV battery (SOC: 5-100%), v_{B2} should always be smaller than $v_{EV.}$
2) The voltage difference between v_{B2} and v_{EV} should be minimized so that a low ratio of the partial power processed by the RDC converter can be achieved. For example, when the voltage difference is zero (v_1=0 in equation (2.2)), the power will flow directly from the B2 to the EV battery. Ideally, the efficiency will be approaching 100%.

For the B1 voltage requirement, since B1 is the input of the buck circuit (the upper half-bridge as shown in Fig.2.9), its voltage should be always higher than the voltage difference between v_{B2} and v_{EV}.

The B1 and B2 voltage design procedures will be discussed in detail in Section 3.1.3. Section 3.1.1 and Section 3.1.2 first investigate the EV battery voltage and the BESS cell level behavior.

3.1.1 EV Battery

In this case, the EV battery voltage range is first investigated, and the BESS (B1 and B2) voltage ranges are designed. The Tesla Model Y is taken as an example of designing of the RDC converter. As discussed in Section 2.1, Fig. 3.1 shows the voltage vs state-of-charge (SOC) of Tesla Model Y [18]. The voltage of this EV battery will range from 274 V at SOC equal to 0% to 403V (SOC=100%). For SOC ranging from 5% to 100%, the voltage increases from around 350V to 403V. Voltage variation is relatively small in this range. EV manufacturers often recommend that EV drivers should not discharge their EVs below 5% to maintain good battery performance over a long lifespan.

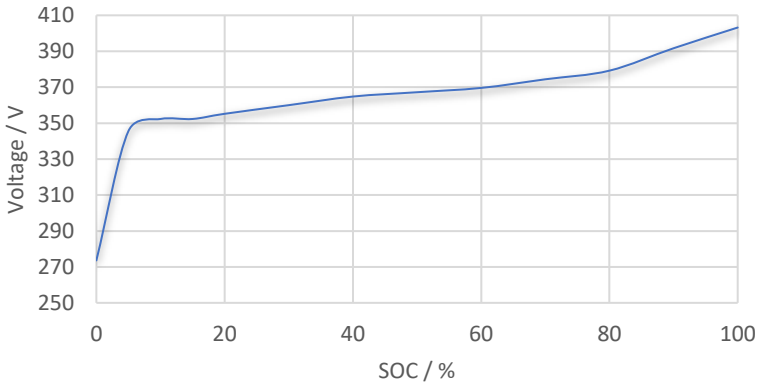


Figure 3. 2: Voltage variation of Tesla EV battery versus SOC[18]

However, over-discharge of EV batteries can happen in some extreme cases. The voltage of EV batteries decreases sharply from 350V to 274V when SOC drops from 5% to 0%, as shown in Fig.3.2. In this hardware design, for the EV battery normal cases (SOC: 5% to 100%), the RDC converter operates under mode 1 (partial power processing). Therefore, the voltage of the EV battery ranges from 350V to 403V.

Table 3. 1: The voltage vs SOC of Tesla Model Y

SOC	Voltage Cell /V	Voltage Pack/V
0%	2.85	274
10%	3.7	355
20%	3.75	360
80%	4.0	384
90%	4.11	395
100%	4.2	403

3.1.2 BESS Cell Characteristics

Like EV batteries, the BESS (B1 & B2) has a similar voltage variation with respect to its SOC. The BESS design itself is complicated. In this paper, the complete BESS design is not a major task. But, the voltage range of the BESS should be investigated and designed, in order to make the RDC converter practical for future applications. The designed BESS is emulated by a unit from Cinergia. This unit will be discussed in Section 5.

First of all, a BESS system is composed of individual cells organized in series and parallel [19]. A battery cell is the smallest component in a battery system. A battery pack (BESS) is assembled by connecting cells together in series and parallel. The voltage of a battery pack is

determined by the number of cells connected in series. The B1 and B2 voltage design is based on this and will be discussed in Section 3.1.3.

Lithium-ion batteries are commonly used for energy storage, and the main types of battery cells used in stationary BESS are NMC (nickel manganese cobalt) and LFP (lithium iron phosphate). In this RDC converter, the LFP-type battery cell is considered for BESS (B1 and B2). It has an optimal trade-off among the performance parameters below [20], as shown in Fig.3.3.

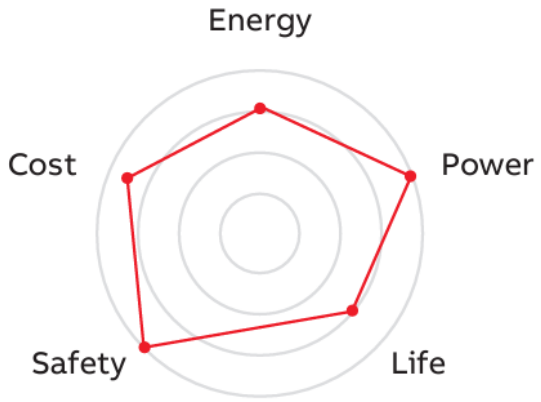


Figure 3. 3: LFP-type battery performance

The performance and advantages of the LFP-type battery are summarized as follows:

- Safety: LFP is one of the safest Lithium-Ion chemistries
- Power density: LFP batteries can reach 240 W/kg
- Energy density: LFP batteries can reach 120 Wh/kg
- Lifetime: LFP batteries can reach 6,000 charge/discharge cycles
- Cost: the price is very competitive due to the cheaper raw materials and low-price fluctuations

According to [21], the voltage profile with respect to its SOC for the LFP battery cells is shown in Fig.3.4.

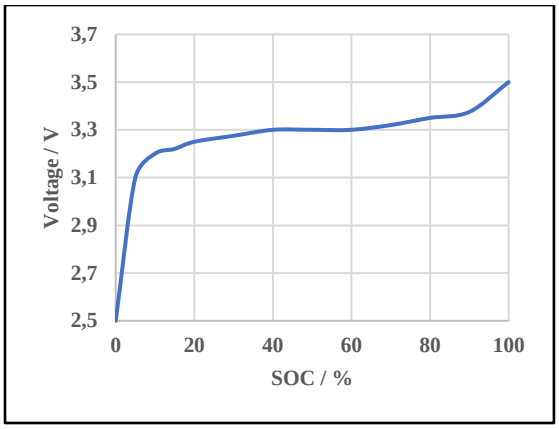


Figure 3. 4: The voltage variations for LFP battery cells. [21]

From Fig.3.4, we can find the voltage for a specific SOC of the LFP battery cell. Like EV batteries, the voltage of the cell drops sharply, when SOC < 5%, from about 3.0V to 2.5V. The main voltage values at critical SOC are summarized in Table 3.2. These values are critical to designing the B1 and B2 voltage range, which will be discussed below.

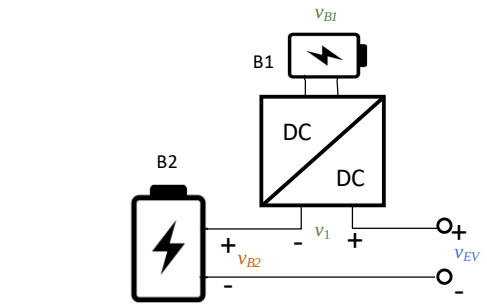
Table 3. 2: Critical voltages vs SOC for the LFP cell

SOC	**Voltage Cell /V**
0 %	2.5
5 %	3.1
100 %	3.5

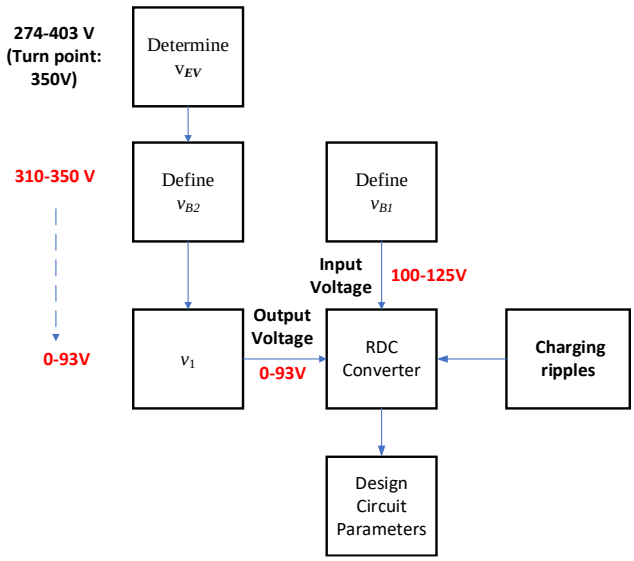
3.1.3 BESS Voltage Design

As discussed above, the LFP battery cell is chosen for the stationary BESS (B1 and B2). The BESS voltage can be designed by determining the number of cells connecting in series. The BESS voltage ranges are designed as below step by step.

The RDC converter configuration has been discussed in Section 2.1. This configuration is shown in Fig.3.5 (a). The input voltage for the DC/DC converter is v_{B1}, while the output voltage of the DC/DC converter is the voltage difference between the B2 and the EV. As discussed in Section 2.1, v_1 can be regulated by v_{B1}, so that v_1 equals the voltage difference between the B2 and the EV, as shown in equation (2.1).



(a) The RDC configuration.



(b) BESS voltage ranges design process

Figure 3. 5: BESS voltage design process for the RDC converter

The B1 and B2 voltage ranges are investigated and designed based on this RDC configuration. The BESS voltage ranges design process is illustrated in Fig. 3.5 (b). Based on Fig.3.5 (b), the B1 and B2 voltage ranges are designed step by step as below.

1) Design B2 voltage range

As discussed above, for normal cases of the EV, v_{EV} increases from 350V (at SOC=5%) to 403V (at SOC=100%). v_1 is the voltage difference between the B2 and the EV. Recall equation (2.2):

$$\underbrace{v_1 \cdot i_{EV}}_{P_{RDC}} + \underbrace{v_{B2} \cdot i_{EV}}_{P_{B2}} = \underbrace{v_{EV} \cdot i_{EV}}_{P_{EV}},$$

To achieve partial power processing (mode 1 in Section 2.3), we hope to maintain v_{EV} is slightly larger than v_{B2}. Ideally, when $v_{EV} = v_{B2}$, v_1 is zero. The power handled by the RDC converter is zero. The power is transferred from the BESS to the EV with 100% power efficiency.

To guarantee $v_{EV} > v_{B2}$ (mode 1) for all EV normal cases (v_{EV}:350V-403V), the maximum of v_{B2} should be smaller than v_{EV} minimum (350V). Therefore, the maximum voltage of B2 is set to 350V. As mentioned above, the voltage variation of the BESS is caused by the voltage variation of its cell.

According to Table 3.2, we can find that the LFP cell has a maximum voltage of 3.5 V (at SOC=100%). We can determine that the number of series connections is 100. For the BESS (B2), we often will not over-discharge it in order to extend its lifespan. The minimum SOC of the B2 can be set to 5% (cell voltage is 3.1V). Regarding this, the minimum voltage of the B2 is calculated to be 310V. The detailed information on the designed B2 is summarized in Table 3.3.

Table 3. 3: The main parameters of the designed B2

B2	Series Number	Vmin / V	Vmax / V
LFP cell	100	310	350

The number of parallel connections for the B2 is not required, since it will not affect the voltage variation of the B2. This can be determined in the future when defining the total capacity of the BESS in a fast-charging station.

2) Design B1 voltage range

With v_{EV} and v_{B2} ranges designed above, the voltage difference v_{EV}-v_{B2} can be calculated. Considering all the extreme cases during charging, the maximum difference (v_{EV}-v_{B2}) is based on the maximum v_{EV} (403 V) and minimum v_{B2} (310V), as shown in equation (3.1).

$$v_{1max} = (v_{EV} - v_{B2})_{max} = v_{EV_{max}} - v_{B2\ min} = 93V \quad (3.1)$$

As shown in Fig.3.5(a), v_{EV}-v_{B2} is the input voltage while v_1 is the output voltage of the RDC converter. Considering the step-down (input voltage > output voltage) characteristics of the buck circuit, the minimum voltage of the B1 (input voltage) must be larger than v_1 (output voltage). Like the B2, we can design the number of the cells connected in series, so as to guarantee the minimum voltage of the B1 is larger than 93V.

According to Table 3.2, we know the minimum voltage of the LFP cell is about 3.1V. As discussed above, v_{B1} should be always larger than v_{1max} (93V). To give some design margin, the number of the cells connected in series of the B1 is chosen to be 35, so that the minimum voltage of the B1 is about 100V (> 93V). The associated maximum voltage of the B1 is about 125V. The designed B1 is summarized in Table 3.4.

Table 3. 4: The main parameters of the designed B1

B1	Series Number	Vmin / V	Vmax / V
LFP cell	35	~100	~125

3) Circuit specifications of the RDC converter

From the above voltage definitions, the BESS and EV are summarized in Table 3.5.

Table 3. 5: Summary of the BESS and EV designed in this RDC converter.

Battery	Cell	Number of series	Voltage range/V
EV	NCM	96	271-403
B1	LFP	35	100-125
B2	LFP	100	310-350

Based on these parameters, as shown in Fig.3.5(b), we can get the input and output ranges of the RDC converter. When charging/discharging the batteries, it often requires the charging/ discharging voltage and current have limited ripples. Table 3.6 summarizes the ripple requirements from different charging standards/manufacturers.

Table 3. 6: Ripples limits for batteries from different sources

Sources (Standard/manufacturer)	Current ripples / p.u.	Voltage ripples / V
CCS (Standard)	5% (p-p)	0.4 (p-p)
Tesla Supercharger	2% (p-p)	NA
CHAdeMO	5% (p-p)	0.1 (p-p)
This study	5%	0.4

The current ripple (peak-to-peak) is usually defined by the ratio of ripple magnitude divided by the DC current value. In Table 3.6, we can see that CCS and CHAdeMO require the current ripple to be less than 5%, while the Tesla supercharger has a smaller ripple requirement (2%). In this study, since this is the first iteration of the prototype, a 5% current ripple requirement is chosen and a 0.4V (peak-to-peak) voltage ripple requirement is chosen for the design.

From Table 3.5 and Table 3.6, we get the circuit specifications of the RDC converter. The RDC converter should satisfy all the requirements as well as provide voltage and current regulation for all the voltage ranges of the BESS and the EV. Circuit parameters are then designed in the following sections.

3.2 Converter Loss Model

For the hardware design of power electronic circuits, high power efficiency (BESS to EVs) and power density are two major design goals. The definitions of power efficiency and power density are shown in equations (3.2) and (3.3) respectively.

$$Efficiency = \frac{Input\ power - Loss}{Input\ power} \tag{3.2}$$

$$Power\ density = \frac{Input\ power}{Converter\ Volume} \tag{3.3}$$

Often there is a trade-off between efficiency and power density. The optimization method (see Fig.3.1) is to find an optimal operating point where high efficiency (loss) can be achieved without sacrificing the power density. The converter loss model is then needed for the optimization method. Therefore, this subsection focuses on the analysis of the converter losses first.

As we have discussed in Section 2.3, the RDC converter works under partial power processing (mode 1) for most charging scenarios. To simplify the design process, the loss analysis is based on mode 1 of the RDC converter. The overview of the loss distribution of the RDC converter is given in Fig 3.6. The pink blocks represent losses of power switches (S1, S2, S3) [17], inductors (L1 and L2), and capacitors (C) respectively.

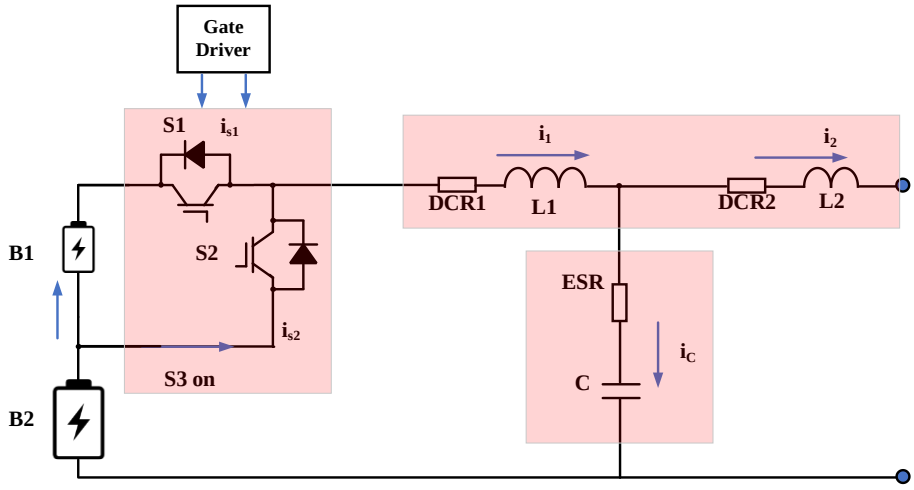


Figure 3. 6: Losses break-down of the RDC converter

For each component, the loss is analyzed based on its current waveform and its own loss characteristic. The overview of major losses is as follows:

- Power switches loss: The losses are mainly composed of switching loss and conduction loss.

- Inductor loss: inductor loss often contributes a significant part for total loss. The loss is composed of the DC winding loss (DCR1 & DCR2), the AC winding loss (high-frequency losses), and the core loss. In this study, only the DC winding loss and core loss are analyzed.
- Other losses: The Capacitor loss is determined by the equivalent series resistance (ESR) of the capacitor. A low-ESR capacitor is always preferred, but low-ESR capacitors are usually more expensive. PCB trace loss, cable loss, terminal losses, etc. are not included in the power loss model in this study.

In this study, the semiconductor loss and inductor loss are taken into the converter loss model for the optimization method, as shown in Fig.3.1.

3.2.1 Semiconductor Losses

Power switches (semiconductors) losses are composed of conduction loss and switching loss. To derive the power switches loss model, the current waveform flowing through the power switches should first be analyzed.

As discussed in Section 2.1.1, the converter-side inductor current i_1 shows a triangular waveform added on a DC value (I_1). The peak-to-peak value of the triangular waveform is the current ripple (Δi_1), as shown in Fig.3.7. The current waveforms (i_{S1} *and* i_{S2}) of S1 and S2 are illustrated in Fig.3.7 too. Since S3 is "permanently" on and connected in series with S2, the current waveform is the same as that of S2. So, the conduction loss of S3 is the same as S2.

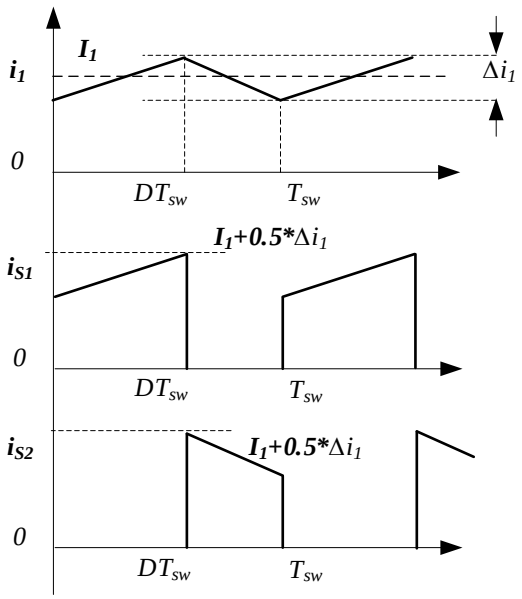


Figure 3. 7: Current waveforms for power switches S1 and S2.

In one switching cycle T_{sw}, the switches S1 and S2 are only conducting in a period of DT_{sw} and $(1\text{-}D)\ T_{sw}$ respectively, where D is the duty cycle of PWM signals.

- At $t=0$, S2 is turned off and S1 is turned. The inductor current i_1 is commutating from S2 to S1. During $t=0 \sim DT_{sw}$, the S1 current i_{S1} is the inductor current i_1. The current i_{S1} waveform shows a pulsating waveform with a linear ripple.
- At $t= DT_{sw}$, i_1 commutates from S1 to S2. During $t=DT_{sw} \sim T_{sw}$, the inductor current i_1 flows through S2. The current i_{S2} is also a pulsating waveform with a linear ripple.

The current waveforms can be used to calculate the conduction loss for the switches. Besides, for non-ideal power switches, at $t=0$ and $t= DT_{sw}$, it takes time to commutate the current between the switches (S1 and S2). The transient processes will result in switching losses. This will be discussed in the switching loss part.

MOSFETs are often used in relatively high switching frequency (higher than IGBT), low voltage, and high current applications. In this small-scale RDC converter, MOSFETs are selected to achieve high switching frequency and efficiency.

1) Power Switches Conduction Losses

Conduction losses (P_{con}) in power MOSFET can be calculated by its approximated on-state resistance (R_{dson}), and the associated power loss is shown in equation (3.4).

$$P_{con} = R_{dson} \times I_{RMS}^2 \tag{3.4}$$

, where I_{RMS} is the root-mean-square value of the conducting current.

Taking into account the current waveforms of S1 and S2 in Fig.3.7, the RMS value for each current waveform i_{S1} and i_{S2} can be calculated as follows [4]:

$$I_{RMS_{S1}} = I_1\sqrt{D}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_1}{I_1}\right)^2}$$
$$I_{RMS_{S2}} = I_1\sqrt{1-D}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_1}{I_1}\right)^2} \quad (3.5)$$

, where D is the duty cycle, Δi_1 is the converter-side current ripple (peak-to-peak) and I_1 is the output DC current (50A).

Substitute equation (3.5) into equation (3.4), the conduction losses of S1 and S2 are given by following

$$P_{S1_{con}} = R_{dson}{I_1}^2 D\left[1+\frac{1}{12}\left(\frac{\Delta i_1}{I_1}\right)^2\right]$$
$$P_{S2_{con}} = R_{dson}{I_1}^2(1-D)\left[1+\frac{1}{12}\left(\frac{\Delta i_1}{I_1}\right)^2\right] \quad (3.6)$$

These are the conduction loss models for S1 and S2. In practice, R_{dson} relates to the operating temperature of MOSFETs. We will come back to this temperature dependency in the next part.

2) Switching losses

The linearized switching process of MOSFETs is often sufficient for the engineering switching loss calculation. Fig.3.8 shows the linearized turn-on and turn-off process of MOSFET S1. The left graph represents the process of turning on a MOSFET, where V_{GS} increases, causing I_{DS} to rise and V_{DS} to fall. The right graph represents the turn-off process, where V_{GS} decreases, leading to I_{DS} falling to zero and V_{DS} rising.

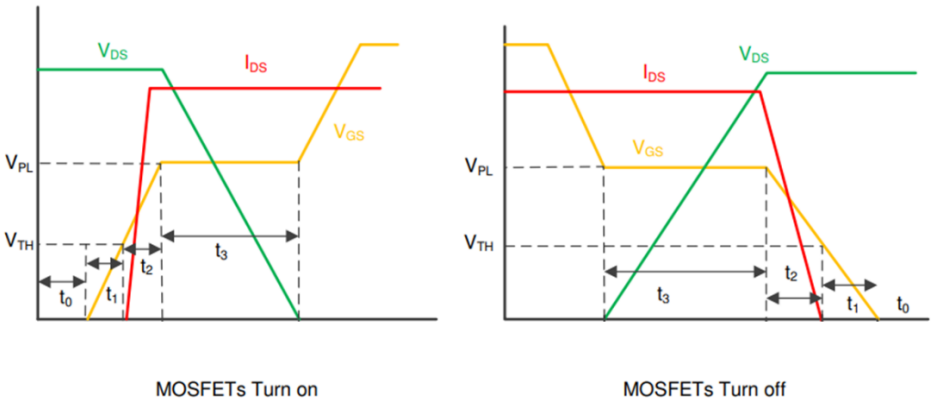


Figure 3. 8: Turn-on and turn-off transient processes of MOSFETs[22]

The details information can be found in [22] , this thesis will not discuss the details. For a better understanding, the key aspects of Fig.3.8 are summarized as follows:

- V_{GS} (yellow curve) is the driver gate voltage to turn on and turn off the MOSFET. I_{DS} (red curve) is the current flowing into the MOSFET. V_{DS} (green curve) is the voltage across the MOSFET.
- For turn on process, during t_1, the gate voltage V_{GS} begins to rise from 0V. During this time, the MOSFET is still off. During t_2, V_{GS} reaches the threshold voltage V_{TH}. The MOSFET begins to conduct slightly (I_{DS} increases). But V_{DS} remains high. During t_3, V_{GS} reaches the plateau voltage V_{PL}, the MOSFET is fully turned on. During this time, the drain-source voltage V_{DS} decreases to "zero".
- For the turn-off process, during t_3, the gate voltage V_{GS} begins to decrease. During this time, the MOSFET is still on, and V_{DS} begins to increase slightly. During t_2, V_{GS} reaches V_{PL} and begins to decrease to V_{TH}. The MOSFET begins to switch off slightly (I_{DS} decreases). During t_1, V_{GS} reaches V_{TH}, the MOSFET is fully turned off. During this time, the drain-source current I_{DS} decreases to "zero".

With the above-linearized switching on/off waveforms, we can calculate the energy loss for one switching period T_{sw}. In one switching period T_{sw}, the MOSFET is turned on and turned off each time. According to the energy definition, the energy loss is the integral of the power loss with time. Thanks to the linearized waveform, the energy loss can be easily calculated. The turn-on energy loss $E_{on_{s1}}$ and the turn-off energy loss $E_{off_{s1}}$ in S1 for one switching period T_{sw} can be calculated as follows:

$$E_{on_{s1}} = \int_0^{t_2+t_3} V_{DS}(t) \times I_{DS}(t)dt = \frac{V_{B1}}{2}\left(I_1 - \frac{\Delta i_1}{2}\right) \times (t_2 + t_3) \quad (3.7)$$

$$E_{off_{s1}} = \int_0^{t_2+t_3} V_{DS}(t) \times I_{DS}(t)dt = \frac{V_{B1}}{2}\left(I_1 + \frac{\Delta i_1}{2}\right) \times (t_2 + t_3) \quad (3.8)$$

, where $(t_2 + t_3)$ can be calculated by the parameters from the datasheet [22]. According to Fig.3.7, the S1 current during turn on process reaches the valley ($I_1 - \frac{\Delta i_1}{2}$) of the triangular waveform; the S1 current during turn off process is the peak value ($I_1 + \frac{\Delta i_1}{2}$) of the triangular waveform. Besides, the worst-case parameters are often used to calculate switching energy losses. For example, the maximum voltage V_{B1} of the B1 is considered.

The switching losses $P_{S1_{sw}}$ in the MOSFET S1 are the product of energy losses and switching frequency f_{sw}.

$$P_{S1_{sw}} = E_{on_{s1}} \times f_{sw} + E_{off_{s1}} \times f_{sw} \quad (3.9)$$

For MOSFET S2, switching loss is often negligible, due to the benefits of the zero voltage switching [23]. But transient losses of S2 are composed of its body diode loss during dead time as well as reverse recovery [17]. In practice, the dead time is needed to prohibit the switches S1 and S2 from short-circuiting, since it always takes time for MOSFETs to be fully turned off. Fig.3.9 illustrates the current waveforms and gate drive signals of S1 and S2, taking into account the dead time (the two pink blocks *dT*). G1 and G2 represent gate drive signals for S1 and S2 respectively. During the dead time (*dT*), both S1 and S2 are turned off, and the body diode of S2 is now conducting.

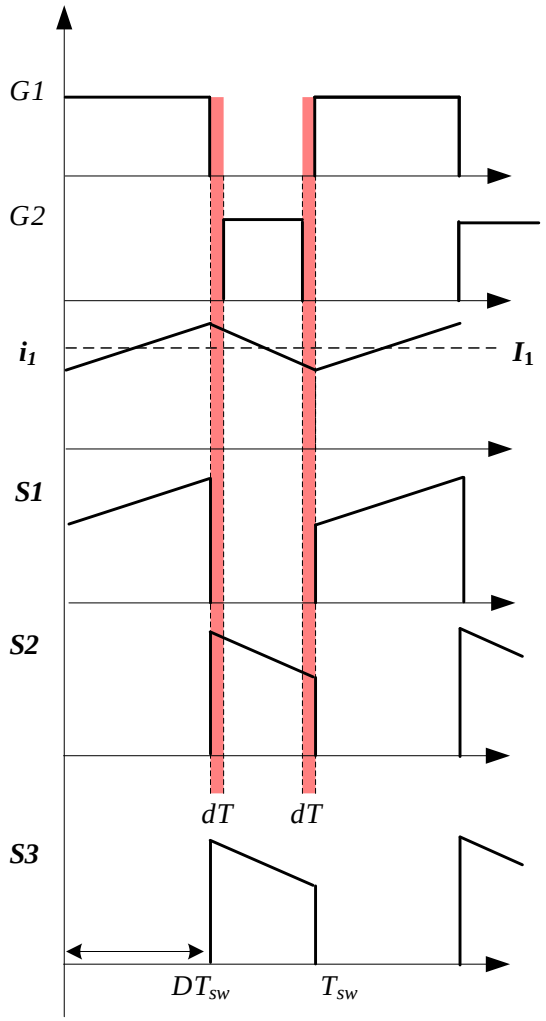


Figure 3. 9: Current waveforms and gate signals for switches S1 and S2 considering dead-time.

The transient losses of S2 are composed of body diode loss during dead time $P_{S2_{DT}}$ and body diode reverse recovery loss P_{rr}. These two transient losses can be calculated as follows,

$$P_{S2_{DT}} = V_{SD} \times \left[\left(I_1 - \frac{\Delta i_1}{2}\right) \times dT + \left(I_1 + \frac{\Delta i_1}{2}\right) \times dT\right] \times f_{sw} \quad (3.10)$$

, where V_{SD} is the conducting forward voltage of the body diode and dT is the dead time.

$$P_{rr} = Q_{rr} \times V_{B1} \times f_{sw} \quad (3.11)$$

, where Q_{rr} is the reverse recovery charge of the body diode. V_{B1} is the voltage across the body diode, it is the input supply voltage V_{B1} in this case. Taking into account equation (3.10) and equation (3.11), transient loss of S2 is given by equation (3.12).

$$P_{S2_{sw}} = P_{S2_{DT}} + P_{rr} \quad (3.12)$$

For power switch S3, since S3 is always on, only conduction losses should be taken into account. The conduction of S3 is the same as S2. Overall, the conduction losses and switching losses for S1, S2, and S3 are analyzed.

3) Switches loss model considering temperature.

In Section 3.2.1, we have discussed about conduction losses and switching losses of MOSFETs. However, the changing junction temperature of MOSFETs has not been considered. The changing temperature could affect the electrical parameters of MOSFETs. In practice, several parameters of MOSFETs are closely related to temperature. For example, the on-state resistance is higher at higher temperatures. We use the junction temperature of the MOSFET to build a more accurate loss model for MOSFETs.

The on-state resistance of a MOSFET depends on the junction temperature and can be represented by

$$R_{dson}(T_j) = R_{dson}(25\ ℃) \times \left(1 + \frac{\alpha}{100}\right)^{T_j - 25\ ℃} \tag{3.13}$$

Where α is the coefficient of resistance vs temperature. T_j is the junction temperature of the MOSFET. Often, MOSFET manufacturers will provide a R_{dson} vs T_j curve. Taking into account this curve, α can be calculated, leading to the model of $R_{dson}(T_j)$.

After we get the temperature-dependent parameters of MOSFETs, losses of MOSFETs can be calculated by the following procedure, as shown in Fig.3.10. First, the conduction and switching losses of MOSFETs are calculated at 25 ℃. Based on the calculated power loss, the junction temperature of the MOSFET will be updated. Then, the next junction temperature $T_j(n)$ of the MOSFET can be calculated by its thermal resistances. At the updated $T_j(n)$, the conduction and switching losses of the MOSFET are calculated again. This will continue till $T_j(n)$- $T_j(n-1)$ is less than the required accuracy ΔT.

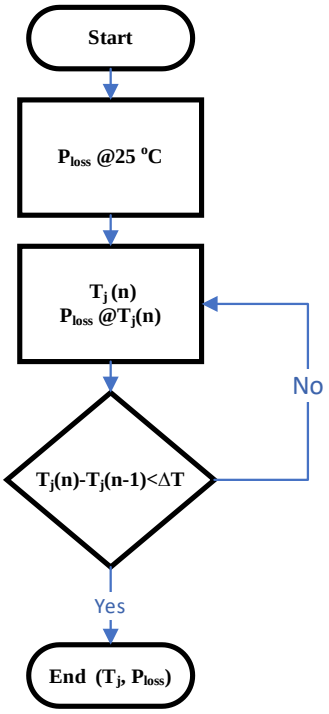


Figure 3. 10: Accurate loss model of MOSFETs considering junction temperature.

In this RDC converter, IRF300P226 MOSFET has been selected as the power switch for S1 and S2. The equivalent specifications of the RDC buck converter are shown in Table 3.7.

Table 3. 7: Specifications of the RDC buck converter for the loss model verification

Parameters	Value
V_{B1} *(max)*	125 V
I_1	50A
D	0.5
f_{sw}	40kHz
Δi_1	40%@50A
L1	31 μH
Semiconductor	IRF300P226

The loss model above has been built in MATLAB. To verify the accuracy of the above loss model, a buck converter circuit with the thermal model of MOSFETs and heatsink has been built in PLECS. The comparison of the simulation results (PLECS) and the calculation (MATLAB) are also shown in Table 3.8.

Table 3. 8: Comparison of simulation results (PLECS) and calculation (MATLAB)

	MATLAB	**PLECS**	**ERROR**
S1 Loss/W	39.50	39.55	0.10%
S2 Loss/W	22.61	22.22	1.7%
S3 Loss/W	22.02	22.10	1.50%
Tj_S1 /℃	72.56	72.47	0.10%
Tj_S2/℃	63.95	63.63	0.50%
Tj_H/℃	52.42	52.33	0.17%

As shown in Table 3.8, the differences between MATLAB calculation results and PLECS simulation results are all less than 1.7%, the accuracy of which is acceptable for power loss estimation. Overall, the MATLAB calculation fits very well with the simulation results, which verifies the accuracy of the loss model. The loss model of the MOSFETs is sufficient to estimate the losses and temperature for different working conditions. This MOSFET loss model will be applied to optimize the efficiency and power density of the RDC converter under different switching frequencies and current ripples in Section 3.3.

3.2.2 Inductor Loss

In power converters, magnetic components (inductors in this case) are often the most bulky components[11]. A properly designed inductor can provide sufficient regulation of the RDC converter while keeping the physical size as small as possible. As discussed in Section 3.1, we have two inductors L_1 and L_2 in the LCL filter. Usually, L_2 is very small and L_1 is big. Therefore, the inductor design is mainly focused on the design of L_1 in this study. The inductor L_2 can be easily bought from the market, with the calculated inductance.

To derive the inductor loss model, an inductor design method (Area Product (*Ap*) Method) will be first introduced. Based on the *Ap* design method, the inductor loss model can be derived for different f_{sw} and Δi_1. Later, an optimization method based on the trade-off between efficiency and power density is analyzed and illustrated.

1) Inductor *Ap* design method

An inductor is composed of a magnetic core and a set of windings to store magnetic energy for the power converters, as shown in Fig.3.11.

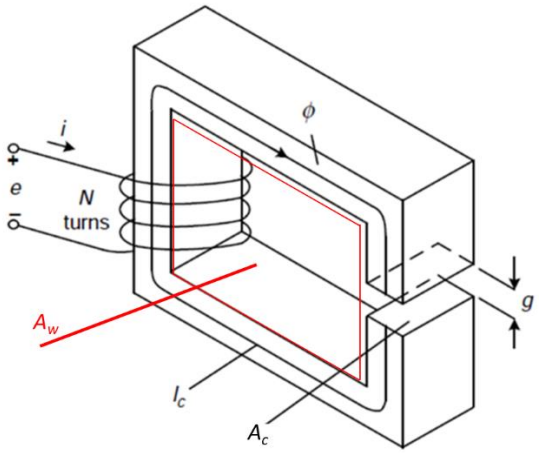


Figure 3. 11: A typical physical model of an inductor with an air-gapped core and windings[12]

In Fig.3.11, the magnetic core is surrounded by a set of windings with N turns. The magnetic core has a cross-section area of A_c and the length of the core is l_c. g represents the length of the air gap (An air gap is usually to avoid saturation of the core). When there is a current i flowing into the windings, it will introduce a magnetic field inside the core with the total magnetic flux Φ.

The magnetic core manufacturers will usually provide the physical parameters of the core. This can help the designer to choose proper magnetic cores and do the initial loss calculations. Table 3.9 shows the parameters of the magnetic core PC47EI60-Z. A_c is the core cross-sectional area, A_w is the core window winding area, and Ap is the area product. V_c represents the total volume of the core. MLT is the mean length per turn of the core. It can be used to calculate the total length of the winding with the designed turns. B_{sat} is the saturation magnetic flux density of the magnetic material used in the core. If the magnetic flux density goes above this value, the inductance of the inductor will be smaller than the required value. The inductor will then lose the regulation of the current.

Table 3. 9: The parameters of the magnetic core PC47EI60-Z

Parameters	Value
A_c /cm^2	2.47
l_c /cm	10.90
A_w /cm^2	4.02
Ap /cm^4	9.94
V_c /cm^3	26.90
MLT /cm	8.80
B_{sat} /T	0.42

There are many available cores in the market. A big core often can provide more stored energy, but it will increase the volume of the converter. If a small core is selected, it will often increase the inductor loss, since a thinner set of windings should be used to fit in the core. Therefore, a proper core selection is very important for the inductor design. A good starting point for an inductor design is calculating area product *Ap* from the circuit specifications and empirical data. This initial inductor design is the so-called *Ap* method[4]. Fig.3.12 shows the inductor design procedure used in this paper. The detailed parameters and equations shown in Fig.3.12 will be illustrated step by step below.

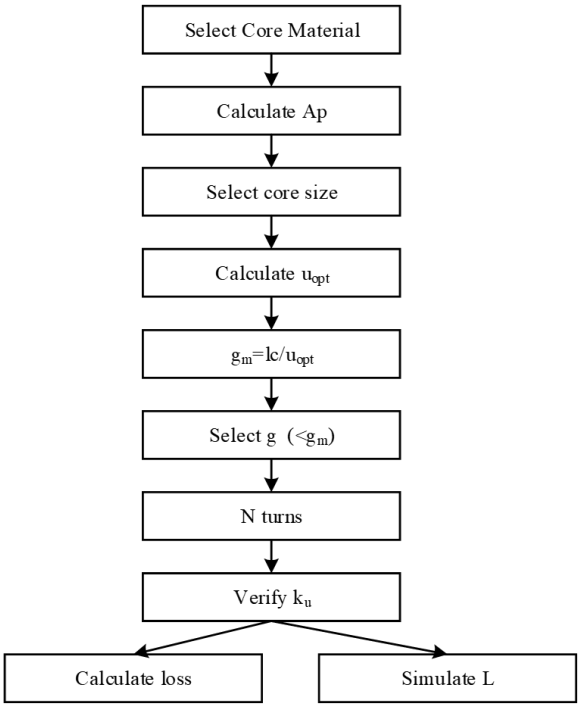


Figure 3. 12: The design methodology of the inductor

First, the magnetic material for the core should be first selected. For a power inductor, a Mn-Zn ferrite core with an air gap is usually used. Table 3.10 shows different materials of the ferrite core from TDK company. PC40 material is suitable for a large core of high-power applications (usually low frequency <100 kHz). While PC95 and PC47 are usually used for high-switching frequency applications (up to 300 kHz). The materials summarized here are later used as a starting point for the inductor design.

Table 3. 10: Different magnetic material for the inductor core

	PC95	**PC47**	**PC40**
Application	<300 kHz	<300 kHz	Large core
Permeability μ_r	330	2500	2300
B_{sat} / T @100 °C	0.41	0.42	0.38
Size Ap /cm^4	< 9.93	< 9.93	> 16

With the above pre-selected material, a core library is built by all the available cores from TDK company. The area product *Ap* is calculated to initially select a suitable core for the inductor. As shown in equation (2.7), the inductance is first calculated by the circuit specifications. The physical size (area product *Ap*) of the inductor is usually calculated by equation (3.14) [9].

$$Ap = A_c A_w = \frac{V_{B1max} D(1-D)_{max}}{f_{sw} \Delta i_1} \times \frac{I_p I_{rms}}{B_{max} k_u J_{rms}} \tag{3.14}$$

Comparing the calculated area product *Ap* to available cores, a core with a minimum size (slightly larger than the calculated *Ap*) can be identified and selected from the built core library. In equation (3.14), there are mainly three groups of parameters, as summarized below.

- Circuit specifications

These values are required by the input voltage and output voltage of the RDC converter. For example, V_{B1max} is the maximum input voltage of the B1 in the RDC converter, as defined in Fig.2.8. At the different working conditions, duty cycle D can also vary from 0 to 1. The worst case of the duty cycle is considered to guarantee that the designed inductor is large enough for all situations. Therefore, V_{B1max} represents the maximum operating input voltage. $D(1-D)_{max}$ stands for the maximum value of the expression when D=0.5.

- Design choices

Switching frequency f_{sw} and inductor L_1 current ripple Δi_1 can be defined by the designer. With the defined DC charging current I_1 (50A) and current ripple Δi_1, we can easily calculate the peak current I_p and RMS current I_{rms} flowing into the inductor.

As can be seen from equation (3.16), switching frequency f_{sw} and inductor L_1 current ripple Δi_1 can significantly affect the *Ap* value of the inductor. High switching frequency and larger Δi_1 can significantly reduce the size of the inductor. But this will introduce much larger losses to the RDC converter. This forms the basis for the optimization of the trade-off between power density and efficiency, which will be discussed in detail in Section 3.3.

- Empirical data

Other values are based on empirical data for a power inductor with a gapped ferrite core.

a) B_{max} is the maximum flux density in the magnetic core. It should be set to less than the saturation flux density B_{sat} of the magnetic material.

b) k_u is the window winding utilization factor, which is calculated by winding area (winding cross-section area multiplied with turns) over total core window area *Aw*. If k_u is too small, the winding might not be fitted inside the selected core. According to empirical data, it is usually set to be around 0.3-0.7[4].

c) J_{rms} is the current density in the winding. If the current density is too large, the winding will be overheated, causing extreme temperature rise in the inductor.

In this study, B_{max}, k_u, J_{rms} are set to be 0.3T, 0.4, and 4A/mm^2 respectively by empirical data [13]. With this current density and 50A rated current for the RDC converter, the diameter of the wire for the windings can be roughly selected [14]. In this design, the Litz wire is used to reduce the AC loss inside the inductor. The parameters of the selected Litz wire are shown in Table 3.11.

Table 3. 11: parameters of the selected Litz wire for the inductor

Parameters	Value
Strand diameter*number	0.1mm*1500
Diameter/mm	5.34
Total area / mm^2	22.40
Conductor area A_{con} / mm^2	11.78

Litz wire is composed of many small strands. As shown in Table 3.11, the selected Litz wire has 1500 strands with 0.1mm diameter. The total conductor area A_{con} is about 11.78 mm^2 (this is the area of the conductor itself), so the current density is about 4.2 A/mm^2. Including necessary isolation material between each strand as well as the surrounding case, the Litz wire has a total cross-section area of 22.40 mm^2. The loss of the selected lite wire in the inductor will be discussed at the end of this subsection.

As discussed, with the calculated *Ap*, we can select a suitable core from the core library. The parameters of the selected magnetic core are given by its datasheet. Table 3.9 gives an example of the parameters of a magnetic core.

According to[13], with the parameters of the core, we can calculate the optimal effective permeability u_{opt} by equation (3.15).

$$u_{opt} = \frac{B_{max} l_c K_i}{\mu_0 \sqrt{\frac{P_{cu} N A_w}{\rho_w MLT}}} \tag{3.15}$$

, where K_i is the ratio of I_{rms}/I_p, and μ_0 is the permeability of the free space. P_{cu} is the winding loss (copper loss). ρ_w is the resistivity of the conductor (copper). Then, we can design the optimal length of the air gap g_m by equation (3.16).

$$g_m = \frac{l_c}{\mu_{opt}} \tag{3.16}$$

Based on the calculated g_m, we still have the freedom to change the air gap length. In this design, the calculated air gap length g_m is used as a starting point. Fig.3.13 shows the relationship between air gap length and A_L (inductance per turn square nH/N^2) value given by the datasheet of the core PC47EI60-Z from the manufacturer TDK.

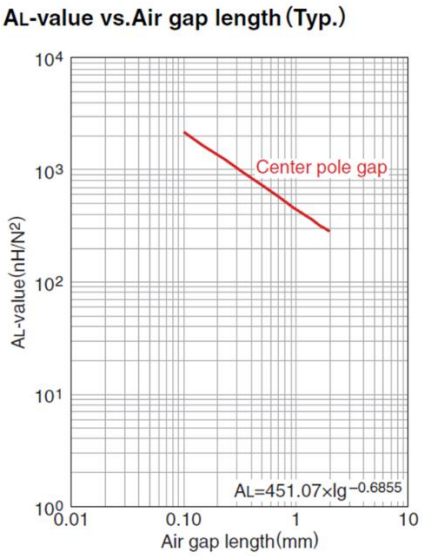


Figure 3. 13: The diagram of the inductance per turn value A_L for a specific core

As shown in Fig.3.13, A_L will decrease when increasing the air gap length. Besides, it provides an equation for the air gap length and A_L. The relationship between air gap length and A_L is given in equation (3.17).

$$A_L = 451.07 \times \log_{10}(g_m)^{-0.6855} \tag{3.17}$$

After the A_L value is determined at the defined air gap length g_m, the number of turns can be calculated with the required inductance, as shown in equation (3.18).

$$N = \sqrt{\frac{L}{A_L}} \tag{3.18}$$

With the calculated number of turns, the window utilization factor k_u can be calculated by the total area of the selected Litz wire (as shown in Table 3.11) over the core window area A_w, as shown in equation (3.19).

$$k_u = \frac{N \times Total\ area}{A_w} \tag{3.19}$$

Finally, with the selected core and the above-designed winding, we can calculate the inductor power losses. The loss model for the inductor is discussed as follows.

2) Inductor loss model

A practical inductor can be modeled as an ideal inductor connected in series with a resistor (DCR1 and DCR2), as shown in Fig.3.6. In power inductors, there are two major losses, including winding loss and core loss.

- Winding losses

  The accurate winding loss model of the inductor is very complicated. The inductor current contains a portion of high-frequency components (ripples) with a DC component. These high-frequency currents will cause large AC winding losses due to skin effects, proximity effects, and fringing effects in the inductor. Due to the limitations of time, the AC winding loss model is not analyzed in this study. The accurate AC winding loss model of the inductor is necessary for further optimization.

- Core loss

  High-frequency current will introduce a high-frequency magnetic field in magnetics, resulting in core losses. These losses highly depend on switching frequency as well as current ripple.

a) Winding loss

The current i_1 flows in the winding of the inductor L_1 will cause power loss due to the resistance of the winding. As shown in Fig.3.7, the inductor L_1 current i_1 is composed of a DC current (I_1=50A) and a small portion of high-frequency AC current (triangular waveform). Therefore, it will introduce two types of winding loss in the inductor [4], as summarized below.

- DC loss

DC loss is caused by a DC current flowing into the winding. It is very easy to calculate this DC loss, as shown in equation (3.20).

$$P_{DC} = MLT \times N \times \frac{\rho_w}{A_{con}} \times {I_1}^2 \quad (3.20)$$

, where ρ_w is the resistivity of the conductor at the operating temperature, and I_1 is the DC value of the output charging current (50A).

- AC loss

In power electronics applications, high-frequency AC current will induce AC winding loss due to skin, proximity, and fringing effects[15]. These effects will not be discussed in detail in this study.

According to Faraday's law, if an AC current flows into a conductor, it will cause a non-uniform distribution of current in the conductor. This non-uniform distribution phenomenon will reduce the effective cross-section area of the conductor (much smaller than the physical cross-section area). Therefore, AC resistance will be larger than the DC resistance (about 3 times the DC resistance) [15].

However, the RMS value of AC current is usually much smaller than that of the DC current. Taking this study as an example, as shown in Fig.3.7, the inductor current is composed of a 50A DC current plus a triangular AC current with Δi_1 peak-to-peak current. As discussed, Δi_1has not been finally defined, this will be defined in Section 3.3.3. But, for power inductors, Δi_1usually is among 20%-60% of the DC current (50A) for a good design [13]. Taking 40% as the worst case, Δi_1 is about 20A. The RMS value for this triangular current is calculated as equation (3.21) [4].

$$RMS_{AC} = \frac{\Delta i_1}{2\sqrt{3}} = 5.7A \quad (3.21)$$

As can be seen from equation (3.21), the RMS value of the AC current is nearly 10 times smaller than the DC value 50A. The squared value of the AC RMS value is even smaller (nearly 1% of that DC squared value). Therefore, the AC loss is negligible in this study.

b) Core loss

In inductors, core losses are introduced by the hysteresis effect and eddy current in the core induced by AC current. A detailed illustration of this effect can be found in [16]. This thesis uses the celebrated general Steinmetz equation [16] to calculate the core loss per unit volume, as shown in equation (3.22).

$$P_{fe} = K_c f_{sw}^{\alpha} (\frac{\Delta B}{2})^{\beta} \quad (3.22)$$

, where P_{fe} is the core (ferrite) loss per unit volume. f_{sw} is the switching frequency. The AC current will induce changing magnetic flux density in the core, and ΔB is the peak-to-peak value of the alternating flux density in the core. The typical constants [13] for ferrite material are summarized in Table 3.12.

Table 3. 12: Typical constants for ferrite material

Parameters	Value
K_c	16.9
α	1.25
β	2.35

Overall, the inductor losses have been analyzed. DC loss is calculated based on the selected core and lite wire. Core loss is calculated by the general Steinmetz equation. While AC loss is usually a very small portion (<2% of the winding loss) of the winding loss. In this study, only the DC loss and core loss models are considered. With the loss models, the optimization method is introduced in Section 3.3.

3.2.3 Other losses

As shown in Fig.3.6, a practical capacitor is modeled as an ideal capacitor connected in series with a resistor (ESR). For a well-designed LCL filter, nearly all the current ripples Δi_1will flow through the capacitor. Thus, the current waveform of i_c is the same as the triangular waveform (Δi_1), as shown in Fig.3.7. The power loss of the capacitor ESR can be calculated as shown in equation (3.23)[4]

$$P_{C_{loss}} = ESR \times I_{cRMS}^2 = ESR \times \frac{1}{12} \times {\Delta i_1}^2 \tag{3.23}$$

, where Δi_1 is the peak-to-peak value of the inductor L1 current ripple.

The total converter loss model is summarized as equation (3.24).

$$P_{RDC} = P_{C_{loss}} + P_{S1_{sw}} + P_{S2_{sw}} + P_{S1_{con}} + P_{S2_{con}} + P_{S3_{con}} + P_{ind} \tag{3.24}$$

, where $P_{S3_{con}}$ is the conduction loss of S3. As discussed above, the conduction loss of S3 is the same as that of S2. P_{ind} represents the inductor loss. The physical inductor has not been designed. This loss will be investigated together with the inductor design method in Section 3.3.

In this study, the loss model (equation (3.24)) forms the basis of the optimization of the RDC converter.

3.3 Optimization Method

The converter loss model has been analyzed and illustrated, as shown in equation (3.24). This forms the basis for the efficiency (equation (3.2)) of the RDC converter. From the equations in Section 3.2 above, we can see that the efficiency relates to the switching frequency f_{sw} and current ripple Δi_1. Increasing the switching frequency will obviously increase the loss. Different current ripples will also bring different losses. For the power density (power/volume), different f_{sw} and Δi_1 will significantly affect the volume, so as to affect the power density. This subsection will discuss how f_{sw} and Δi_1 affect the volume with a classical inductor design method.

In Section 3.2, we have derived the semiconductor loss model and inductor loss model from the practical design point of view. Achieving high efficiency and high power density are two major goals in power electronics design. However, usually, these two aspects are contradictory to each other.

- On one hand, when increasing the switching frequency, the required inductance will be reduced, so that the physical size of the inductor will usually be reduced.
- On the other hand, as discussed in Section 3.2, the switches (semiconductor) loss as well as inductor AC loss will be increased under high switching frequency.

Therefore, it is possible to find an optimal point, where high efficiency can be achieved while maintaining good power density. The optimization method is illustrated step by step.

3.3.1 Design Freedom

To optimize the converter, the design freedom should first be investigated. Since the inductor will be the most bulky component in the converter. The size of the inductor should be analyzed. As discussed in Section 3.3.1, the inductor size is calculated by equation (3.14). Though Ap is the area product, it is usually used to represent the size of the inductor.

From equation (3.14), we can find that the size is affected by several parameters. In detail, the switching frequency f_{sw} and the inductor L_1 current ripple Δi_1 are the design freedom to optimize the RDC converter. The other parameters are determined by circuit specifications as well as empirical data, which are usually unchangeable. Besides, as discussed in Section 3.2, switching frequency f_{sw} and inductor L_1 current ripple Δi_1 will affect the switches (semiconductor) losses. Regarding to this, the RDC converter hardware optimization is to find the optimal f_{sw} and Δi_1. In this RDC converter (relatively high power), a reasonable range of the switching frequency is between 10 kHz and 200 kHz for MOSFETs. The current ripple Δi_1 range is analyzed from 2A to 60A.

3.3.2 The Design Procedure

The detailed design procedure for the optimization is shown in Fig.3.13. Within the pre-defined switching frequency range and current ripple range, f_{sw} and Δi_1 are discretized first. Within the range, the switching frequency step is 5kHz, so we have 39 different switching frequency values. For Δi_1, the step is 2 A, so the number of the different current ripples is 30. In total, we have 1170 different combinations, which we call it points in the rest of the discussion.

For each discretized f_{sw} and Δi_1, the design process and calculation in Fig.3.14 is repeated. The total number of repetitions is 1170.

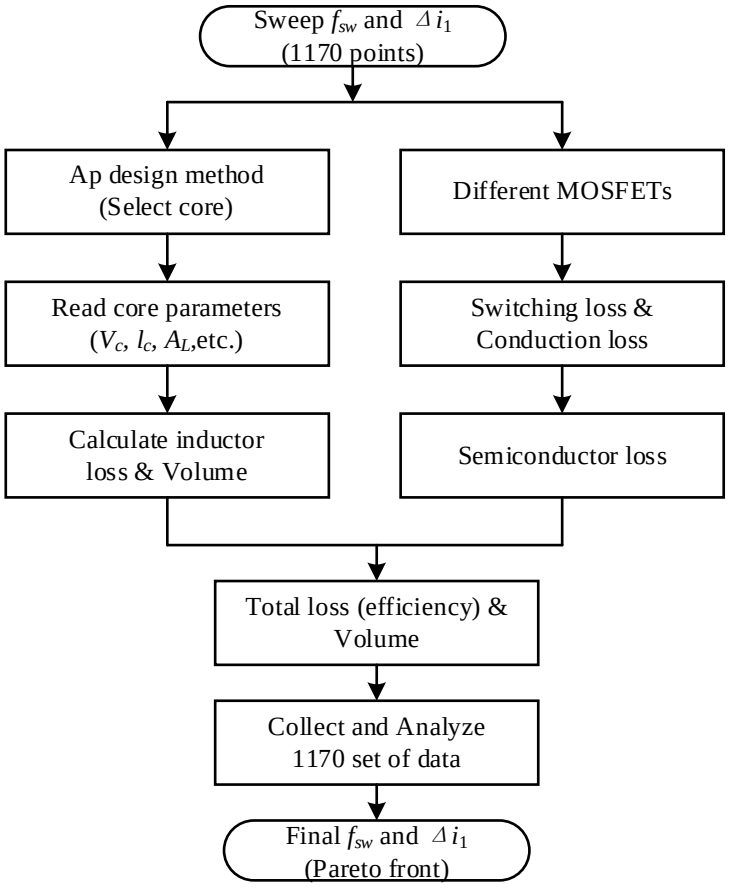


Figure 3. 14: General Process of the optimization method

First, the *Ap* is calculated by each f_{sw} and Δi_1. Later, the calculated *Ap* is compared to the arear product of all the cores in the core library. The core with the most similar area product value (slightly larger than the calculated *Ap*) is selected then.

Then, based on the selected core, the parameters of the selected core are read from the core library. The calculation of turns N and air gap length is given in Section 3.2.2. The window utilization factor k_u can also be calculated and compared to 0.4. If k_u is large 0.4, it could mean

that the winding might not be able to fit in the window of the core. If this happens, a bigger core should be selected. The above procedure will be repeated.

With the selected core and designed inductor, the inductor loss and semiconductor loss will be calculated. The efficiency of the RDC converter (20 kW) can be easily calculated by the total loss. The efficiency of the RDC converter and the volume of the inductor are saved in a matrix for later analysis.

Finally, for all the discretized values of f_{sw} and Δi_1, the design is repeated. The results are collected and analyzed below.

3.3.3 Results Analysis

As discussed above, for each of the discretized values of f_{sw} and Δi_1, the efficiency of the RDC converter and the volume of the inductor are calculated by the design method. For the power density, the total converter volume should be considered. It is very hard to calculate the total volume since the RDC converter has not been built. The inductor is the most bulky component of the RDC converter. The inductor volume is selected to represent the converter volume. All the data is summarized and plotted in Fig.3.15.

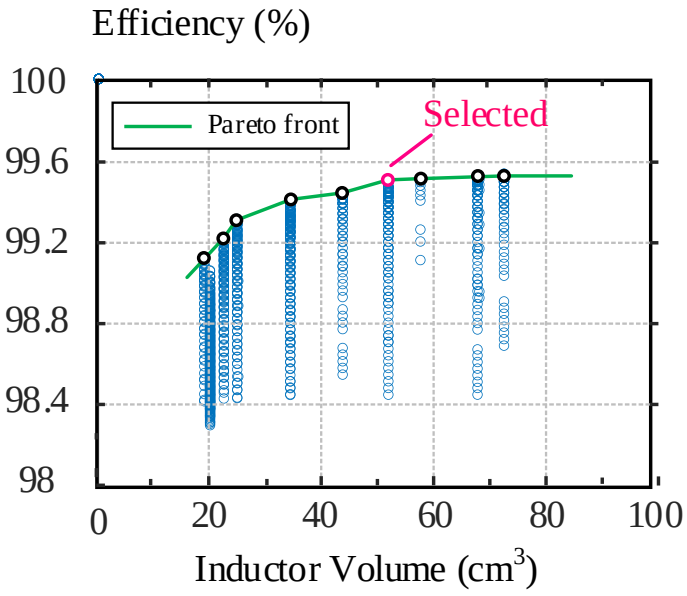


Figure 3. 15: Efficiency and Inductor volume for all the discretized values of f_{sw} and Δi_1.

In Fig.3.15, the blue 1170 scatted points are first plotted. Since we have a limited number of cores available, in this case, only 10 cores are selected in the core library. From the drawn blue points, we can clearly see that there are 10 sets of points distributed horizontally. For each column (set), the points are basically aligned vertically at the same volume. The points in the

same set are actually using the same size of core. (Even though the f_{sw} and Δi_1 are different for each point, their multiplication (*Ap* calculation) could be close to each other, so that the core is selected by different points, according to equation (3.14).)

The green line is the so-called Pareto front, where the highest efficiency points can be found for each size of the core. As can be seen in the green line, the efficiency will increase when sacrificing the power density (using a larger core). However, when it reaches the red point shown in Fig.3.15, using a larger core (bigger volume) can not further increase the efficiency of the RDC converter too much. This means that this point is the optimal point where efficiency is very high (about 99.4%) while the volume is relatively small.

This red point is selected in this study for the final design of the RDC converter. With the selected optimal point, the key parameters from the calculation (as shown in Fig.3.14) of this point are summarized in Table 3.13.

Table 3. 13: Key parameters from the calculation of the selected point (f_{sw} and Δi_1)

Parameters	**Value**
f_{sw} / *kHz*	40
Δi_1 / *%*	40% (20A)
P_{all} / *W*	114.51
Efficiency / % (Calculated)	99.4
Core type	PC47PQ60/52-Z
Ap /cm^4	22.56
V_c / cm^3	56.24

In conclusion, the switching frequency and current ripple are 40 kHz and 20A respectively. The rated output current (DC value only) is 50A. With the max EV voltage (about 400V), the power of the RDC converter is about 20 kW. As discussed in Fig.3.14, the total loss is calculated to be 114.51 W. And the efficiency of the RDC converter is about 99.4%, this efficiency will then be verified in Section 5.2. Besides, the magnetic core is also selected. The core part number is PC47PQ60/52-Z from TDK company. It has 56.24 cm^3 total volume.

3.4 Parameters Design

As discussed in Section 3.3, the optimal switching frequency f_{sw} and inductor L_1 current ripple Δi_1 have been determined. This subsection will discuss the design of the circuit parameters with respect to the optimal operating f_{sw} and Δi_1.

The main component L_1 has been initially designed in the optimization method. However, other components have not been designed and selected yet. This subsection will illustrate the design procedures and summarize the designed parameters for other components.

3.4.1 LCL Filter Parameters Design

LC filters are the most used filters for buck topologies[4]. However, in fast charging of EV batteries, an LC filter is not enough. A battery is modeled as a voltage source with a very small internal resistance [17], this can be modeled as a short circuit at high frequency. Therefore, the output current ripple will flow into the EV battery rather than the filter capacitor, which is unacceptable.

To avoid this, an additional inductor L_2 is introduced and needs to be designed, as shown in Fig.3.2. At high frequency, the impedance ($Z=j2\pi f L_2$) of L_2 is very large so that it will prohibit the high-frequency current ripples from the converter flowing into the EV.

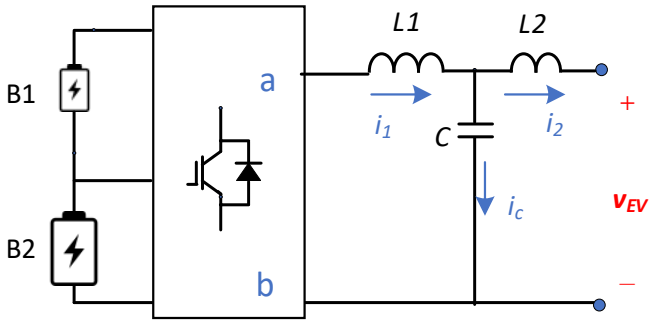


Figure 3. 16: RDC converter with LCL filter

The LCL filter is composed of two inductors L_1 and L_2 and a capacitor C. The additional capacitor branch can bypass high-frequency current ripples. On the left-hand side of the LCL filter, BESS (B1 and B2) and power switches form the topology of the RDC converter. On the right-hand side of the LCL filter, the EV battery connects to the output of the LCL filter. Ideally, the LCL filter bypasses all the ripples from the input side and only allows the DC component to flow into the EV battery.

When designing an LCL filter [24], the following two constraints must be taken into account.

- Voltage and current ripple requirements for the EV battery. Table 3.6 shows the current and voltage ripple limits of different sources. For example, the Tesla Supercharger

provides DC power to EVs with 2% current ripples and 0.1V voltage ripples. The LCL filter parameters need to be designed to meet these limitations.

- Current ripple at the converter side. This has been discussed in Section 3.2.

In this section, a parameter design procedure of LCL is illustrated. Fig. 3.17 shows a simplified equivalent circuit of the LCL-type RDC converter. According to the working principle of buck converter, as discussed in Section 2.1.1, the current waveforms of i_1, i_2, and i_c have also been presented in Fig.3.17.

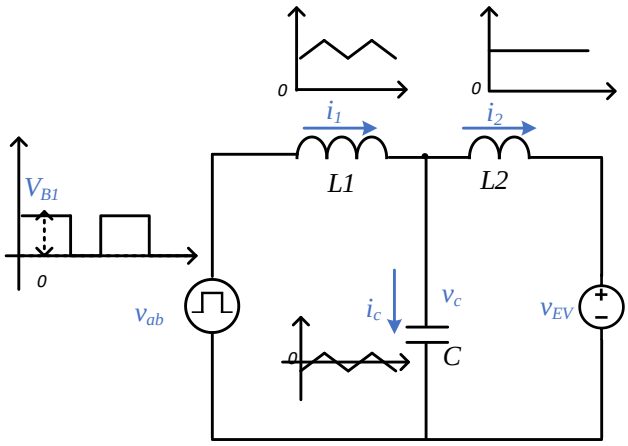


Figure 3. 17: Equivalent circuit of LCL-type RDC converter

On the left-hand side of the LCL filter, the PWM voltage waveform v_{ab} is generated by power switches and BESS (B1 and B2). This PWM voltage waveform contains a DC component with a large number of ripple components, as shown in Fig.3.17. This is the input of the LCL filter. On the right-hand side, the EV battery is represented by a DC voltage source v_{EV}, assuming nearly all the ripples have been bypassed by the LCL filter.

The design procedure for this LCL filter is illustrated step by step as following [25], [26], [27].

1) Converter-side inductor L_1 design

For the L_1 design, since the voltage ripple (0.4V) on the capacitor is very small compared to the output EV voltage (up to 403V), v_c is assumed to be a DC voltage (403V). The PWM voltage of v_{ab} applied on the inductor L_1 will first introduce a triangular current waveform, as discussed in Section 2.1.1.

During one switching cycle of the RDC converter:

- When S1 is on and S2 is off, v_{ab} equals V_{B1}. The voltage across the inductor L_1 is $v_{L1} = V_{B1} - V_c$. The current i_1 increases to its peak value.

- When S1 is off and S2 is on, v_{ab} now is 0. The voltage across L_1 is then $-V_c$. The inductor current i_1 decreases to its minimum value.

At the steady state, the behavior of the inductor L_1 current waveform i_1 will repeat in the next switching cycle. According to Section 2.1.1, the ripple of i_1 (peak-to-peak) is calculated as follows.

$$\Delta i_1 = \frac{V_{B1} - V_c}{L_1} DT_{sw} \tag{3.25}$$

, where DT_{sw} is the duty cycle, T_{sw} is the switching period.

Substitute the V_c with $D*V_{B1}$ in equation (3.25), we get

$$L_1 \geq \frac{V_{B1max}(D - D^2)_{max}}{\Delta i_1 f_{sw}} \tag{3.26}$$

, where f_{sw} is the switching frequency. V_{B1max} is the maximum input voltage. For the optimal ripple Δi_1 and switching frequency f_{sw}, L_1 can be designed. Usually, some design margins should be given, in this case, the inductance might be larger than the calculated value in equation (3.26). The inductor L_1 detailed parameters (turns, loss, etc) will be illustrated in Section 3.5.

2) Filter capacitor C design

The capacitor is designed to limit the voltage ripple at the steady state. At the steady state operation, the capacitor absorbs all the ripple current, as shown in Fig. 3.17. This ripple current i_c charges and discharges the capacitor in one switching cycle. Thus, the voltage v_c varies. It is calculated as follows,

$$\Delta v_c = \frac{V_{B1max}(D - D^2)max}{8 L_1 C f_{sw}^2} \tag{3.27}$$

As shown in Table 3.6, the voltage ripple requirement is selected to be 0.4V. Therefore, the initial capacitance can be calculated by substituting the ΔV_c with 0.4V, as shown in equation (3.28).

$$C \geq \frac{V_{B1max}(D - D^2)}{0.4 \times 8 f_{sw}^2 L_1} \tag{3.28}$$

The voltage ripple caused by the ESR (see Fig.3.6) of the capacitor has not been included now. Therefore, the required capacitance should be larger than the calculation in equation (3.28). The capacitor selected will be discussed in Section 3.5.

3) EV side inductor L_2 design

The parameter design of L_2 is driven by the current ripple requirement at the EV side. The converter side current i_1 has a peak-to-peak ripple. This ripple will be further reduced by the filter capacitor C and the EV side inductor L_2.

To design L_2, the transfer function of i_1 to i_2 is derived as follows[19]

$$\frac{i_2}{i_1} = \frac{1}{1 + L_2 C s^2} \tag{3.29}$$

According to Table 3.6, the EV side current ripple should be less than 5% (peak-to-peak). Considering the converter side ripple (40% as shown in Table 3.13), L_2 can be designed by giving enough suppression to the ripple from i_1. As shown in equation (3.29), the magnitude of the right-hand side expression should be less than 1/8 at the switching frequency 40 kHz. Therefore, the inductance of L_2 can be calculated as follows.

$$L_2 \geq \frac{7}{C(2\pi f_{sw})^2} \tag{3.30}$$

The minimum required inductance is a little bit small. According to [25], the inductance of L_2 should be larger. This will be discussed in Section 3.5.2. Overall, the main design process for the LCL filter has been illustrated above. The parameters of the LCL filter are summarized in Table 3.14.

Table 3. 14: Designed Parameters for LCL filters

Parameters	Value
L_1 / μH	31.25
C / μF	220
L_2 / μH	0.5

3.4.2 Input Filters Design

Input filters are necessary and important for a power circuit design to pass the EMC test. In this case, the main purpose is to suppress the ripples from going back to the batteries. LC filters are the ones that are often used in filter circuits. Figure 3.18 shows the RDC converter with the LC input filters under mode 1. L_{f1} and C_{f1} compose the input filter for the B1, while L_{f2} and C_{f2} are to reduce ripples flowing into the B2. Under mode 1, both input filters are working in the circuits, which makes the converter to be a multi-port system. Under mode 2 (simply a buck converter), the B1 is cut from the main circuit. Therefore, only the input filter (L_{f2} and C_{f2}) of the B2 is working.

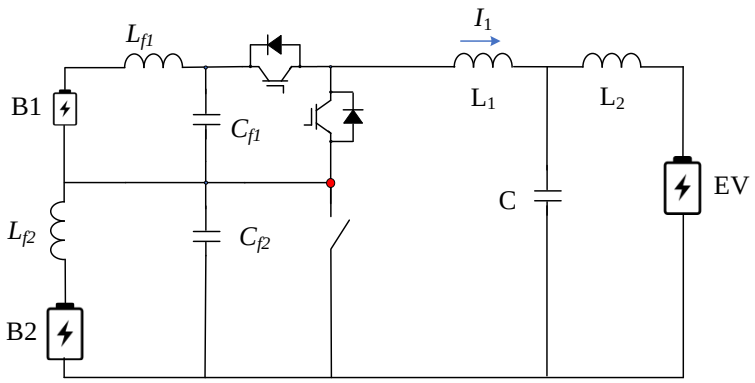
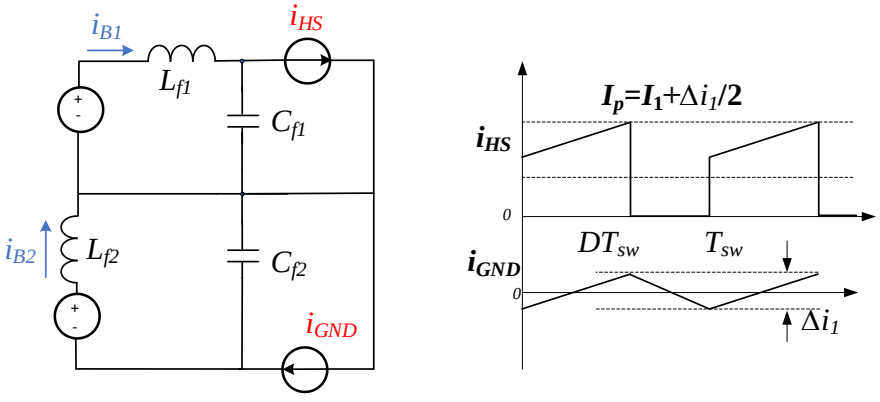


Figure 3. 18: Circuit diagram of the RDC converter including LC filters.

Similarly to EV batteries, the input batteries (B1 and B2) also limit the current ripples flowing into them. As mentioned in Table 3.6, the maximum current ripple requirement for batteries is 5% peak-to-peak, and the maximum voltage ripple is 0.4V. The input filter design is to first meet the ripple requirements for the batteries.

Figure 3.19 (a) illustrates the equivalent circuit of the RDC converter at the input side. The B1 and B2 are modeled as a voltage source. The rest of the converter are modeled as two current sources i_{HS} and i_{GND}, to simplify the analysis. As shown in Fig.3.7, we know the principle current waveforms for the RDC converter. The current waveforms i_{HS} and i_{GND} are extracted, as shown in Figure 4.10 (b). i_{HS} represents the ripple current flowing into the high-side switch S1, while i_{GND} is the ripple current flowing into the ground.

For two input filters, the ripple currents are different. Therefore, the parameters of the two input filters will be different. The design procedure for these two input filters will be discussed below.

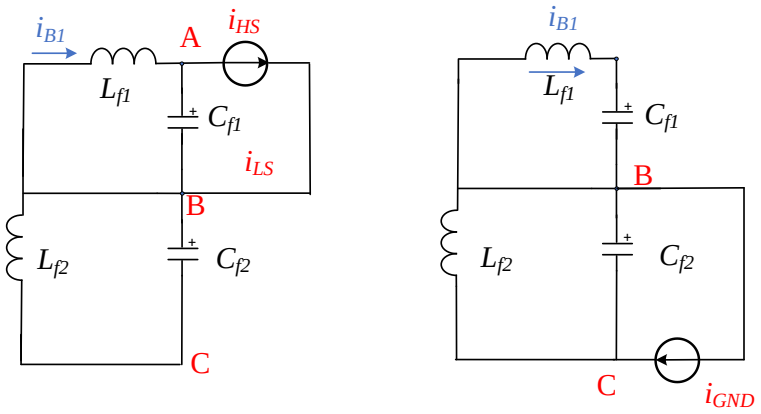


(a) Equivalent circuit (b) Ripple Currents

Figure 3. 19: The equivalent circuit and associated current waveforms of the converter at the input side

1) LC filter for B1

Based on the equivalent circuit in Figure 3.19 (a), we know that both current ripples i_{HS} and i_{GND} might flow into B1. To analyze the influence of the two ripple currents for B1, the superposition principle is applied. The equivalent circuits for two independent current sources are derived, as shown in Figure 3.20.



(a) Current source i_{HS} (b) Current source i_{GND}

Figure 3. 20: The equivalent circuits to analyze ripples into B1 from two independent current sources

For the current source i_{HS} in Figure 3.20 (a), we can simplify the equivalent circuit to Figure 3.21. From Fig.3.21, we can see that the LC filter (L_{f1} and C_{f1}) is to reduce the ripples from the current source i_{HS} to B1. For the current source shown in Fig.3.20 (b), the current source i_{GND} will not affect Bat1, since the branch of L_{f2} and C_{f2} has been bypassed. Therefore, L_{f1} and C_{f1} can be designed by meeting current and voltage ripple requirements.

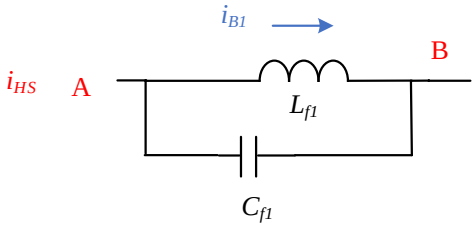
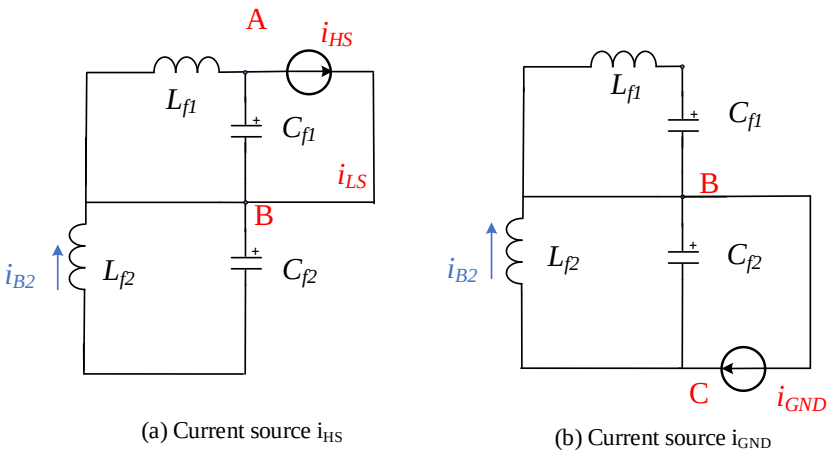


Figure 3. 21: The simplified equivalent circuit to analyze ripples into B1 from i_{HS}

2) LC filter for B2

Similarly, for B2, we can get the equivalent circuits for the two current sources separately, as shown in Fig.3.22.



(a) Current source i_{HS} (b) Current source i_{GND}

Figure 3. 22: The equivalent circuits to analyze ripples into B2 from two independent current sources.

Fig.3.22 (a) shows the B2 current ripple caused by the current source i_{HS}, while Figure 3.22 (b) shows the B2 current ripple caused by the current source i_{GND}. Similarly, the current source i_{HS} will not affect B2. The simplified equivalent circuit to analyze the current ripples from current source i_{GND} to B2 is derived and shown in Fig.3.23.

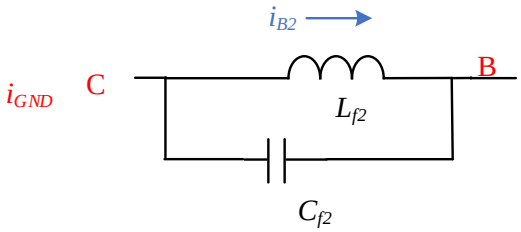


Figure 3. 23: The simplified equivalent circuit to analyze ripples into B2 from i_{GND}.

With the simplified equivalent circuits shown in Fig.3.21 and Fig.3.23, we can design the two LC filters to meet the voltage and current requirements for batteries (B1 and B2). The design procedure for the two LC filters is the same. Here, the input filter (L_{f2} and C_{f2}) is taken as an example to illustrate the procedure.

The transfer function from i_{GND} to i_{B2} is derived, as shown in equation (3.31).

$$\frac{i_{B2}(s)}{i_{GND}(s)} = \frac{1}{1 + s^2 L_{f2} C_{f2}} \tag{3.31}$$

From the transfer function, we can calculate the current ripple i_{B2} from i_{GND}. In other words, considering the current ripple requirement (5%, see Table 3.6) of the B2 and magnitude of i_{GND}, we can get one equation for the calculation of L_{f2} and C_{f2}.

From the voltage ripple requirement (0.4V, see Table 3.6), we can select a practical capacitor on the market and get the capacitance for the input LC filter. A practical selection method for the capacitor is illustrated in Fig.3.28.

With equation (3.31) and the voltage ripple requirement of the B2, a practical design procedure of the input LC filters is introduced in Fig 3.24.

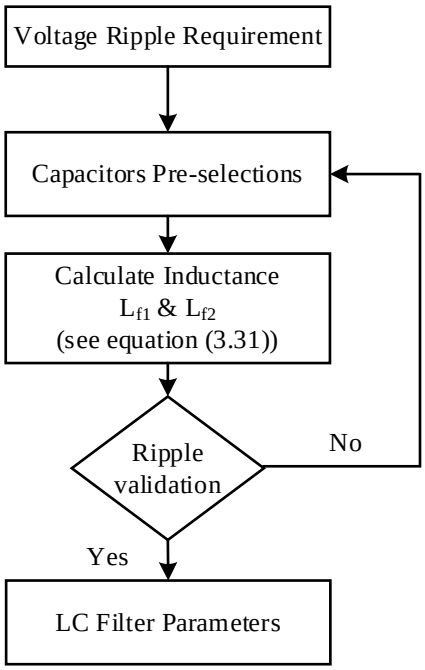


Figure 3. 24: The practical design procedure of the input LC filters considering current and voltage ripple requirements.

The general process is to first select suitable capacitors on the market to guarantee the voltage ripple is small enough. With the pre-selected capacitors, the inductor L can be calculated by the current ripple requirement. Finally, validations of the ripples of the LC filter should be made to make sure the designed parameters can provide sufficient suppression for the current and voltage ripples. Several iterations need to be taken to make the final design. Table 3.15 shows the designed input LC filters for the RDC converter.

Table 3. 15: The designed parameters for the input LC filters.

C_{f1} / μF	C_{f2} /μF	L_{f1} /μH	L_{f2} /μH
400	100	9	16

The designed input filters are not physically implemented in the experiments in Section 5 due to time limitations. However, the control system stability including the designed input filters will be discussed in Section 4.3.

3.5 Components Selection

In the previous sections, the optimal operating f_{sw} and Δi_1 of the RDC converter and its main circuit parameters have been determined. This subsection will illustrate the detailed procedures of the components selection for the 20 kW RDC prototype.

3.5.1 Power Switches

There are various types of power switches available on the market. In [28], the running rated voltage and current (usually maximum breakdown voltage) for different power switches are summarized in Fig.3.25.

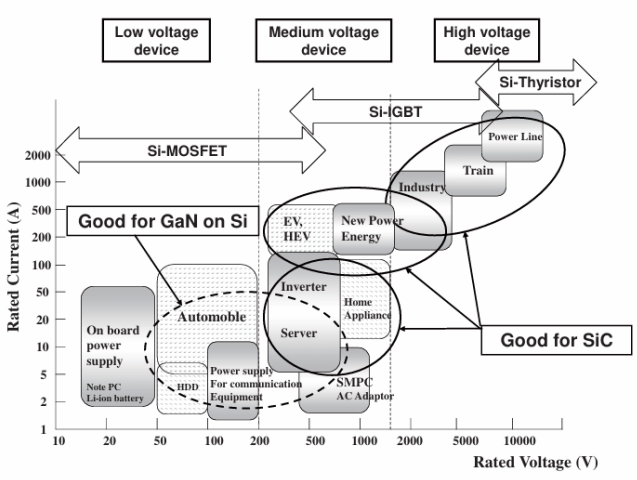


Figure 3. 25: Power semiconductor devices and their applications [28]

As shown in Fig.3.25, for EVs, several types of power switches are available, like Si-IGBT, Si-MOSFET, SiC MOSFET, etc. The benefits and limitations of each type of power switch are illustrated shortly as follows.

- GaN devices are recently developed for extremely high frequency (MHz) applications. However, it is mostly applied in low-power applications (up to 1.5 kW). It is not suitable for the high-power applications in this study.
- Si MOSFETs are suitable high frequency, for low voltage (up to 600V), and relatively high current applications [29]. The most important benefit of Si-MOSFET is the low price and availability.
- SiC MOSFETs are the recently developed high-frequency power switches for higher voltage applications (600V - 1200V, even higher). It is very expensive (10 times more than Si-MOSFETs).

- IGBTs are for high power and high voltage applications. But its switching frequency can only go up to 20 kHz. As discussed in Section 3.3, this low switching frequency operation will make the converter very bulky.

In this design, since the switching frequency is settled to be 40 kHz, the IGBT devices are not suitable. Si MOSFETs and SiC MOSFETs are selected. As shown in Fig.2.8, we can easily analyze the voltage for each power switch. The conclusions are summarized as follows:

- For S1 and S2, the voltage applied on them is v_{B1} (<125V). Therefore, the rated voltage is relatively low. But the current is about 50A, as mentioned in Section 3.1. Considering the low cost of Si-MOSFET, it is the perfect candidate for S1 and S2.
- For S3 and S4, the voltage applied on them is v_{B2} (>300V). For this voltage range, both Si MOSFET and SiC MOSFET are suitable. In this study, both SiC MOSFET are selected and tested, due to the better switching performance as well as higher efficiency than Si MOSFET [29].

According to the discussion above, the selected Si MOSFETs and SiC MOSFETs are summarized in Table 3. The selected Si / SiC MOSFETs will be implemented in the RDC converter and tested in Section 5.

Table 3. 16: The part numbers of the selected Si/SiC MOSFETs

Power Switches	Part Number
S1&S2	IRF300P226
S3&S4	C3M0015065K

3.5.2 LCL Filter

As discussed in Section 3.4.1, the parameters of the LCL filter have been designed. In this subsection, the components of the LCL filter will be selected.

1) Inductor L_1. (Main Inductor)

According to Table 3.13, the initially selected core is PC47PQ60/52-Z. Unfortunately, this core is not immediately available. Therefore, another core (B65982Q0400K097) is selected, as shown in Fig.3.26. This core is ordered together with its coil former CF-PQ65/60-V-1S-16P.

Figure 3. 26: The physical model of the magnetic core B65982Q0400K097

It has a slightly larger size (*Ap*) than PC47PQ60/52-Z. For the RDC prototype, it is reasonable to choose a bigger core, in order to guarantee the assembled inductor can provide enough inductance. The main parameters of the selected core are summarized in Table 3.17.

Table 3. 17: The parameters of the core B65982Q0400K097

Parameters	Value
A_c /cm^2	6.0
l_c /cm	13.7
A_w /cm^2	5.31
Ap /cm^4	31.86
V_c /cm^3	81.95
MLT / cm	12.77
Air gap	Distributed air gap
A_L / nH/N^2	400

As shown in Table 3.17, this core has a distributed air gap. According to [30], the distributed air gap will lead to lower loss. The air gap length of B65982Q0400K097 is not adjustable. Therefore, in this case, the air gap length will not be designed.

According to equation (3.20), the number of winding turns can be calculated as follows.

$$N = \sqrt{\frac{L_1}{A_L}} = 8.6 \tag{3.32}$$

The winding turns N are determined to be 8. According to Table 3.11, this Litz wire is pre-selected. Based on the Litz wire parameters in Table 3.11, the total area (cross-section) of the Litz wire is about 22.40 mm^2. The window utilization factor can be calculated as follows.

$$k_u = \frac{N \times Total\ area}{A_w} = \frac{8 \times 22.40 \times 10^{-6}\ m^2}{5.31 \times 10^{-4} m^2} = 0.34 < 0.4 \tag{3.33}$$

Since k_u is calculated to be 0.34 (<0.4), the windings can fit in the magnetic core. The designed inductor L_1 (core and windings) will be assembled and tested in Section 5.

2) Capacitor C

According to Table 3.14, the capacitance of C has been calculated. However, a practical capacitor is a non-ideal component. A real capacitor is modeled as an equivalent series resistor (ESR) connected in series with an ideal capacitor, as shown in Fig.3.27.

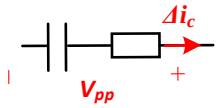


Figure 3. 27: The circuit model of a practical capacitor

When the ripple current Δi_c flows into the capacitor, the ESR will lead to two consequences as follows.

- It will introduce power loss in the capacitor, as shown in equation (3.14).
- According to Ohm'law, the ripple current will introduce a voltage ripple across the capacitor.

Considering the ESR, the additional voltage ripple across the capacitor can be calculated as follows

$$\Delta V_{cESR} = ESR \times \Delta i_c \tag{3.34}$$

, where Δi_c is the same as Δi_1. Adding equation (3.34) and equation (3.27), the total voltage ripple across the capacitor can be calculated as follows.

$$V_{pp} = \Delta V_c + \Delta V_{cESR} = \frac{V_{B1max}(D - D^2)max}{8L_1 C f_{sw}^2} + ESR \times \Delta i_c \tag{3.35}$$

Since a very restricted voltage ripple (0.4 V) requirement is needed for the RDC converter, a low ESR capacitor should be selected. Film capacitors are selected in this study due to their low ESR. According to [31], a practical design selection method has been illustrated in Fig.3.28.

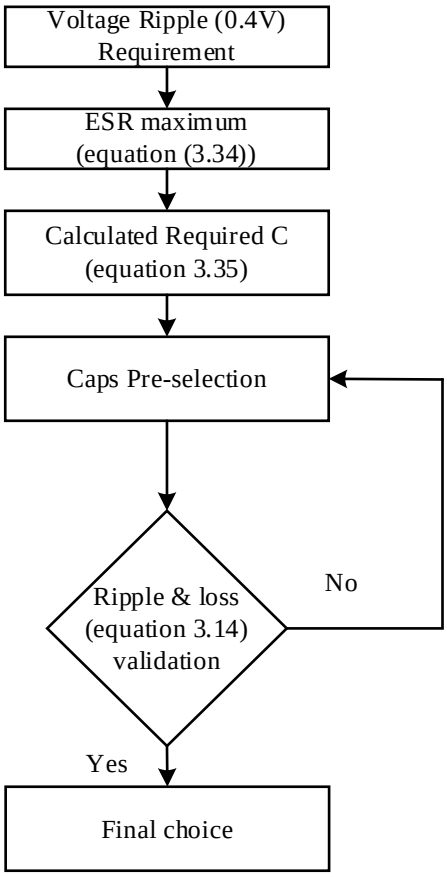


Figure 3. 28: A practical design selection method for the capacitor C.

In Fig.3.28, we start with the voltage ripple requirement for the RDC converter. The detailed explanation of the practical design method is illustrated step by step below.

First, we can determine the maximum ESR by equation (3.34) and ripple requirement. Several film capacitors with a ESR lower can be selected as possible candidates (If the ESR is too large, the voltage ripple caused by ESR is already larger than 0.4V).

Second, calculate the required capacitance by equation (3.35). We can pre-select several film capacitors available on the market.

Then, the ripple and loss (equation (3.14)) of the selected capacitor will be calculated. If the ripple is higher than the requirement, a different capacitor should be selected. If the power loss in the capacitor is higher than the maximum allowed loss of the selected capacitor, a different capacitor should be considered.

Finally, in this design, B32718H8117K000 is selected. Two B32718H8117K000 are paralleled to form the capacitor C. The main parameters of the selected capacitor B32718H8117K000 are summarized in Table 3.18.

Table 3. 18: The main parameters of the selected capacitor B32718H8117K000

Parameters	Value
Capacitance / μF	110
ESR / mΩ	2.8
Rated DC voltage / V	650
Max allowed (RMS) / A	33.5

Based on the parameters in Table 3.18, we can re-calculate the voltage ripple as follows.

$$\Delta V_c = \frac{V_{B1max}(D - D^2)max}{8L_1Cf_{sw}^2} + ESR \times \Delta i_c = 0.38V\ (< 0.4V) \qquad (3.36)$$

The calculated voltage ripple is less than the ripple requirement (0.4V). The RMS value of the current ripple is calculated (3.23) to be about 5.7A (at 40% current ripple). This value is much lower than the rated RMS value of 33.5A of the capacitor in Table 3.18. This means that the power loss in the selected capacitor is much lower than its rated loss dissipation of the capacitor. The ripple current will not overheat the selected capacitor.

3) Inductor L_2

As discussed above, the inductor L_2 can be selected from the inductor market. Regarding the rated DC current (50A) of the RDC converter and the required inductance (equation (3.30)), B82559A5472A033 is selected for L_2. The parameters of B82559A5472A033 are shown in Table 3.19.

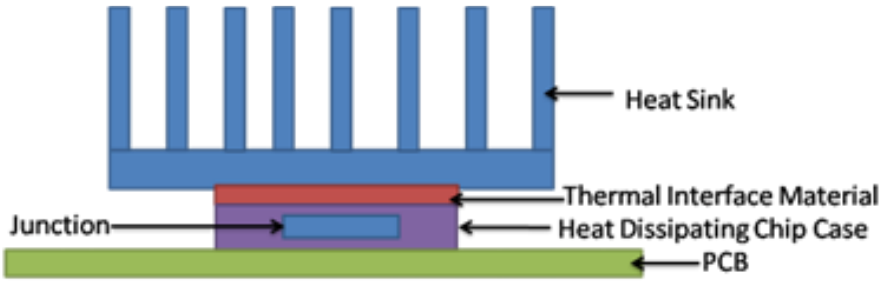
Table 3. 19: The main parameters of B82559A5472A033

Parameters	Value
Inductance / μH	4.7
DCR2 / mΩ	1.2
Rated Current / A	45.5

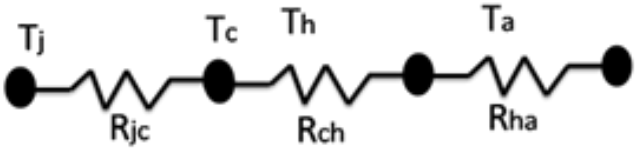
From Table 3.19, the inductance (4.7 μH) is higher than the required inductance of L_2 (see Table 3.14). This can help the LCL filter attenuate the current ripple from the inductor L_1. The current ripple (<5%) in L_2 will be tested and verified in Section 5. The rated current of the selected inductor is a little bit lower than 50A. It will introduce a little bit higher temperature in L_2 due to higher loss. During the experiment, a fan can help cool down L_2 and prevent L_2 from overheating.

3.5.3 Cooling Design

The power switch losses dominate in the RDC converter. The heat generated inside the MOSFETs due to the power loss should be sufficiently transferred to the ambient. According to [32], the thermal model of the MOSFETs with a heatsink is shown in Fig.3.29.



(a) Thermal structure



(b) Thermal resistance

$$R_{ja} = R_{jc} + R_{ch} + R_{ha} = \frac{T_j - T_a}{Q}$$

Figure 3. 29: The thermal model of the MOSFETs with a heatsink [32].

As shown in Fig.3.29 (a), the thermal system is composed of two parts, as follows.

- The thermal pad: The MOSFETs are first attached to a thermal pad. The thermal pad is to provide enough galvanic isolation between the MOSFETs and heatsink as well as isolate each MOSFET from each other.
- Heatsink (with a fan): The heatsink (usually with a fan) is installed above the thermal pad. It can significantly transfer the heat out to the ambient.

To simplify the thermal model, the thermal system can be simplified as a thermal resistance network, as shown in Fig.3.29 (b). T_j, T_c, T_h, T_a represent the temperature of the MOSFET junction, the case of the MOSFET, the heatsink, and the ambient respectively. R_{jc} is the thermal resistance of the MOSFET from the junction to the case. This parameter is usually given by the manufacturer. R_{ch} is the thermal resistance of the thermal pad. Usually, according to the parameters of the thermal pad, R_{ch} can be roughly calculated. R_{ha} is the thermal resistance of

the heatsink (This is given by the manufacturer). The thermal resistances are summarized in Table 3.20.

Table 3. 20: The thermal resistances of the different parts in the thermal system

Thermal resistance (K/W)	Value
R_{jc}	0.27
R_{ch}	unknown
R_{ha}	0.18

The initial thermal pad is taken from the lab. The thermal parameters of the pad are not clear. Therefore, the thermal resistance is unknown. With the known total loss (see Q in Fig.3.29) in the MOSFET, the junction temperature of the MOSFET T_j can be estimated by the equation shown in Fig.3.29. In other words, the maximum thermal resistance of the heatsink and the thermal pad is limited by the maximum allowed T_j of the MOSFET (This is given by the manufacturer) divided by the total loss (Q). The RDC converter is first tested with this thermal pad in Section 5.

3.6 Summary

In short, the hardware design of the RDC converter has been completed.

1) In Section 3.1, the voltage range of BESS (B1 and B2) was defined, to maintain regulation of the voltage of EVs while keeping low processing power of the RDC converter. The LCL filter parameter was designed according to the current charging standard for the voltage and current ripple.
2) The semiconductor loss model is analyzed in Section 3.2. Then, the inductor design method (AP method) is first discussed in Section 3.2.2. This gives a simple method of how to select a proper magnetic core from the market for a specific application. The DC loss and core loss of inductors have been analyzed. The converter loss model was derived for the optimization method.
3) Based on the total loss and volume of the RDC converter, a simple and practical optimization method is illustrated in Section 3.3, to optimize the efficiency and power density.
4) An optimal operating f_{sw} and Δi_1 for the RDC converter is selected. Based on the found f_{sw} and Δi_1, the detailed parameters of the final design for L_1 are determined, followed by the final parameter calculations for C and L_2 in the LCL filter.

5) With the designed parameters, the components of the RDC converter are designed or selected in Section 3.5. The cooling system is designed for the power switches.

4 CONTROL METHOD

In Section 2, the novel topology has been proposed and analyzed under different charging conditions. This section will illustrate the control design of the proposed topology since the control is essential to provide safe and smooth charging for EVs.

In fast EV charging, an EV battery is usually charged by constant-current (CC) during SOC increasing from 20% to 80% [33]. During this period, the voltage of the EV battery is increasing gradually. Constant-voltage (CV) charging is applied in the end (SOC:80%-100%) to protect the EV battery from over-voltage and the charging current decreases gradually.

In this study, CC charging is investigated. The mathematical dynamic model of the RDC converter was first analyzed and built, as shown in Section 4.1. In Section 4.2, a simple and straightforward PI controller was then designed to provide stable control for both modes. Section 4.3 analyses the stability of the control system including input LC filters. Finally, the designed PI controller was implemented in the DSP28379 control card.

A current feedback control loop was applied for the power converter. The output current of the RDC converter must be kept constant, regardless of changes in the input voltage or the output voltage (EV battery voltage). The feedback control system of the RDC converter is shown in Fig 4.1. In Fig.4.1, we can see that $i_{EV}(t)$ is not fed back to the controller. Instead, $i_1(t)$ is fed back. This is called converter-side current control. The reason for this will be discussed in Section 4.2.

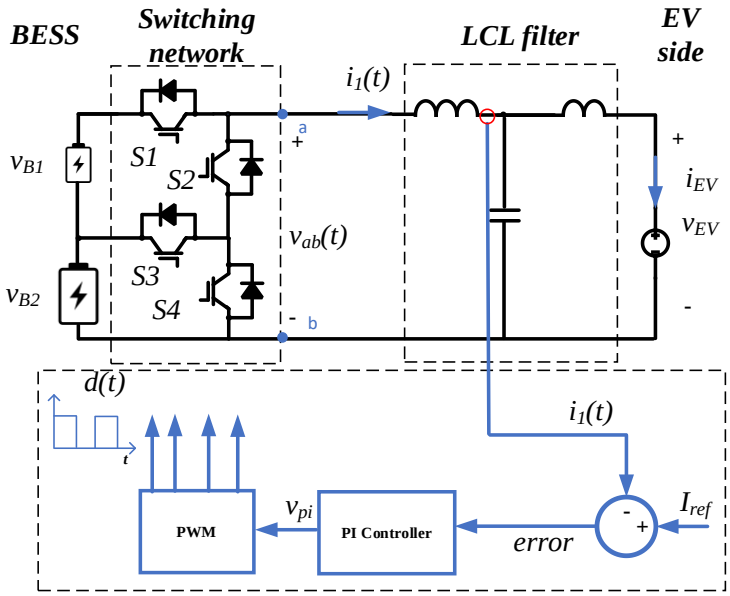


Figure 4. 1: Feedback control system for the RDC converter.

As shown in Fig. 4.1, the control system consists of the power stage of the RDC converter and a current feedback control loop. The power stage is divided into four parts: input BESS, the switching network, an LCL filter, and the EV battery. For the control loop, the converter control input (duty cycle *d(t)*) is fed into the switching network, so that the converter voltage $v_{ab}(t)$ can be regulated. Through the LCL filter, the output current $i_1(t)$ can be regulated by the converter voltage $v_{ab}(t)$. Thus, output current $i_1(t)$ can be regulated by the duty cycle *d(t).*

By the feedback control loop, the output current $i_1(t)$ is compared to the reference current I_{ref} (constant = 50A). Error is then calculated and fed into the controller. The controller is to update the control signal till the error is nearly zero.

The output current $i_1(t)$ should be accurately regulated and be insensitive to the changes in the input voltage (v_{B1} *and* v_{B2}) and output voltage v_{EV}. In addition, the feedback control system should be stable and meet specifications, such as limited transient overshoot and zero steady-state error. Thus, the controller must be well-designed to compensate for the undesired behavior in the control loop. To design a controller, a dynamic model of the RDC converter control loop is needed, also known as a small signal model. In this section, the small signal model of the RDC converter is first analyzed under two different modes. Then a Proportion and Integration (PI) controller is designed to improve the control performances.

4.1 Dynamic Model of the RDC Converter

Small signal approximation [34] is a useful and widely adopted method to derive a linear model of a power converter, in order to control the power converter by using a simple and linear PI controller. The output voltage ripple (0.4V) is quite small compared to the output voltage DC value (400V), therefore, the ripple (0.1%) can be neglected. An underlying small AC variation of the output voltage $\hat{v}$ is considered [35].

By the small signal approximation, for the duty cycle d(t), it can be modeled as a DC value D plus a small AC variation $\hat{d}$, as shown in equation (4.1).

$$d(t) = D + \hat{d} \tag{4.1}$$

, where D is the DC value, $\hat{d} \ll D$. Similarly, the small signal approximation is applied to all the other variables in the RDC converter in Fig. 4.1. Small signal approximation can easily linearize the RDC converter. This is illustrated as follows.

4.1.1 PWM Model

The PWM signal $d(t)$ is generated by comparing the control signal $v_c(t)$ with the triangular carrier waveform $v_{tri}(t)$[36], as shown in Fig.4.2. When $v_{pi}(t) > v_{tri}(t)$, $d(t) = 1$, as shown in period B. When $v_{pi}(t) < v_{tri}(t)$, $d(t)=0$, as shown in period A.

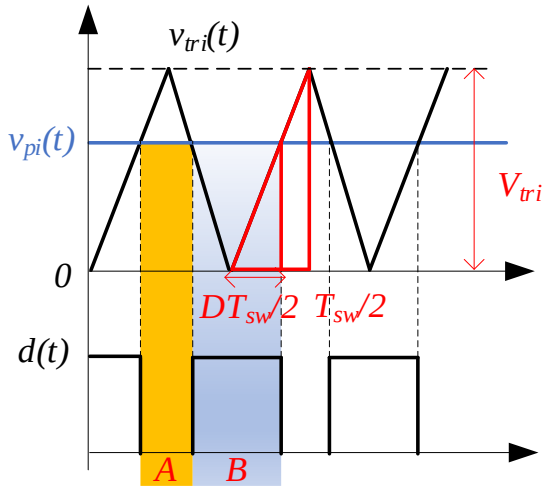


Figure 4. 2: PWM signal generated by comparison between the triangular carrier and control signal.

From Fig.4.2, according to the triangular similarity theorem, the duty cycle $d(t)$ can be derived:

$$d(t) = \frac{\frac{dT_s}{2}}{\frac{T_s}{2}} = \frac{v_{pi}(t)}{V_{tri}} \tag{4.2}$$

, where V_{tri} is the peak value of the triangular carrier waveform. Substitute equation (4.1) into (4.2), we get,

$$d(t) = D + \hat{d} = \frac{V_{pi}}{V_{tri}} + \frac{\hat{v}_{pi}}{V_{tri}} \tag{4.3}$$

, where D is the DC value (quiescent value), $\hat{d}$ is the small signal value for the duty cycle. The dynamic model of the power converter is based on the small signal value. The relationship between $\hat{d}$ and $\hat{v}_{pi}$ can be written as

$$\hat{d} = \frac{\hat{v}_{pi}}{V_{tri}} \tag{4.4}$$

Applying the Laplace transformation to the above time-based equation, we get the associated transfer function from $\hat{v}_{pi}(s)$ to $\hat{d}(s)$, as shown in equation (4.5).

$$G_{pwm}(s) = \frac{\hat{d}(s)}{\hat{v}_{pi}(s)} = \frac{1}{V_{tri}} \tag{4.5}$$

4.1.2 Model of LCL Filter

The rest of the power plant is modeled as an LCL filter plus a voltage source v_{EV}(t) (EV battery), as shown in Fig.4.3. The EV battery can be modeled as a voltage source v_{EV}(t) [37].

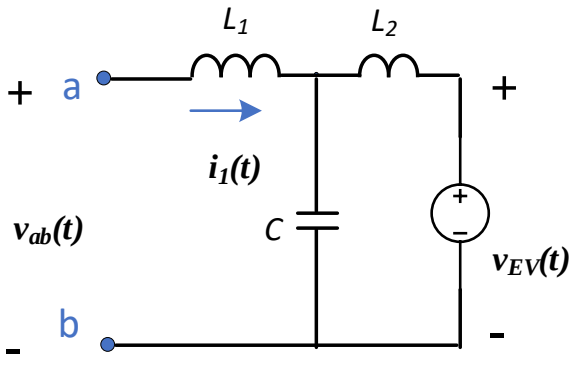


Figure 4. 3: Circuit model of the LCL filter and EV battery

Applying AC circuit theory to the LCL filter network, we can easily get the relationship between input voltage $v_{ab}(s)$ and output current $i_1(s)$.

$$\frac{i_1(s)}{v_{ab}(s) - v_{EV}(s)} = \frac{1}{Z_{L1} + Z_{L2}//Z_C} \tag{4.6}$$

Where, Z_C, Z_{L1}, and Z_{L2} are the impedances of C, L_1, and L_2 respectively. According to superposition theory, the dynamic model of the output voltage $v_{EV}(s)$ is set to be zero, when considering the transfer function from $v_{ab}(s)$ to $i_1(s)$. Therefore, the transfer function from $v_{ab}(s)$ to $i_1(s)$ can be derived as follows.

$$G_{iv}(s) = \frac{i_1(s)}{v_{ab}(s)} = \frac{s^2 L_2 C_2 + 1}{L_1 L_2 C s^3 + (L_1 + L_2)s} \tag{4.7}$$

4.1.3 Model of Switching Network

Under mode 1, as shown in Fig.2.9, the S1 and S2 are controlled by PWM to regulate output. Under mode 2, as shown in Fig.2.10, the S3 and S4 are now regulating the output. The feedback control loop has the same structure: two PWM-modulated switches, an LCL filter, a feedback current sensor, and a controller. In this subsection, the small signal model of the switching network under two modes will be analyzed and the corresponding transfer functions from duty cycle $d(s)$ to $v_{ab}(s)$ will be derived.

To modulate the four switches (S1-S4), the PD-PWM is applied, as shown in Fig. 4.4 (b). Fig.4.4 (b) illustrates the two stacked triangular carrier waveforms and control signal v_{pi}. Comparing the triangular carrier with the control signal v_{pi}, the PWM control signals for four switches are generated.

- For S1 and S2: the control signal v_{pi} is compared to the upper triangular carrier waveform.
- For S3 and S4: the control signal v_{pi} is compared to the lower triangular carrier waveform.

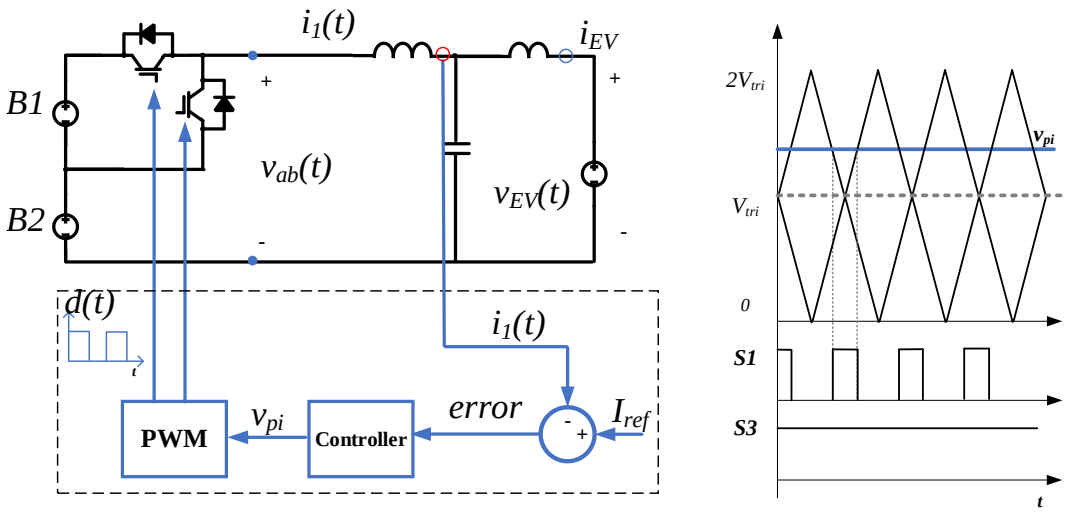
Under mode 1, the control signal v_{pi} is always higher than V_{tri}, as shown in Fig.4.4 (b). Switch S4 is constantly off and S3 is constantly on. The duty cycle of S1 is determined by the level of the control signal v_{pi}, while the PWM signal for S2 is complementary of S1.

Under mode 2, the control signal v_{pi} is always lower than V_{tri}, as shown in Fig.4.4 (b). Switch S1 is constantly off and S2 is constantly on. The duty cycle of S3 is determined by the level of the control signal v_{pi}, while the PWM signal for S4 is complementary of S3.

In this way, a single control signal v_{pi} can generate four PWM signals for S1-S4 to regulate the RDC converter under two modes.

1) Mode 1

Under mode 1, the switching network will be reconfigured as shown in Fig. 4.4 (a). In this configuration, both B1 and B2 are supplying the converter to regulate the outputs. The working principle of this configuration is the same as the RDC converter using buck topology, which has been illustrated in Section 2, as shown in Fig. 2.2.



(a) Current feedback control system (b) Four PWM signals

Figure 4. 4: PWM signal generated by comparison between triangular carrier and control signal under mode 1.

The output voltage of the switching network $v_{ab}(t)$ is a rectangular voltage (v_{B1} regulated by the duty cycle) plus v_{B2}. Applying moving average [38] to $v_{ab}(t)$, $\langle v_{ab}(t)\rangle_{T_{sw}}$ is derived as shown in equation (4.8).

$$v_{ab} = \langle v_{ab}(t)\rangle_{Ts} = \frac{d \times v_{B1} \times T_{sw}}{T_{sw}} + v_{B2} = d \times v_{B1} + v_{B2} \tag{4.8}$$

This moving average value can then be simplified as a DC value plus a small signal value. Equation (4.8) can be re-written as

$$\begin{gathered} v_{ab} = V_{ab} + \hat{v}_{ab} = \left(D + \hat{d}\right) \times (V_{B1} + \hat{v}_{B1}) + V_{B2} + \hat{v}_{B2} \\ V_{ab} = D \times V_{B1} + V_{B2} \\ \hat{v}_{ab} = V_{B1} \times \hat{d} + \hat{v}_{B2} + D \times \hat{v}_{B1} \end{gathered} \tag{4.9}$$

Where V_{ab}, V_{B1}, $V_{B2,}$ *and* $D$are the DC values of $v_{ab}(t)$, $v_{B1}(t)$, $v_{B2}(t)$ *and* $d(t)$ respectively [39]. $\hat{v}_{ab}$,$\hat{v}_{B1}$, $\hat{v}_{B2}$ and $\hat{d}$ are the corresponding small signal values of those variables. Equation (4.9) illustrates the time-based relationship between inputs ($v_{B1}(t)$, $v_{B2}(t)$, $d(t)$) and output voltage $v_{ab}(t)$ of the switching network under mode 1.

Applying the Laplace transformation to equation (4.9), the transfer function of the switching network is derived:

$$\hat{v}_{ab}(s) = V_{B1}\hat{d}(s) + \hat{v}_{B2}(s) + D\hat{v}_{B1}(s) \tag{4.10}$$

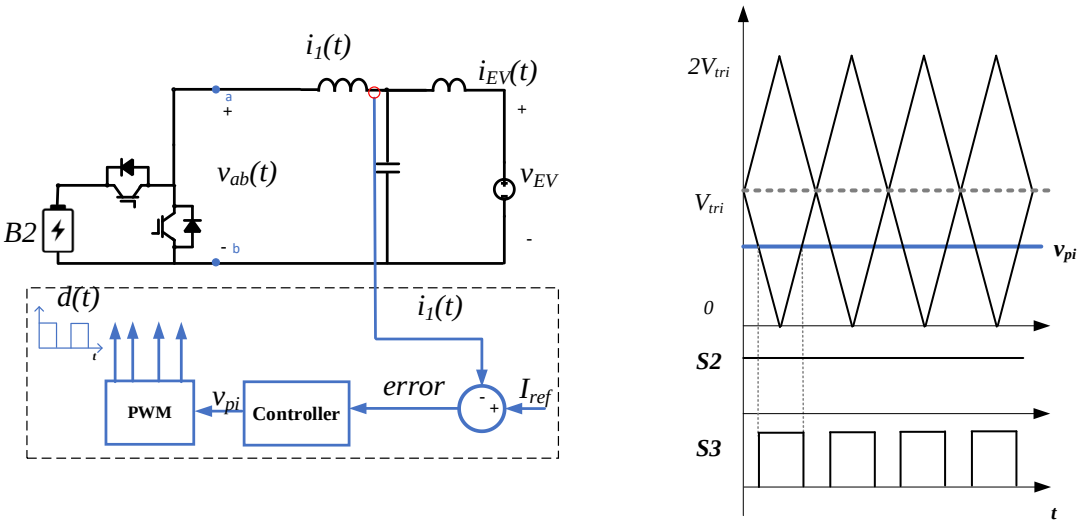
where $\hat{d}(s)$ is the duty cycle control signal for the switching network. $\hat{v}_{B2}(s)$ and $\hat{v}_{B1}(s)$ represent the independent disturbances from B1 and B2.

According to superposition theory, the independent disturbances are $\hat{v}_{B2}(s)$ and $\hat{v}_{B1}(s)$ set to zero [40], when deriving the transfer function from $\hat{d}(s)$ to $\hat{v}_{ab}(s)$.

$$G_{vd1}(s) = \frac{\hat{v}_{ab}(s)}{\hat{d}(s)} = V_{B1} \tag{4.11}$$

2) Mode 2

As illustrated in Section 2.3, under mode 2, the switching network will be configured as shown in Fig. 4.5 (a). In this configuration, B1 will be cut from the main circuit. B2 is supplying the converter to regulate the outputs. This configuration is the same as the buck converter, as shown in Fig. 2.3. Therefore, the working principle of the RDC converter under this condition is basically the same as a buck converter. Fig.4.5 (b) illustrates the two stacked triangular carrier waveforms and the control signal v_{pi}. The duty cycle of S3 is determined by the level of the control signal v_{pi}, while the PWM signal for S4 is complementary to S3.



(a) Current feedback control system (b) Four PWM signals

Figure 4. 5: Control system and PWM signals of the RDC converter under mode 2.

According to the buck converter principle in Section 2.1, the output voltage of the switching network $v_{ab}(t)$ shows a rectangular waveform. According to the small signal approximation, $v_{ab}(t)$ is approximated by its moving average value $\langle v_{ab}(t)\rangle_{Ts}$, as written in equation (4.12).

$$v_{ab} = \langle v_{ab}(t)\rangle_{Ts} = \frac{d \times v_{B2} \times T_{sw}}{T_{sw}} = d \times v_{B2} \tag{4.12}$$

Similarly to the duty cycle and control signal, this moving average value can then be simplified as a DC value plus a small signal value. Equation (4.12) can be expanded as

$$\begin{gathered} v_{ab} = V_{ab} + \hat{v}_{ab} = \left(D + \hat{d}\right)(V_{B2} + \hat{v}_{B2}) \\ V_{ab} = DV_{B2} \\ \hat{v}_{ab} = V_{B2}\hat{d} + D\hat{v}_{B2} \end{gathered} \tag{4.13}$$

, where V_{ab}, V_{B2} and D are the DC value of $v_{ab}(t)$, $v_{B2}(t)$ and $d(t)$ respectively. $\hat{v}_{ab}, \hat{v}_{B2}$ *and* $\hat{d}$ are the corresponding small signal values of those variables. Equation (4.13) illustrates the time-based relationship between inputs ($v_{B2}(t)$, $d(t)$) and output voltage $v_{ab}(t)$ of the switching network.

To get the frequency-domain relationship, Laplace transformation is applied to the above small signal equation. We get the transfer function of the switching network as follows.

$$\hat{v}_{ab}(s) = V_{B2}\hat{d}(s) + D\hat{v}_{B2}(s) \tag{4.14}$$

, where $\hat{d}(s)$ is the duty cycle control signal for the switching network. $\hat{v}_{B2}(s)$ represents the independent disturbances from B2 to the network output voltage $\hat{v}_{ab}(s)$. V_{B2} *and* D are the

steady-state DC values of the RDC converter [39], which are considered constant when analyzing the dynamics. According to superposition theory, the trafer function from $\hat{d}(s)$ to $\hat{v}_{ab}(s)$ can be derived considering $\hat{v}_{B2}(s)$=0, as shown in equation (4.15).

$$G_{vd2}(s) = \frac{\hat{v}_{ab}(s)}{\hat{d}(s)} = V_{B2} \tag{4.15}$$

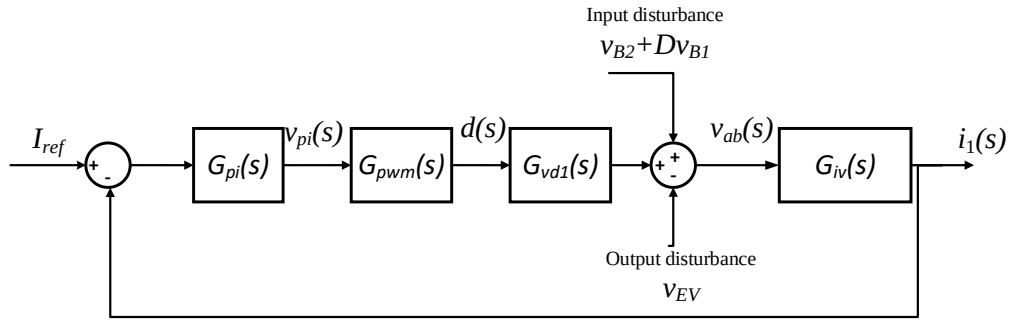
All the disturbances will be considered and illustrated in the graphical control diagram in Section 4.2.

4.2 Converter-side Current Control Loop

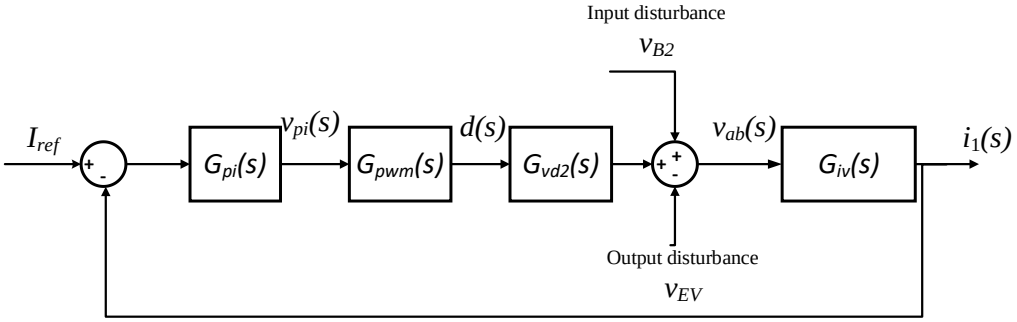
In Section 4.1, the transfer functions of the different parts in the control loop have been derived under two operation modes. This section will first analyze the open loop gains of the control system under two modes. Then, a single PI controller was designed to stabilize the system under both modes, and its design procedure was introduced.

4.2.1 Open Loop Gain

According to the transfer functions derived in Section 4.1, we can derive the graphical control diagrams of the closed control loops for mode 1 and mode 2, as shown in Fig.4.6 (a) and (b) respectively. The diagram incorporates the control-to-output gain, feedback closed loop, and independent input disturbances and output disturbances [38]. The major differences between the two diagrams are illustrated as follows.



(a) Current control diagram of RDC converter under Mode 1



(b) Current control diagram of RDC converter under Mode 2

Figure 4. 6: Feedback control loops for regulation of the output current under two modes.

1) Independent external disturbances

For mode 1, B1 and B2 both provide power. They will bring independent disturbances (v_{B1} and v_{B2}) to the control loop. For mode 2, the input disturbances only come from B2 (disturbance: v_{B2}), since B2 is the only one supplying the power. The independent disturbances coming from the output side for the two modes are the same.

2) Open loop gain

Apart from the independent disturbances from input and output, the other difference between the two modes is the open loop gain variation. The dynamic model in the above diagram is a linear model. The superposition theorem can be applied to this control diagram. The open loop transfer function of the power plant without input and output disturbances can be derived by setting disturbances to zero.

Multiply equations (4.5), (4.7), and (4.11), and the open loop gain $G_{op1}(s)$ under mode 1 is derived, as shown in equation (4.16).

$$G_{op1}(s) = \frac{V_{B1}}{V_{tri}} \frac{(s^2 L_2 C + 1)e^{-1.5sT_s}}{s^3 L_1 L_2 C + s(L_1 + L_2)} \tag{4.16}$$

Multiply equations (4.5), (4.7), and (4.15), and the open loop gain $G_{op2}(s)$ under mode 2 is:

$$G_{op2}(s) = \frac{V_{B2}}{V_{tri}} \frac{(s^2 L_2 C + 1)e^{-1.5sT_s}}{s^3 L_1 L_2 C + s(L_1 + L_2)} \tag{4.17}$$

Since V_{B2} and V_{B1} are different, the open loop gains under two modes are not the same. The frequency-domain analysis is often used to illustrate the dynamics of the control system. Therefore, bode plots of the two open loop gains are drawn, as shown in Fig. 4.7.

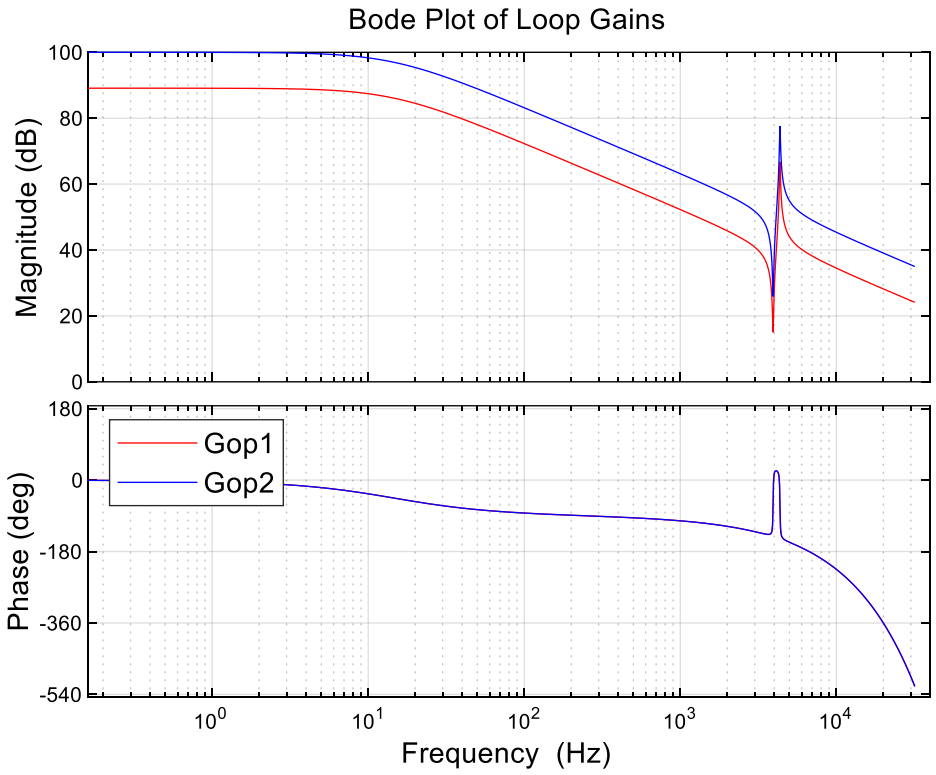


Figure 4. 7: Bode plots of the open loop gain under two different modes.

The blue curve represents the bode plot of the open loop gain under mode 1, which is $G_{op1}(s)$. The red curve illustrates the bode diagram of the open loop gain $G_{op2}(s)$ for mode 2. From the magnitude plots, we can see that the blue curve is always higher than the red curve. While the phase plots of the two open loop gains are the same. For an LCL filter-based converter, stability is often not easily achieved since it has a very high resonant peak. The resonance frequency of the LCL filter is expressed as shown in equation (4.18).

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_1 L_2 C}{L_1 + L_2}}} = 4.35\ kHz < \frac{f_s}{6} \tag{4.18}$$

, where f_s is the sampling frequency of the control system. According to LCL filter-based control theory, the converter-side current control for LCL filter is a robust stable design without adding extra active damping. (when $f_s/6 > f_r$). Therefore, the converter-side current control is implemented to control the charging current.

A PI controller should be carefully designed to guarantee stability. In this case, we have two different open-loop gains, and we need to design a single PI controller to control two modes stably. According to Nyquist criteria in this case, the closed-loop system is stable if and only if the number of negative crossings is zero. That means the magnitude at the frequency of crossing -180 degrees should be less than zero. As shown in Fig 4.7, the magnitude of the blue curve (mode 1) is always higher than the red curve (mode 2). Therefore, if a PI controller can stably control the converter under mode 1, the control system will also be stable under mode 2. Section 4.2.2 introduces the design procedure of the PI controller focusing on control system open loop gain under mode 1.

4.2.2 PI Controller

A PI controller is the most used control method in the industry, due to its simplicity and robustness. The transfer function for the PI controller is:

$$G_{pi}(s) = k_p + \frac{k_i}{s} \tag{4.19}$$

, where k_p represents the proportion and k_i represents integration.

As mentioned above, a PI controller should be designed to tune the bode plot, so that control performances of the feedback closed-loop control system can be improved. There are mainly three performance aspects mostly concerned. Each of them relates to the characteristics of the bode plot. These aspects are summarized as follows.

- Small steady-state error: High low-frequency (DC) loop gain.
- Fast response: High bandwidth (0 dB crossover frequency f_c).
- Small overshot: Large Phase Margin and Gain Margin.

Usually, trade-offs need to be made when designing the parameters of a PI controller. For instance, when a PI control system shows a high bandwidth, it will introduce a larger overshoot.

In this case, a step-by-step PI parameters design procedure [41] is first introduced to guarantee stability as well as high bandwidth, as follows.

1) Determine cross-over frequency $f_c = f_{sw}/10$ =4 kHz.
2) Calculate $k_p = 1/G_{op2}(f_c) = 0.0018$
3) Determine $f_L = 100Hz$ (reduce the phase delay at f_c)
4) Calculate the integral parameter $k_i = 2\pi k_p f_L = 1.131$

Initial PI controller parameters are designed according to the procedure introduced above. The PI control parameters can be tuned and adjusted to provide sufficient control under other extreme working conditions.

Multiply equations (4.17) and (4.19), we get the open loop transfer function with the PI controller under mode 2 as follows.

$$T_2(s) = \frac{V_{B2}}{V_{tri}} \frac{(s^2 L_3 C_2 + 1)e^{-1.5sT_s}}{L_1 L_2 C s^3 + (L_1 + L_2)s} \times \left(k_p + \frac{k_i}{s}\right) \tag{4.20}$$

Finally, the bode plot of the loop gain with the designed PI controller is shown in Fig. 4.8.

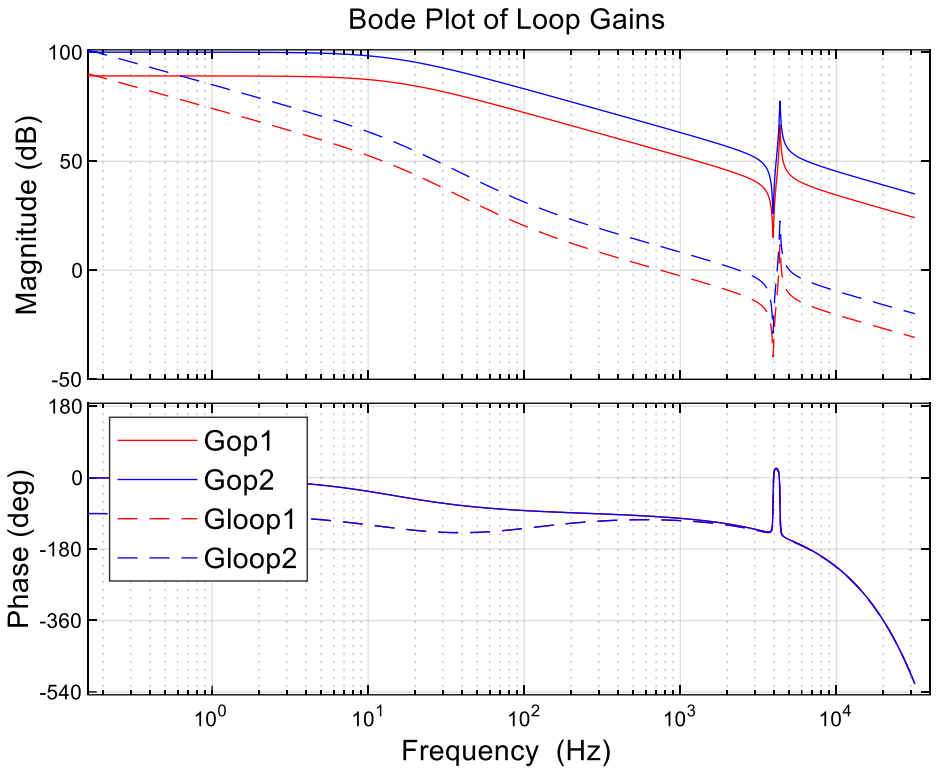


Figure 4. 8: Loop gain of the control system with the designed PI controller

The dashed red and blue curve represents the loop gain with the designed PI controller under mode 2 and mode 1 respectively. From the bode plot, the steady-state and dynamic performances of the control system are summarized as follows:

1) DC loop gain: High (>100 dB)
2) Bandwidth: Around 2 kHz
3) Phase and Magnitude Margin: 5dB & 22 degree

4.3 Stability Analysis including Input LC filters.

The closed-loop control of the RDC converter with an LCL filter has been designed in Section 4.2. The two input filters from the input side have been designed in Section 3.4.2. This subsection first analyzes the small signal model including the input filters of the RDC converter. Finally, the stability of the whole system is then analyzed according to the impedance-based analysis.

If the RDC converter is stable under mode 1, it will also be stable under mode 2. Therefore, this subsection focuses on the stability analysis under mode 1.

LC filters are to suppress the ripples/noises from the converter to the batteries/power supplies. However, sometimes, the designed LC filter might affect the stability of the control loop [42]. This subsection is to analyze the control stability of the RDC converter with the designed LC filters. To analyze the stability of a multi-port network, the impedance-based analysis method [43] is usually applied. A converter and its power supply can be modeled as an impedance network, as shown in Fig.4.9. The power supply or battery with an input filter is most commonly modeled as a voltage source V_s connected in series with output impedance (Z_s), according to Thevenin equivalent circuit law. [44] Z_{in} represents the input impedance of the feedback control system.

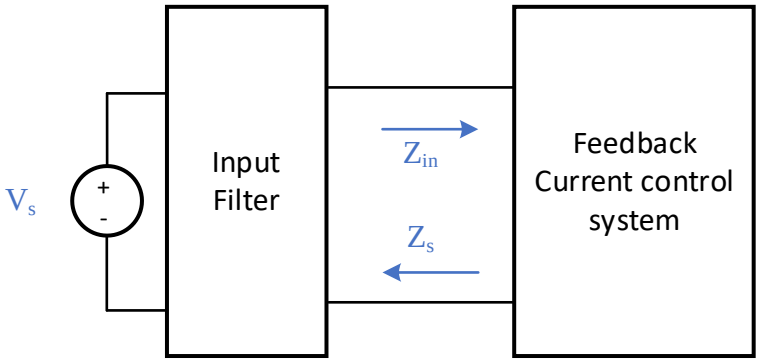


Figure 4. 9: Impedance model of the feedback control system with input filters

According to [44], if the output impedance Z_s of the LC filter over the input impedance of the RDC converter (Z_{in}) satisfies the Nyquist Criterion, the system will be stable. A more practical method is introduced. To avoid instability and oscillation, the input impedance Z_{in} of the converter should be higher than the output impedance Z_s of the LC filter [42].

For the RDC converter, the output impedance Z_s of the LC filter can be easily derived. In Section 4.2, the control diagram and loop gain of the RDC converter have been discussed, However, its input impedance has not been discussed and derived. In this subsection, to calculate the input impedance of the RDC converter, the canonical small signal converter model including input LC filters has been built, as shown in Fig.4.17. In the canonical equivalent circuit model, we can see there are four different voltage sources $\hat{v}_{B1}(t)$, $\hat{v}_{B2}(t)$, $V_{B1}\hat{d}(t)$, $\hat{v}_{EV}(t)$ and a current source $I_1\hat{d}(t)$. The passive components in the equivalent circuit are the designed input filters as well as the designed LCL filter. To apply the impedance-based analysis method for the stability of the RDC converter, the output impedance of the LC filter is modeled as Z_s, and the input impedance of the RDC converter Z_{in} must be calculated.

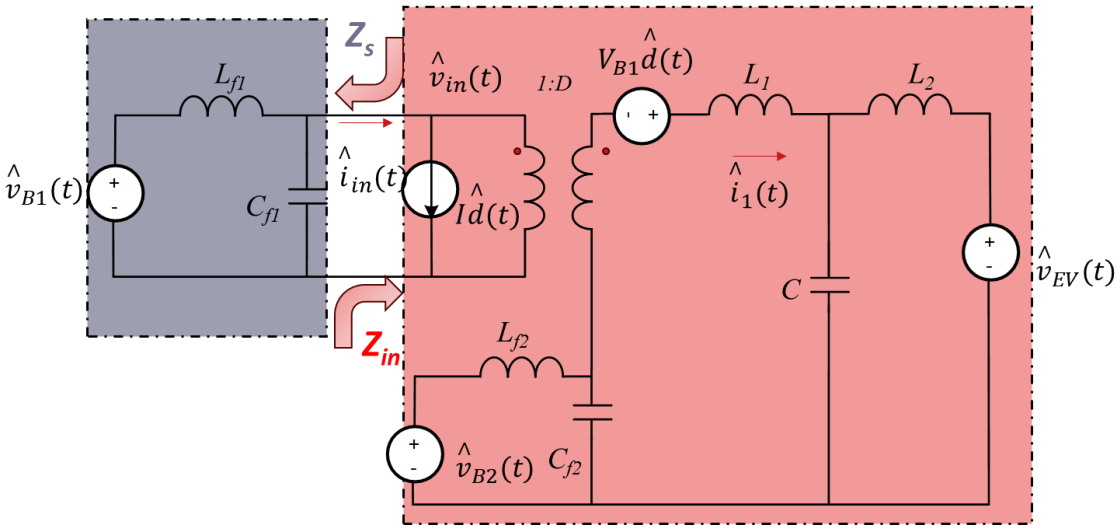


Figure 4. 10: Canonical small signal model [38] *of the RDC converter including input LC filters[33]*

As discussed in Section 4.1, a transfer function is mostly used to describe how variations or disturbances of a variable lead to variations in another variable.

The transfer function $G_{iv_{EV}}(s)$ is calculated by setting other variations to zero [38], and then solving for the transfer function from $\hat{v}_{EV}(s)$ to $\hat{i}_1(s)$:

$$G_{iv_{EV}}(s) = \frac{\hat{i}_1(s)}{\hat{v}_{EV}(s)}\Big|_{\hat{v}_{B1}(s),\hat{v}_{B2}(t),\hat{d}(t)=0} \tag{4.21}$$

From this definition, we can simplify the equivalent circuit model (Fig.4.10) to Fig.4.11, as below.

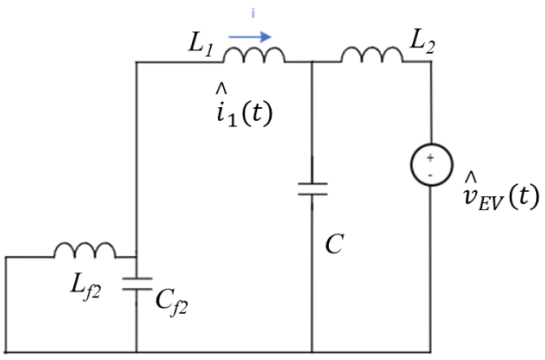


Figure 4. 11: Equivalent circuit model calculating transfer function from $\hat{v}_{EV}(s)$ to $\hat{i}(s)$.

The transfer function can be easily derived from Fig.4.11, as equation (4.22).

$$G_{iv_{EV}}(s) = \frac{\hat{i}_1(s)}{\hat{v}_{EV}(s)} = -\frac{(Z_{L1}+Z_{f2})//Z_C}{(Z_{L1}+Z_{f2})//Z_C + Z_{L2}}\frac{1}{Z_{L1}+Z_{f2}} \tag{4.22}$$

, where Z_{L1}, Z_{L2}, Z_C, Z_{f2} represents the impedance of L_1, L_2, C and the input filter at B2 respectively.

The equivalent circuit model calculating the input impedance of the RDC converter can be derived, as shown in Fig.4.12.

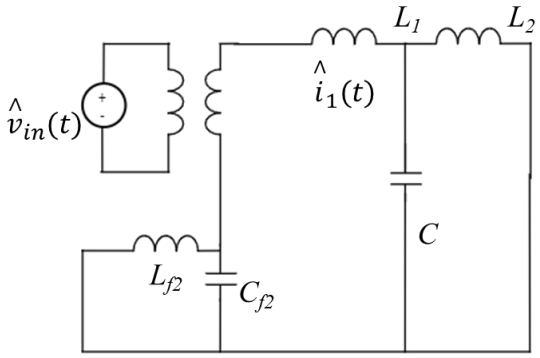


Figure 4. 12: Equivalent circuit model calculating input impedance

The open loop input impedance of the RDC converter seen from B1 can be derived by the definition shown in equation (4.23).

$$Z_{in\_op}(s) = \frac{\hat{v}_{in}(s)}{\hat{i}_{in}(s)}\Big|_{\hat{v}_{B1}(s),\,\hat{v}_{B2}(s),\,\hat{d}(s),\,\hat{v}_{EV}(s)\,=\,0} \tag{4.23}$$

From the definition, we can derive the input impedance:

$$Z_{in\_op}(s) = \frac{1}{D^2}\left[Z_{L1} + Z_{L2}//Z_C + Z_{L_{f2}}//Z_{C_{f2}}\right] \tag{4.24}$$

, where $Z_{L_{f2}}$, $Z_{C_{f2}}$ represents the impedance of L_{f2} and C_{f2} of the input filter at B2 respectively. Similarly, other transfer functions can be derived based on the superposition theory, the other transfer functions are summarized in equations (4.25), (4.26), and (4.27).

$$G_{iv_{in}}(s) = \frac{\hat{i}_1(s)}{\hat{v}_{in}(s)} = D\,\frac{1}{Z_{L1} + Z_{L2}//Z_C + Z_{f2}} \tag{4.25}$$

$$G_{iv_{B2}}(s) = \frac{\hat{i}_1(s)}{\hat{v}_{B2}(s)} = \frac{1}{Z_{L1} + Z_{L2} + Z_{f2}}\,\frac{Z_{C_{f2}}}{Z_{L_{f2}} + Z_{C_{f2}}} \tag{4.26}$$

$$G_{id}(s) = \frac{\hat{i}_1(s)}{\hat{d}(s)} = V_{B1}\,\frac{1}{Z_{L1} + Z_{L2}//Z_C + Z_{f2}} \tag{4.27}$$

Based on the transfer functions derived above, the complete mathematical control diagram of the RDC converter can be derived, as shown in Fig.4.20. The feedback control loop

remains the same as the loop gain shown in Fig. 4. 6(a). The other variations or disturbances $\hat{v}_{EV}(s)$, $\hat{v}_{in}(s)$, $\hat{v}_{B2}(s)$ are also modelled by the transfer functions.

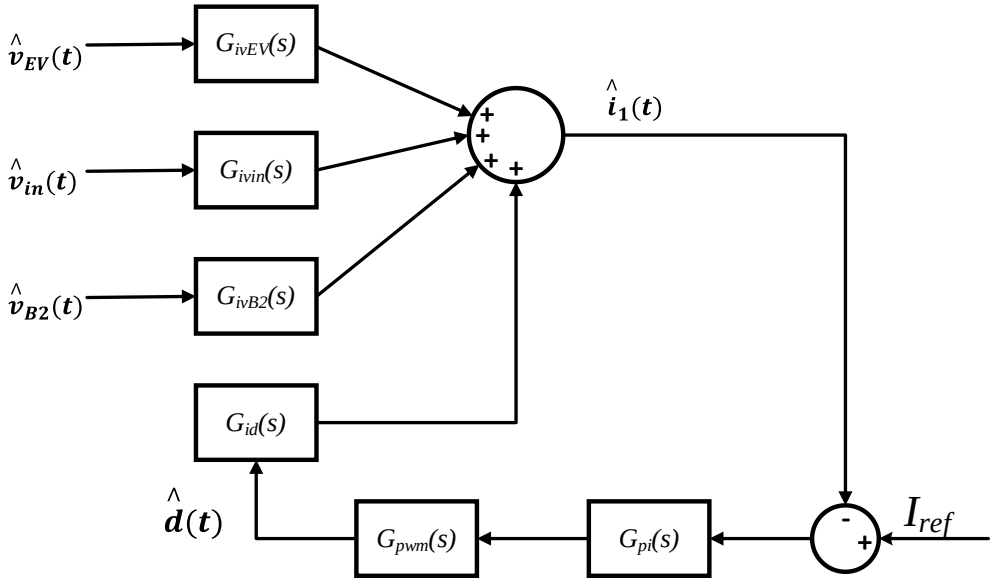


Figure 4. 13: The complete closed-loop control diagram of the RDC converter with input LC filters

The motivation for deriving the complete control diagram of the RDC converter is to derive the input impedance of the RDC converter under the closed-loop control condition. With the transfer functions and completer closed-loop control diagram, we can derive the closed-loop input impedance as the definition below:

$$Z_{in\_}cl(s) = \frac{\hat{v}_{in}(s)}{\hat{i}_{in}(s)}\Big|\hat{v}_{B2}(s), \hat{v}_{EV}(s) = 0 \tag{4.28}$$

From Fig.4.10, by the KCL law, we can easily derive the input current $\hat{i}_{in}(s)$:

$$\hat{i}_{in}(s) = I\hat{d}(s) + D\hat{i}_{1(s)} \tag{4.29}$$

, where *I* is the DC value of the output current and *D* is the DC value of the duty cycle at steady state. From Fig.4.13, we can derive the transfer function from $\hat{i}_{1(s)}$ to $\hat{d}(s)$:

$$\hat{d}(s) = -\hat{i}_{1(s)} \times G_c(s) \times G_{pwm}(s) \tag{4.30}$$

From Fig.4.13, we can calculate the output current $\hat{i}(s)$ in equation (4.31):

$$\hat{i}_{1(s)} = \hat{d}(s) \times G_{id}(s) + G_{ivin}(s) \times \hat{v}_{in}(s) \tag{4.31}$$

Combining equation (4.23), (4.28-4.30), we can calculate the closed-loop input impedance $Z_{in\_cl}(s)$ of the RDC converter as equation (4.32):

$$Z_{in\_cl}(s) = Z_{in\_op}(s) \times \frac{1 + T_1(s)}{1 - I \times G_{pi}(s) \times G_{pwm}(s)/D} \tag{4.32}$$

, where $T_1(s)$ is the loop gain under mode 1 calculated in equation (4.14).

The closed loop and open loop input impedance of the RDC converter have been derived. The bode plots of the impedances can be drawn based on the transfer functions derived above, as shown in Fig.4.14.

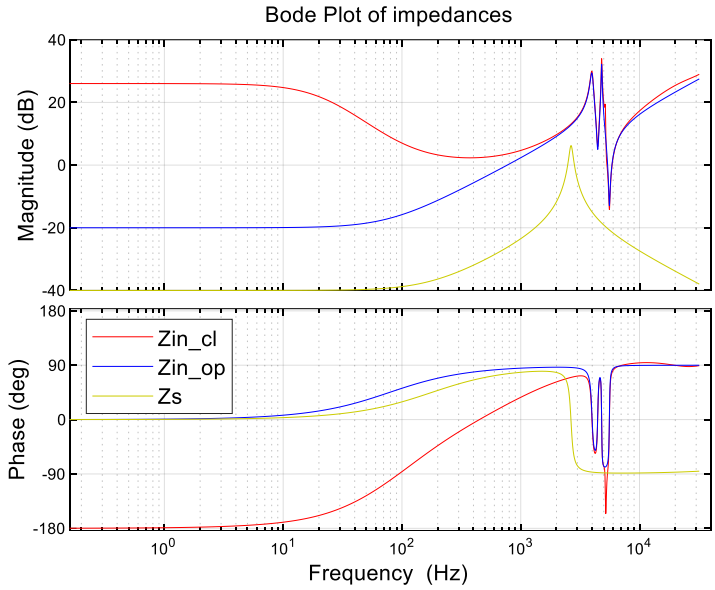


Figure 4. 14: Bode plots of the input impedances of the RDC converter and output impedance of the input LC filter

From Fig.4.14, both the open-loop input impedance Z_{in_op} and closed-loop input impedance Z_{in_cl} are higher than the output impedance Z_s of the input LC filter at B1. This means that the RDC converter will be stable under open-loop control and closed-loop control conditions, with the designed input LC filters.

4.4 DSP28379-based Digital Control Design

In Section 4.2, the current feedback closed loop with a PI controller has been designed, as shown in Fig.4.5 (a). In this section, the designed closed-loop feedback control will be implemented in the DSP28379 control card, as shown in Fig.4.15.

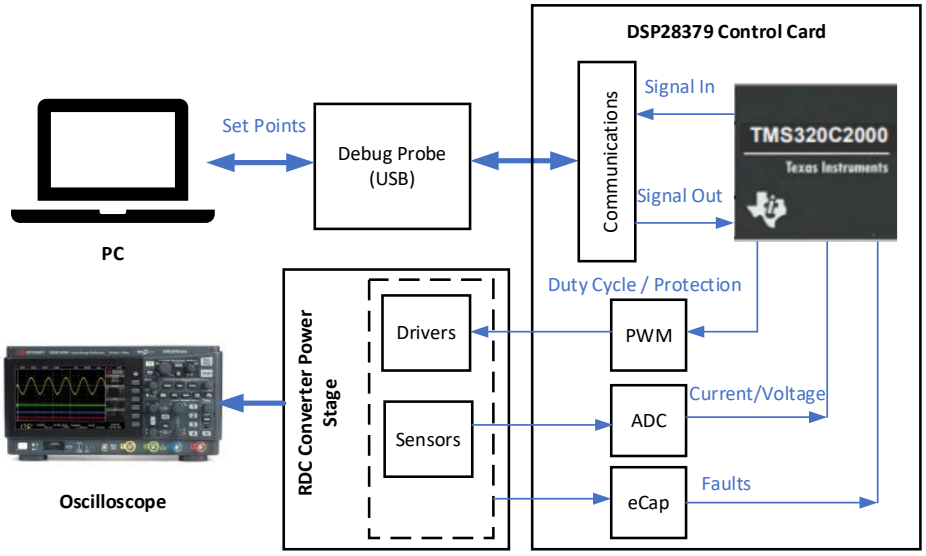


Figure 4. 15: Digital close loop control diagram using DSP28379 control card

The control card is connected to the PC by a debug probe. The digital control algorithm can be programmed and compiled on the PC and downloaded to the control card by the debug probe. The control card can operate online so that the PC can also receive signals from the control card and monitor the real-time calculations in the control card. The MCU inside the control card is the C2000 series from Texas Instruments. It will do all the real-time voltage / current sensing, faults monitoring, and calculations. Then the output of the calculation will adjust the duty cycle of the PWM module to control the turn on and off of the MOSFETs in the RDC converter.

In this RDC converter control, the output inductor current is sensed by the Hall sensor and fed into the ADC module, transforming the analog signal to the digital signal. The MCU will calculate the control output by the designed PI controller and send a control signal to the PWM module. The PWM module will receive the calculated control output and adjust the duty cycle for the switches.

The main function of the detailed digital control algorithm is illustrated in Fig.4.16.

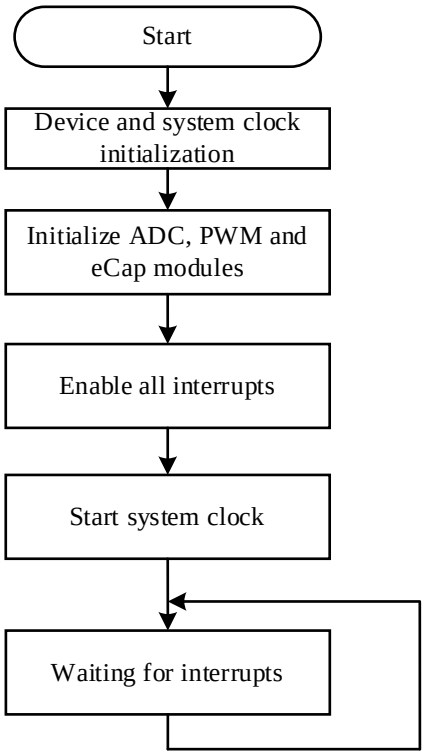


Figure 4. 16: The main function of the digital control algorithm implemented in the DSP28379 control card

The main function of the digital control algorithm is relatively simple. It starts with the initialization of the device (control card). The PWM, ADC, and eCap modules are initialized and set to be ready for functioning. The real-time calculation is always driven by the interrupts. When the interrupts are enabled, the MCU will start the system clock and be waiting for the interrupts from the ADC module or other external interrupts.

In this case, two major interrupts have been set. One is the ADC interrupt to provide the main function of the PI control loop. The other is the interrupt signal from the eCap module when a fault is detected by external circuits.

Fig.4.17 shows the detailed algorithm for ADC interrupt service.

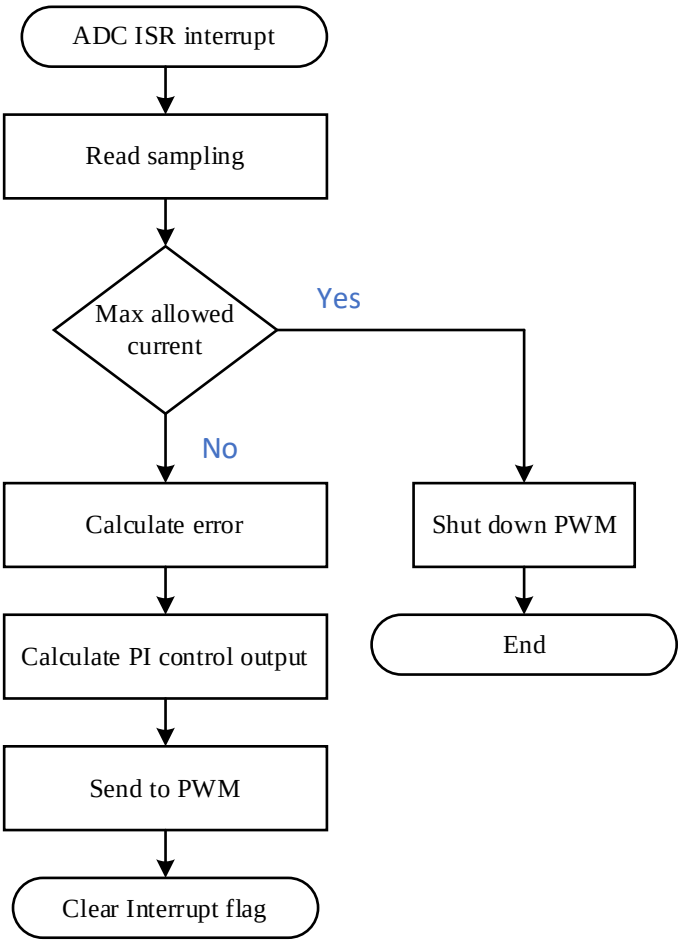


Figure 4. 17: ADC interrupt service of the implemented algorithm

ADC will start sampling and conversion every sampling period. At the end of each conversion period, the ADC module will introduce an interrupt to MCU. Then MCU will give the computing space to this service. It will first read the sampled value from the ADC modules. To provide over-current protection, the sampled value will first be compared with the maximum allowed current. If the sampled current is larger, the MCU will shut down all the PWM modules, so as to cut off the power from BESS to the EV. If not, the MCU will calculate the control error by subtraction of the reference value from the sampled value. Then, the control output is calculated and sent to the PWM modules. Finally, the interrupt flag register of the ADC module is cleared. The MCU will wait for the next ADC interrupt. In normal operation, this ADC interrupt service will run during every sampling period.

Some other necessary interrupts can also be enabled, such as fault signals detected by the eCap modules. When a fault signal is detected by an eCap module, an interrupt will be sent to MCU.

During the interrupts, the MCU will stop current works/calculations and change to the associated interrupt service. The interrupt service of the eCap module is described in Fig.4.18.

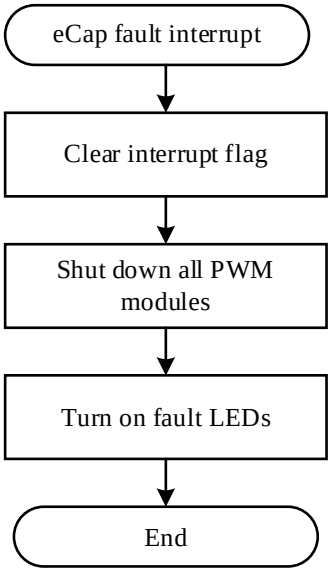


Figure 4. 18: Interrupt service of the eCap module to detect fault signals and provide protection for the RDC converter

The eCap unit is a module in the control card to capture the rising edge or falling edge from the external faults signal. For instance, when an over-current / voltage incident happens, the external sensing circuit will feed a fault signal (usually a rising edge or falling edge) to the eCap unit. When a rising edge or falling edge is detected, eCap module will request an interrupt service from the MCU. The MCU will stop its current working/calculation. In this case, it will shut down all the PWM modules, turn on fault LEDs, and end the program. So, the RDC converter is protected from over current or voltage, we can check the reason for the faults. When the faults are found and cleared, the program will be reinitialized.

4.5 Summary

In conclusion, the dynamic models of the RDC converter with converter-side current control have been built based on the small signal approximation. The associated open loop gains under two modes have been derived. Under two different modes, the control system presents different dynamic models. A single PI controller with delay was then designed to stabilize the control system under both modes. Later, the input LC filters were designed to suppress the ripples from the RDC converter to BESS (B1 and B2). The stability of the control system including input LC filters was analyzed. Finally, the designed PI control was implemented in the DSP28379 control card.

5 EXPERIMENTAL RESULTS

As discussed in Section 2.3, the RDC converter can achieve very high efficiency (about 99.4%), due to the benefits of partial power processing. Section 3 describes the hardware design process of a 20 kW RDC prototype. The RDC converter has been assembled and tested. This section will verify the efficiency and control performance by experiments.

First, the results of the efficiency of the RDC converter are verified. Later in this section, the results of the constant current closed-loop control are analyzed to verify the performance of the designed PI controller in Section 4. Finally, the results and analysis of the dynamic process are given under the step change of the reference current.

5.1 Laboratory Setup

This subsection shows the laboratory setup of the RDC converter. The fabricated main inductor L_1 was tested. With the designed inductor, the RDC prototype was built together with the associated testing environment.

5.1.2 Inductor Testing

High-power inductors are the key components in the RDC converter. As discussed in Section 3.4.1, two inductors (L_1 and L_2) are needed for the LCL filter in the RDC converter. Considering the required inductance of L_1 and L_2, L_2 is commercially available. It has been tested by the manufacturer. So L_2 was not tested in this project. However, the main inductor L_1 for the LCL filter is unique and not available on the market. The main inductor L_1 was designed and fabricated in the lab.

The designed inductor L_1 was tested using an LCR meter - Agilent 4263B, as shown in Fig 5.1. The LCR meter can measure the inductance and resistance of the inductor under test. As shown in the screen of the LCR meter in Fig.5.1, we can read the inductance and resistance. The results are shown in Table 5.1.

Figure 5. 1: The LCR meter testing the parameters of the inductor L1

From Table 5.1, the tested inductance coincided with the designed value (31.25 μH) quite well. The DC resistance of the inductor L_1 is about 2.75 mΩ. The AC resistance (@20 kHz) is around 11.7 mΩ (nearly three times the DC resistance). Due to the bandwidth limitations of the LCR meter, the LCR meter can only measure the AC resistance up to 20 kHz. Therefore, the AC resistance (@40 kHz) of the inductor L_1 was not tested due to the limitations of the LCR meter.

Table 5. 1: The designed inductor L1 and its testing values.

Parameters	Tested value
Inductance (μH)	29.7
R_{dc} / mΩ	2.75
R_{ac} / mΩ @20kHz	11.7

5.1.3 The RDC Prototype

After the main inductor L_1 had been fabricated, the RDC prototype was then assembled. Table 5.2 provides detailed information on the main components and specifications of the RDC converter.

Table 5. 2: Main components and specifications of the RDC converter

	Descriptions / Parameters	
Critical working conditions	• Switching frequency f_{sw}=40 kHz • Sampling frequency f_s=40 kHz • L_1 current ripple: 40% (peak-to-peak) • Output current ripple: 5% • Output Voltage ripple: 0.4V	
Output inductors	L_1: 31 μH B65982Q0400K097 /	L_2: 4.7 μH B82559B5472A027
DC Capacitor (Output)	2* B32718H8117K000 (110 uF)	
Input Capacitors	C_{f1} (400 μF) DCP4G064009JD4KSSD	C_{f2} (110 μF) B32718H8117K000
Semiconductors (Power switches)	S1 & S2: IRF300P226 (300V Si MOSFETs)	S3 & S4: C3M0015065K (650V SiC MOSFETs)
Cooling system	Heatsink (Fischer Elektronik):LA915024V	Thermal pad: GCSP-01710A10G
Control card	• Texas Instruments DSP28379 control card • Isolated XDS100v2 Debug Probe	

As shown in Table 5.2, the key components of the RDC converter are illustrated as follows.

1) The working conditions are based on the optimal operating point designed in Section 3. As described in Section 4.4, the RDC converter was controlled digitally. The digital control system needs to define the sampling frequency. It was set to be the same as the switching frequency in this project.
2) The output inductor L_1 was designed and fabricated. The inductor L_2 is bought.
3) The DC capacitor was selected based on the procedure illustrated in Section 3.5.2.
4) As discussed in Section 3.4.2, the input filters were not implemented. To stabilize the input bus voltage for the RDC converter, the input capacitors (C_{f1} and C_{f2}) are selected according to Fig.3.24, as shown in Table 3.2.
5) As mentioned in Section 3.5.1, the power switches are selected.
6) To dissipate heat from the power switches, a heatsink and a thermal pad are selected. The heatsink is to transfer the heat from the MOSFETs to the ambient. The thermal pad not only provides a heat transfer path but also isolates the MOSFETs from each other.
7) A DSP28379 control card from Texas Instrument is selected as the main control board to regulate the current of the RDC converter. The debug probe is to make the connection between the control card and the computer. So, the program can be downloaded to the control card.

With the above-designed main inductor L_1 and the selected components, the 20 kW RDC prototype has been built in the lab, as shown in Fig 5.2.

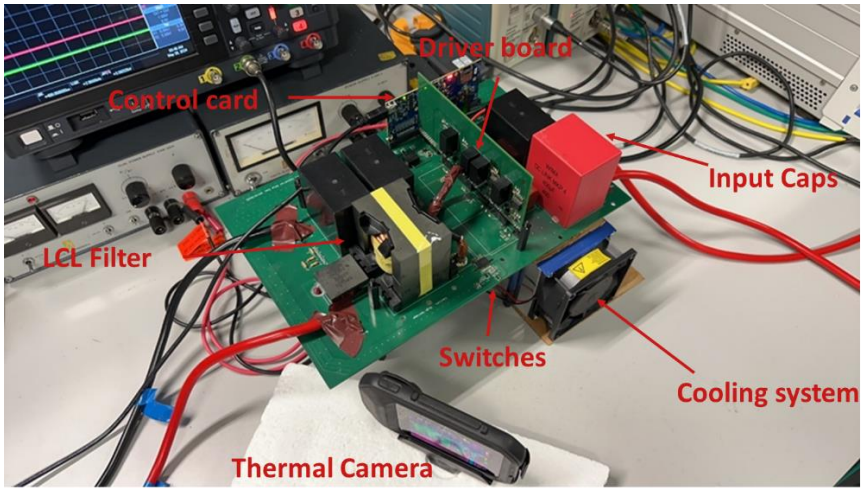


Figure 5. 2: The 20 kW RDC converter prototype. (The power stage consists of the LCL filter, the switches, and the input capacitors).

The 20 kW RDC prototype is composed of four major parts, as follows.

1) The main power stage: the input capacitors, the switching network (at the bottom side of the PCB board), and the output LCL filter.
2) Driver board: the driving circuits for MOSFETs, the isolated auxiliary power supplies for driving circuits, and MOSFETs over-current protection circuits.
3) Control card: The DSP28379 control card is selected to provide sufficient sensing and feedback control for the RDC converter.
4) Cooling system: The thermal pad and the heatsink are attached to the power switches at the bottom side. A thermal camera is pointed to the switches to monitor the temperature, to avoid overheating at extreme conditions.

5.1.4 Testing Environment

After the 20 kW RDC prototype has been built. The necessary testing instruments were set to provide accurate measurements and evaluate the performance of the RDC converter. Table 5.3 shows the equipment and testing instruments to test the RDC converter.

Table 5. 3: Instruments of testing the RDC converter.

	Descriptions / Parameters	
Power supplies/load	1) B1: SM120-50 (Delta Elektronika) 2) B2: SM500CP90 (Delta Elektronika) 3) EV: GE&EL+50 vAC/DC SiC (Cinergia)	
Probes	Current probe: TCP303 current probe+TCPA300 Amplifier (Tektronix)	Voltage probe: • Passive probe: Keysight N2140A • Differential Voltage probe: TA042
Digital oscilloscope	DSOX1204A (Keysight)	
Power analyzer	HIOKI PW6001. (Current probes: HIOKI CT 6843-05)	
Auxiliary power	Dual Power supply E018-0.6D	
Thermal meters	Camera: FLIR C3 Education kit	Thermal gun: 566 IR Thermometer

As summarized in Table 5.3, the key instruments are illustrated as follows.

1) Power supplies/load: There are three different power supplies/loads for the RDC converter. The Cinergia unit (20 kW) is to emulate the EV battery as the load for the RDC converter. For the input side of the RDC converter, the SM120-50 (up to 6kW) DC power source is to emulate the B1. B2 is emulated by SM500CP90 unit (up to 15 kW). The detailed configuration will be illustrated in Fig.5.8.
2) Power analyzer (HIOKI PW6001): The power analyzer is to measure the voltage and current of both the input and output sides, so as to calculate the power efficiency of the RDC converter. The accuracy of the power analyzer HIOKI PW6001 will be discussed later.
3) Oscilloscope and Probes: To measure the inductor (L_1 and L_2) current and voltage waveforms, current and voltage probes are needed. The measured signals from the probes will be sent to the oscilloscope. The oscilloscope will store the signals and display the waveforms.

With the necessary testing instruments, the testing environment of the RDC converter is settled, as shown in Fig. 5.3.

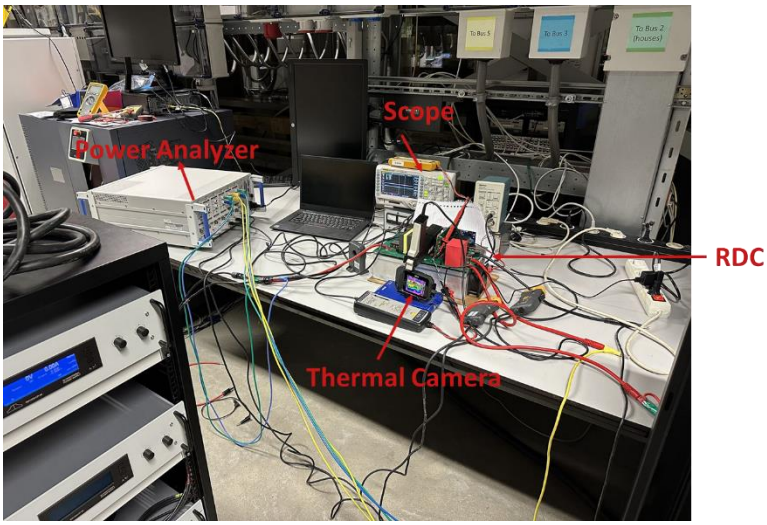


Figure 5. 3: Testing environment of the RDC converter

5.2 Efficiency Testing

The RDC converter and the associated testing instruments were built in the lab. The RDC converter was first tested under low power conditions, to make sure the RDC prototype operated properly first. Any defect or improper behavior inside the RDC prototype was detected and fixed. The results are summarized and discussed in Section 5.2.1. Then, the RDC converter was then tested up to 20 kW. The results of the efficiency of the RDC converter are analyzed in Section 5.2.2.

5.2.1 Initial Testing

As mentioned, before testing the efficiency of the RDC converter, the functionality of the RDC converter was first tested. Since the RDC converter under mode 2 rarely happens in normal operation, the efficiency was not tested in this project. The RDC converter was tested under mode 1 only, under which the RDC converter can achieve very high efficiency due to partial power processing. Fig.5.4 illustrates the measurement setup to test the key waveforms of the RDC converter. A thermal gun was used to measure the temperature of S1. (The temperature of S1 is the highest among the four switches, see Table 3.8). A voltage probe (preferably a differential voltage probe) was connected across S2 to measure the switching voltage V_s, whose duty cycle was controlled by the control card. Two current probes are put around inductors L_1 and L_2 to measure the inductor L_1 current i_1 and the inductor L_2 current i_2, as green and yellow lines in Fig.5.4.

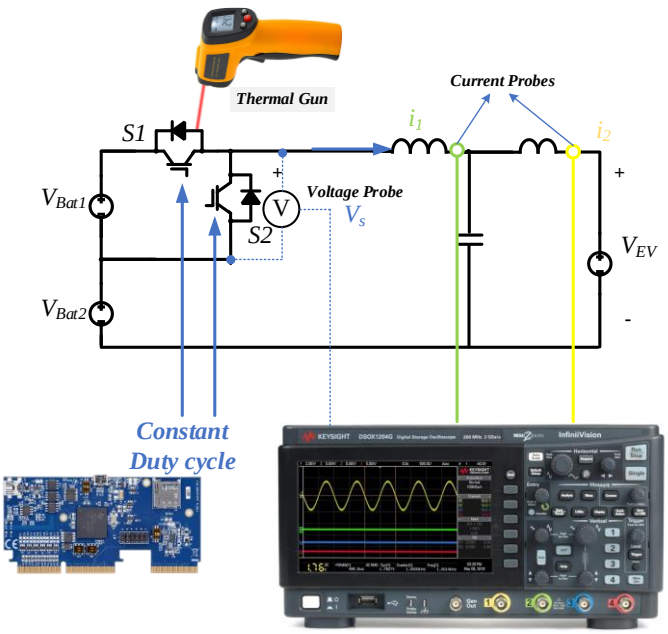


Figure 5. 4: Measurements setup of the RDC converter under mode 1 (Partial Power Processing)

With the arranged testing devices, the RDC converter was tested first under low power. Table 5.4 shows the working conditions of the RDC converter.

Table 5. 4: Working conditions of the RDC converter under low power conditions

Parameters	**Values**
V_{B1} / V	60
V_{B2} / V	10
Duty Cycle	20%
Switching frequency / kHz	40
I_2 (output current) / A	7.5

Based on the working conditions shown in Table 5.4, the RDC converter was working under mode 1 (partial power processing). The S1 and S2 form a buck topology. The working principle of this topology has been discussed in Section 2.1. The key waveforms (the switching voltage v_s and inductor current i_1) of the RDC converter are previously illustrated in Fig.2.4.

In this setup, the switching voltage v_s (voltage across S2) and the inductor current i_1 were measured. The testing results are shown in Fig.5.5.

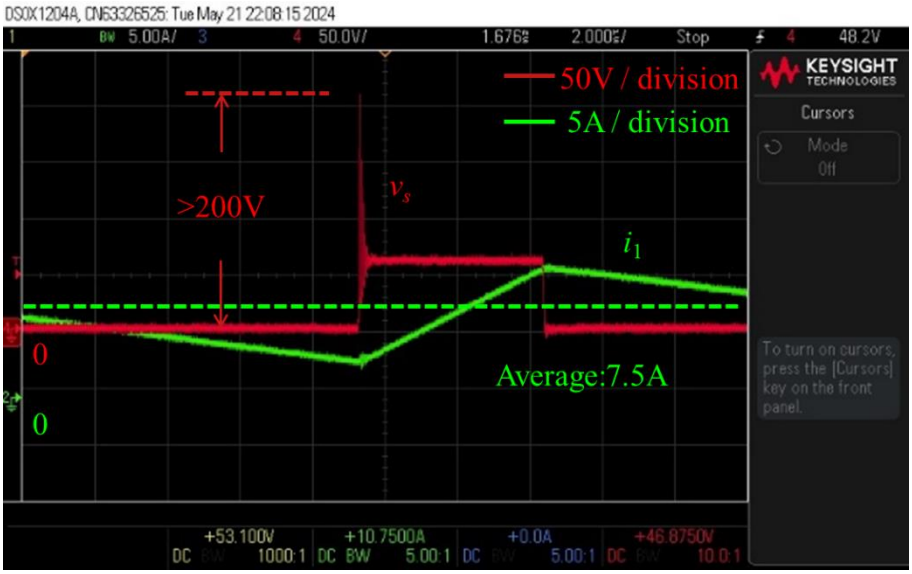


Figure 5. 5: The key waveforms of the RDC converter. (The scale for v_s is 50V per division, while the scale for i_1 is 5A.)

The green curve is the inductor L_1 current i_1. The tested inductor current i_1 shows a triangular waveform. This coincides with the inductor current waveform shown in Fig.2.4 very well. The average value of i_1 is 7.5A. The red curve is the switching voltage v_s. It is a rectangular waveform, except for the high-frequency oscillation at the rising edge. These two waveforms indicate that the RDC converter operates properly based on its working principle.

However, there is an unexpected high-frequency oscillation at the rising edge of the switching voltage v_s. The peak value of v_s is higher than 200V. This could lead to several problems for the RDC converter. To see the high-frequency oscillation, the waveforms are enlarged, as shown in Fig.5.6.

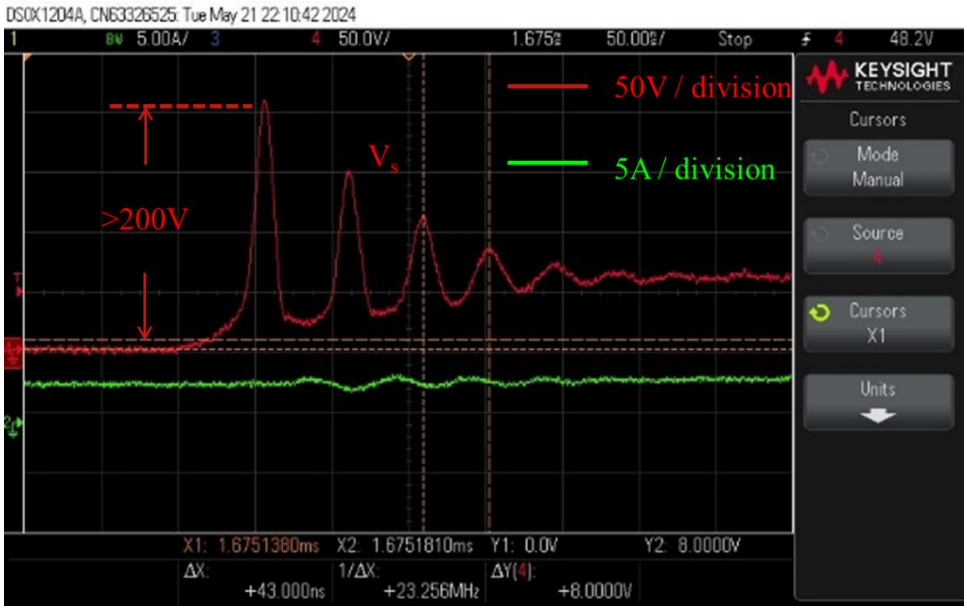


Figure 5. 6: The enlarged high-frequency oscillation in the switching voltage waveforms.

From the expanded curve, we can find that the frequency of the oscillation is about 23 MHz. It is much higher than the switching frequency. The high-frequency oscillations observed at the waveform of v_s are known as switching rings. It can lead to the following consequences [45].

- On one hand, the high amplitude of the ring might exceed the breakdown voltage of MOSFETs - this will shoot through the MOSFETs.
- On the other hand, the ring frequency is usually much higher than the switching frequency, resulting in very high dv/dt in the power circuit. The high dv/dt will then introduce very high conducted and radiated EMI, which might affect the other signal processing circuit nearby and even make the final product not compatible with EMC testing.

Therefore, it is necessary to dampen the high-frequency oscillation before we increase the power of the RDC converter. An RC snubber circuit [46] design procedure and results can be found in Appendix A.

With this designed RC snubber circuit, the oscillation has been significantly damped, as shown in Fig.5.7.

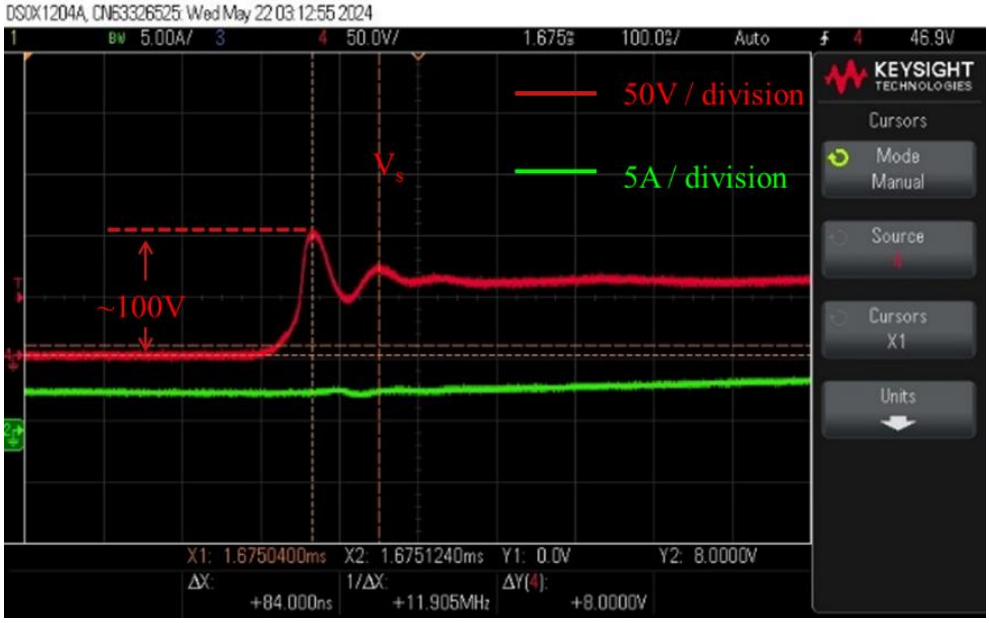


Figure 5. 7: The switching voltage waveform with the designed RC snubber circuit.

From Fig.5.7, we can easily make the following conclusions.

- The peak value of the oscillation is reduced to about 100V (half of the original oscillation). This can prevent the MOSFETs from shoot-through due to high voltage across them.
- The original oscillation shows a sinusoidal waveform lasting for several periods. The designed RC snubber circuit can eliminate the oscillation after about one cycle. This can significantly reduce EMI.

The detailed design procedure and illustrations can be found in Appendix A. With this designed RC snubber circuit, the RDC converter can operate safely under high voltage and high-power conditions.

5.2.2 Power Efficiency

In the previous testing, the basic working principles of the RDC converter have been verified. The RDC converter operates properly under low power conditions. Besides, the designed RC snubber circuits significantly reduced the high-frequency oscillations. This prevents the MOSFETs from shooting through. The efficiency of the RDC converter with the designed RC snubber circuit was then tested under different power conditions. The results of the efficiency are analyzed in this subsection.

To accurately measure the efficiency of the RDC converter, the power analyzer HIOKI PW6001 was implemented, as shown in Fig.5.8.

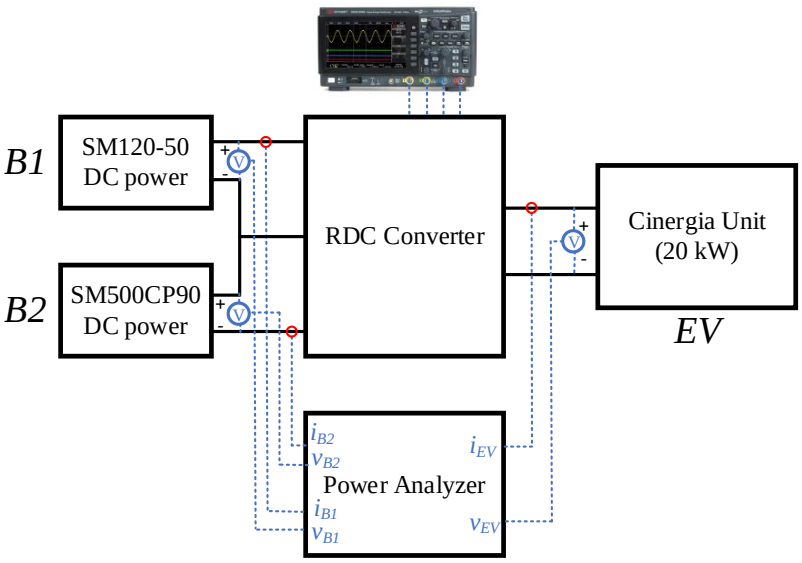


Figure 5. 8: The diagram of the efficiency testing setup

- At the input side, the voltage and current of the input B1 are i_{B1} and v_{B1} respectively. The input power P_{RDC} from B1 can be calculated. Similarly, the input power P_{B2} from B2 can be calculated by the multiplication of i_{B2} and $v_{B2.}$
- At the output side, the i_{EV} and v_{EV} are measured. The multiplication of is the output power P_{EV} of the RDC converter.

The efficiency of the RDC converter can be calculated as shown in equation (5.1).

$$\eta = \frac{P_{EV}}{P_{RDC} + P_{B2}} = \frac{i_{EV} v_{EV}}{i_{B1} v_{B1} + i_{B2} v_{B2}} \tag{5.1}$$

To test the efficiency of the RDC converter, an open-loop control setting was first implemented. In the open loop setting, the duty cycle was set to be 50% constant. The closed-loop control will be discussed later in Section 5.3. Table 5.5 summarizes the working conditions of the RDC converter.

Table 5. 5: Working conditions of the open loop control.

Parameters	**Values**
V_{B1} / V	100
V_{B2} / V	350
Duty Cycle	50%
Switching frequency / kHz	40
V_{EV} / V	400
I_2 / A	5-50
Power / kW	2-20

Under open loop conditions, the input voltages (V_{B1} and V_{B2}) and output voltage (V_{EV}) are set to be constant. The output current I_2 increases stepwise from 5A to 50A, so the total charging power increases from 2 kW to 20 kW (rated power).

With the working conditions in Table 5.5, the RDC converter was tested under mode 1 only, under which the RDC converter can achieve very high efficiency due to partial power processing. Since the RDC converter under mode 2 rarely happens in normal operation, the efficiency under mode 2 was not tested in this project. The measurements setup to test the key waveforms of the RDC converter is the same as the one shown in Fig.5.3.

1) First iteration

As shown in Table 5.5, the output current (EV current I_2) increases from 5A to 50A slightly. The associated power of the RDC converter increases from 2 kW to 20 kW. The efficiency of the RDC converter is measured at different output currents. The curve of the efficiency versus the output current is shown in Fig.5.9. From the curve, we can see that the peak efficiency of the RDC converter is about 99.2%. This is much higher than 97% (state-of-the-art DC/DC converter mentioned in [3]). The RDC converter reaches the peak efficiency at 40% of the load.

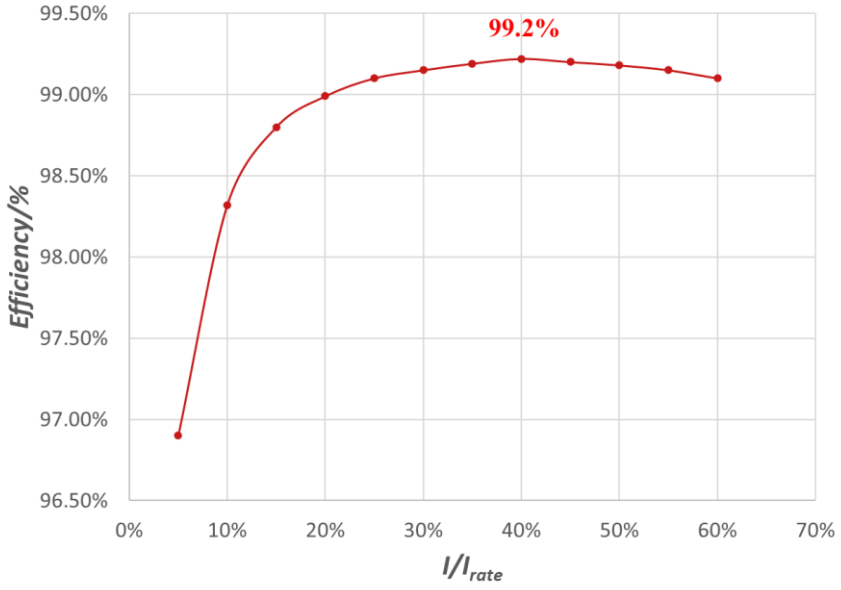


Figure 5. 9: Power efficiency curves versus output current of the RDC converter under mode 1

The testing results show that the RDC converter can achieve very high efficiency (99.2%). However, as shown in Fig.5.9, the measurements of the RDC converter stop at 60%

load (12 kW). The reason behind this is that the temperature of the MOSFETs nearly reaches the limit of the MOSFETs. It is not allowed to increase the power further.

This high-temperature rise of the MOSFETs is due to the insufficient heat dissipation for the MOSFETs. The physical model and equivalent thermal resistance network were discussed in Section 3.5.3. A 1mm thick thermal pad is selected from the lab between the MOSFETs and heatsink. The thermal resistance of the thermal pad might be too large to dissipate the heat sufficiently.

2) Second iteration (Improved thermal management.)

To improve the thermal performance of the cooling system, a much thinner (0.037 mm) thermal pad is selected from the market, as shown in Table 5.2. the thickness is now 30 times lower than the previous thermal pad. The thermal resistance is expected to be much lower.

With the changed thermal pad, the RDC converter is tested again under the conditions shown in Table 5.5. The power of the RDC converter increases to the rated power (20 kW) this time. The efficiency under different loads is shown in Fig.5.10. Besides, the temperature of S1 is measured by a thermal gun (see Fig.5.3).

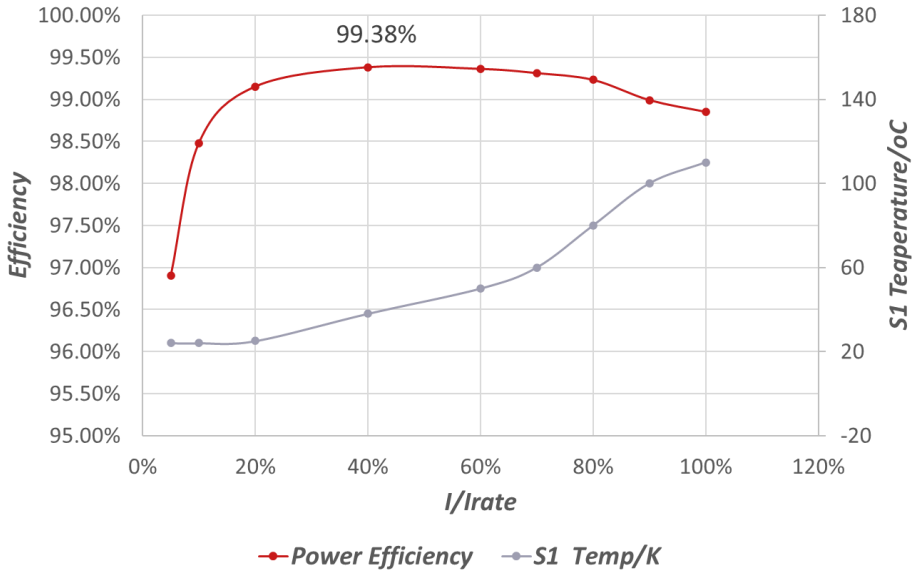


Figure 5. 10: Power efficiency and S1 temperature curves versus output current of the RDC converter (under mode 1)

Fig.5.10 shows the efficiency and the temperature of S1 of the RDC converter under mode 1 (partial power processing). The red curve illustrates the efficiency versus output current, while the grey curve shows the temperature of S1 under different output currents.

- From the results, we can see that the peak efficiency of the RDC converter goes up to 99.38% at 40% (20A) of the output current. This is higher than the previous efficiency (99.2%). So, the improved thermal system helps to dissipate heat as well as improve the efficiency.
- The efficiency decreases to 98.9% at the full load. The case temperature of S1 increases to about 110 ^{o}C at the full load. Besides, when the output current is approaching the rated current (50A), the slope rate of the temperature rise increases. This will rapidly increase the R_{dson} (on resistance of the MOSFETs). The MOSFETs will then produce higher power loss. This deteriorates the efficiency of the RDC converter at the full load. The heatsink system should be further optimized to provide sufficient heat dissipation for the MOSFETs at the full load, so as to cool down the MOSFETs and reduce power loss.

From the measurements setup shown in Fig.5.3, the key waveforms of the RDC converter under 20 kW full load condition are recorded, as shown in Fig.5.11.

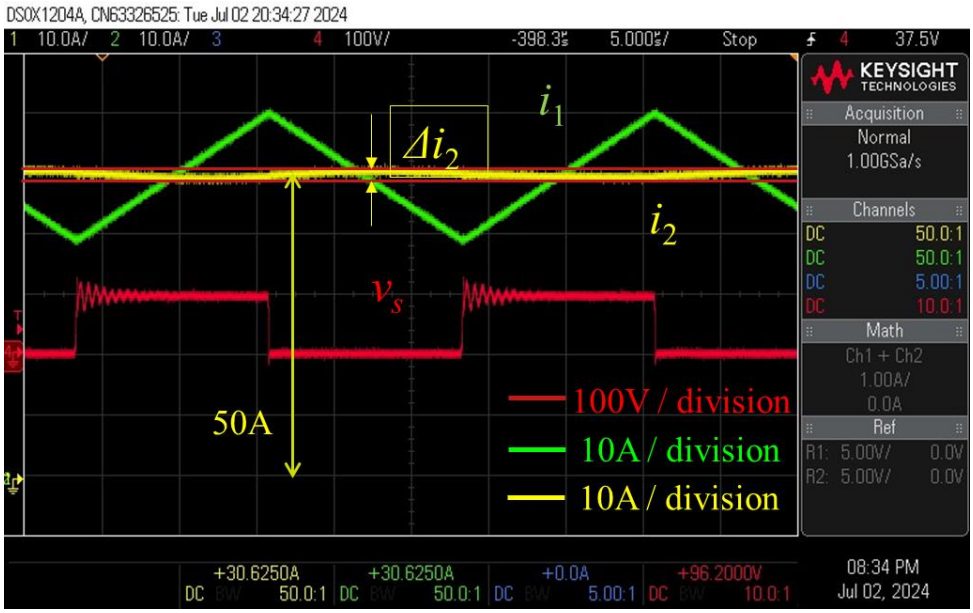


Figure 5. 11: Key waveforms of the RDC converter under mode 1 (partial power processing)

The red waveform shows the switching voltage v_s cross S2. It is a rectangular waveform with a duty cycle of 50%. As can be seen, it still has a high-frequency oscillation at the rising edge, but the magnitude of the oscillation is relatively small (<120V) by the proper snubber

design. This small oscillation will not bring too severe EMI problems and will not shoot through the MOSFETs. The original magnitude of the oscillation is quite large (up to 300V).

The green waveform shows the inductor L_1 current i_1. It demonstrates a very clean triangular waveform, which coincides with the theoretical analysis shown in Fig. 2.4. The average value of i_1 is equal to 50A. The inductor current ripple Δi_1 (peak-to-peak) is about 20A, it also coincides with the desired inductor current ripples of 40%, as shown in Table 5.2. Finally, the output current i_2 is shown as the yellow waveform. The average value of the output current i_2 is also 50A. But the output current ripple Δi_2 (peak-to-peak) is about 2A (4% of 50A). This is a little bit larger than the Tesla Supercharger V3, but it is still less than the CCS and CHAdeMO standard (5%). To further reduce the output current ripple, the output inductor L_2 can be slightly increased to provide sufficient filtering of the current ripples.

5.3 Closed Loop Control

The power efficiency of the RDC converter under open-loop control has been verified in Section 5.2. In this subsection, the designed current feedback closed-loop control (see Section 4.2) will be implemented and tested. The constant current (CC) charging performance is investigated. With the closed loop current feedback control, the efficiency of the RDC converter is tested again for an EV fast charging scenario (fast charging SOC: 20-80%). Finally, the step response of the current control loop is tested and analyzed.

5.3.1 Constant Current EV Charging

The RDC converter is controlled by a DSP28379 control card, as shown in Fig.4.22. The designed PI controller is implemented in the DSP28379 control card. The working conditions of the closed-loop control for the RDC converter are illustrated in Table 5.6. As discussed in Fig.5.8, the RDC converter faces extremely high temperatures for the MOSFETs at the full load (50A).

Besides, the control performance of the RDC converter will not be affected by the value of the output current. (According to equation (4.17), the loop gain of the RDC converter is not affected by the output current). This means that the control performance (including dynamic performance) will be the same at different output currents.

To safely test the control performance of the RDC converter, the output current is recommended to be less than 50A. As shown in Fig.5.10, the RDC converter reaches the peak

efficiency (~99.4%) when the output current is 20A. Therefore, the output current is controlled to be 20A by the controller in this subsection.

As shown in Table 5.6, the sampling frequency is set to be equal to the switching frequency. The power of the RDC converter under 20A is about 8 kW. According to Fig 2.5, we can see that the EV voltage varies from 360V to 380V when SOC increases from 20% to 80%. Later on, the EV voltage will change from 360V to 380V, the RDC converter will operate under CC charging mode to charge the EV battery (Cinergia battery emulator).

Table 5. 6 Working conditions of the closed-loop control.

Parameters	**Values**
V_{B1} / V	100
V_{B2} / V	350
Switching frequency / kHz	40
Sampling frequency / kHz	40
V_{EV} / V	360-380
I_{EV} (I_2) / A	20
Power / kW	~8

Fig 5.12 shows the key waveforms of the RDC converter under 20A CC closed-loop control. The output current i_2 (the EV current) is well controlled to be 20A. The inductor L_1 current i_1 and the switching voltage v_s waveforms remain similar to the waveforms shown in Fig 5.11. Overall, the RDC converter operates stably with the designed PI controller, which verifies the theoretical analysis of the stability issue in Section 4.3. In addition, the high-frequency (40 kHz) ripple caused by the switching behavior is neglectable (<5%).

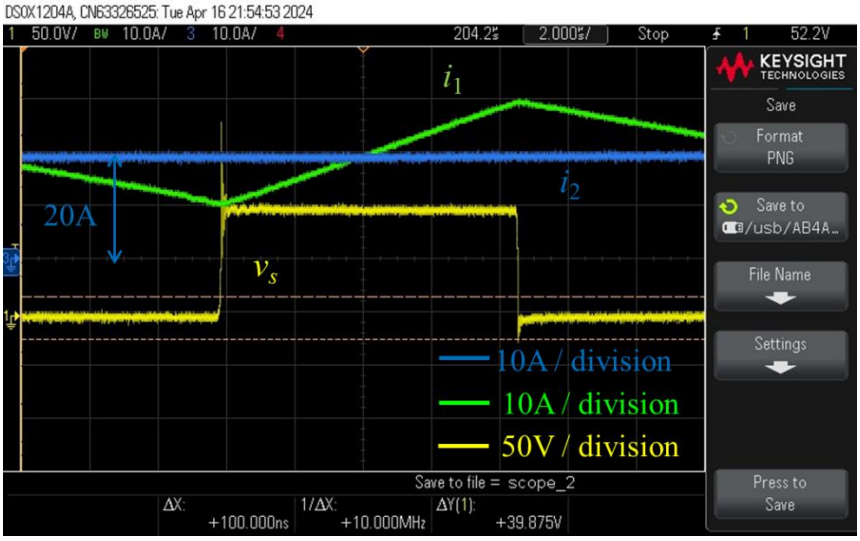


Figure 5. 12: The key waveforms of the RDC converter under 20A CC closed loop control

In Section 5.2, we have illustrated the power efficiency versus load of the RDC converter under open loop control. However, the charging efficiency of a full EV charging scenario has not been tested. Fig 5.13 shows the efficiency of the RDC converter under 20A CC closed loop control, when the B2 voltage equals 350V (Maximum voltage of B2). From Fig 5.13, we can see that the efficiency of the RDC converter is always larger than 99.15% for an EV fast charging scenario.

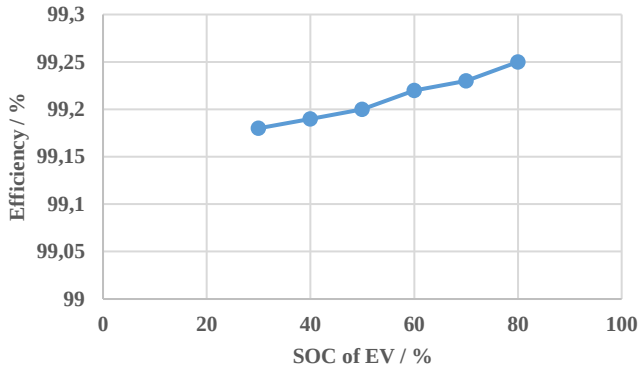


Figure 5. 13: Efficiency Curve under 20A CC charging (V_{B2}=350V)

As mentioned in Section 3.1, the B2 voltage will change from 310V to 350V. The efficiency of the RDC converter when the B2 voltage is equal to 330V (Nominal voltage of the B2) is measured, as shown in Fig.5.14.

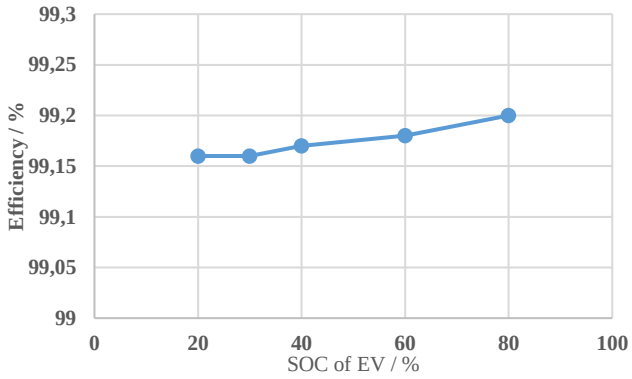


Figure 5. 14: Efficiency under 20A CC Charging (V_{B2}=330V)

The efficiency of the RDC converter is also always larger than 99.15%. According to equation (2.2), when V_{B2} is smaller, regarding the same EV voltage V_{EV}, v_1 regulated by the RDC converter will be larger. Therefore, the partial power processed by the RDC converter is a little bit larger, so the efficiency of the RDC converter is a little bit lower. Overall, the efficiency

of the RDC converter remains extremely high for the whole charging scenario (EV SOC: 20-80%).

5.3.2 Step Response

In Section 4.2, we have designed the PI controller and discussed the performance of the control system under frequency response. However, the time-based performance of the control system has not been analyzed and tested. Step response is often used to analyze the dynamic performance of the control system in the time domain.

According to [27], the step change of the reference current will not be instantaneously from 0A to 50A. The reference current I_{ref} will usually increase step by step. In this case, the reference current I_{ref} has a step change from 20A to 27A (35% step change of 20A). And the response of the output current i_2 (i_{EV}) is measured, as shown in Fig 5.15.

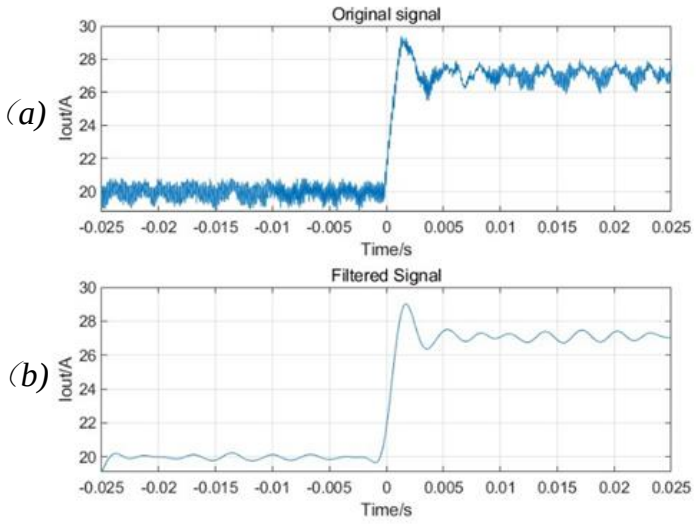


Figure 5. 15: The step response of the closed control loop from

Fig.5.15 (a) shows the original data stored by the oscilloscope. The output current is kept constant basically in the beginning (neglecting the ripples). At the time zero point in the middle, the output current shows a step change with a relatively small overshot (~2A). It turns out to be stable after about 5ms.

From Fig.5.15 (a), the low-frequency ripples of the output current make the system look unstable. However, these low-frequency ripples are introduced by the EV battery emulator (Cinergia unit). The frequency of this ripple is around 200-2000Hz, which accidentally lies very close to the frequency range of the dynamic response. Later, it was acknowledged by the engineers from Cinergia that these ripples coming from the Cinergia unit. The Cinergia unit

(which emulates the EV battery) is not a real EV battery. It is composed of a series of power electronics circuits and filters, as shown in Fig.5.16. It can emulator the EV battery voltage profile during the charging and discharging. However, it will introduce voltage and current ripples by the switching nature of the power electronics and the limitation of the filters inside the unit[47].

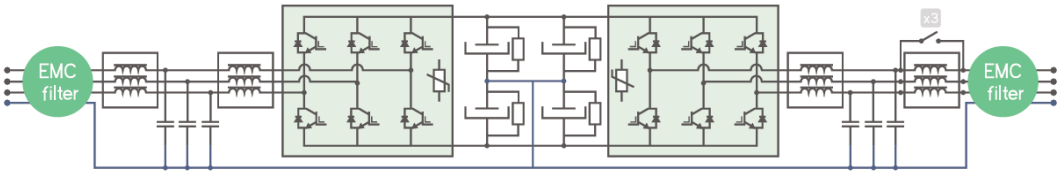


Figure 5. 16: The Circuit diagram of the Cinergia unit used as the EV emulator[47].

A digital band-reject filter [48] was designed to filter out the unwanted ripples from the Cinergia unit. Since the frequency of this ripple is very close to the frequency of the dynamic response, it is very hard to filter out the ripples without affecting the dynamic response by the digital filter.

With a digital signal filter, the curve at the bottom of Fig 5.15 (b) shows the step response of the current closed-loop control. The unwanted ripple is reduced significantly, and the behavior of the step response is kept almost unchanged compared to the curve at the top side. From this step response, we can summarize the control performance as follows:

1) Rise time: < 1ms (rising time from 10% to 90%)
2) Overshot: About 20% (2A)
3) Peak time: About 2 ms
4) Settling time: About 5 ms (5%)

Based on the control performances above, the designed RDC control system is stable with a small overshoot. The control system is also fast with a small rise time and settling time. This time-based dynamic performance can later be compared to the EV charging control standard, so as to evaluate the designed controller. Due to the time limitations, the dynamic performance is not compared with the EV charging control standard. Furthermore, the reference current can be changed to different values (from 0 to 50A). The step response can be repeated to fully satisfy the standard.

5.4 Results Summary

In conclusion, a 20 kW RDC prototype has been designed and built. The testing environment for the RDC converter is arranged. The key experimental results are summarized as follows.

1) The designed RDC converter can achieve 99.4% peak efficiency and 5kW/dm^3 power density. This can be further increased to 7kW/dm^3 by optimizing the heatsink and hardware of the RDC converter.
2) The designed RC snubber circuit can significantly reduce the high-frequency oscillation as discussed in Appendix A.
3) The output current ripple is measured to be about 4%. This is less than the ripple requirement (5%) in CCS and CHAdeMO standards.
4) The RDC converter works under the designed PI controller stably. The output current is kept constant with a very small ripple at the steady state. During a step change of the reference current, the output current can follow the reference current in about 5 ms with a small overshoot.
5) The efficiency of the RDC converter for the whole EV fast charging period (SOC: 20-80%) is also tested under CC control mode. The efficiency is always higher than 99.15%.

6 CONCLUSION

6.2 Main findings

1. We have demonstrated a 20-kW prototype of a partial power DC converter for use in electric vehicle charging. The requirements are directly taken from the commercial standards as set out for example in CCS and CHAdeMO.

2. The power density is 5 kW/L and can be increased to 7 kW/L.

3. Based on the RDC (reduced dissipation converter) concept, we have investigated several topologies. We analyzed the comparative benefits for the simple buck, full bridge, and multi-level (buck series) with respect to efficiency, controllability, and protection.

4. The multi-level topology has 2 modes of charging: mode 1 is used for charging the EV from SOC 5%-100%. This covers most of the commercial EV fast charging scenarios. Mode 2 is for the range SOC=0-5% when over-discharge of EVs has occurred. This last mode 2 is simply a direct buck converter (full power processing) which contrasts with mode 1 where partial power processing is used.

5. We measured peak efficiencies up to 99.4%. This is much higher than the efficiency (around 97%) of the current state-of-the-art EV chargers. Obviously, this means that much less cooling will be required.

6. We designed a single PI controller to regulate both modes for the RDC converter. We assured the system stability by doing an analysis of the network impedance according to the Nyquist criterion.

6.3 Future work

1. AC winding losses in the inductor L1 were estimated to be only around 1-3% of the total winding loss. These were neglected in the current study but should be further investigated for a fully optimized system for the RDC converter.

2. We defined the two modes (1 and 2) above for the operation of the RDC converter. Stable operation at both modes was demonstrated. However, the transition between the two modes has yet to be analyzed and tested. It proved to be very difficult to get a linear model for the dynamic model of the transition between the two modes. Future work might focus on the non-linearity of this process.

3. The step response experiments were limited by the inherent ripples from the Cinergia GE&EL +vAC/DC SiC power supply. The manufacturer has acknowledged this problem and is aiming to find a solution in the future. However, in the meantime, new DC power supplies from a different manufacturer have been ordered.
4. At the rated output current (50A), the efficiency drops somewhat. This is due to heating and excessive temperature generation which increases the resistance of the MOSFET switches. This should be investigated further and improved by better thermal management of the MOSFETs.
5. From the Bode plot, we can derive the dynamic characteristics such as the phase and gain margins as well as the bandwidth. However, at a commercial level of testing, further ranges of step changes over the full range of charging current (0-50A) need to be tested.
6. In this report we have concentrated on constant current (CC) charging. More advanced EV charging profiles can be investigated such as constant current to constant voltage transitions and associated transients and possible overshoots.

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Appendix A---- RC Snubber Design for MOSFETs

During my EngD project, I have the unique opportunity to get involved in an internship with Shell Global Solution B.V.. In this internship, my major responsibility is to explore a practical way of designing snubber circuits for current Si/SiC MOSFETs. This report illustrates the design process of RC snubber circuits to damp high-frequency oscillation during hard switching of Si/SiC MOSFETs.

A.1 Introduction

The high-frequency oscillations will introduce high EMI to the converter and to the environment. In addition, high oscillations might damage the Si/SiC MOSFETs. The high-frequency oscillations are due to the parasitic parameters as well as the reverse recovery effects of the body-diode of MOSFETs.

Section 1 introduces the basic cause of the high-frequency oscillations. An RC snubber design process is then applied to SiC MOSFET in Section 2. Section 3 analyzes the results. Section 4 repeats the design process and further verifies the practicality of the design process.

A.1.1 Cause of problem

The basic half-bridge circuit is shown in Figure 1.1.

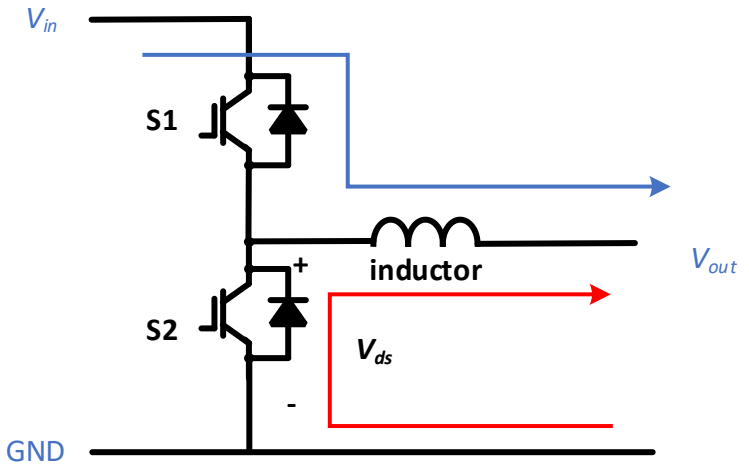

Figure 1. 1 The universal half-bridge circuit

S1 and S2 are high-power Si MOSFETs IRF300P226. The basic working principle of the half-bridge circuit is illustrated in Figure 1.1. When S1 is on and S2 off, the inductor current is established in a blue loop by input power. When S1 is off and S2 is on, the inductor current flows through S2. Usually, to prevent short-circuit at the input side, there is a deadband when S1 and S2 are both off during the switching period.

One of the transition periods is: when turning off S2 and turning on S1. During deadband, that is S1 is not turned on yet. The inductor current flows through the body diode of S2. After the deadband period, S1 is turned on, current commutates to the blue loop and a reverse recovery effect occurs in S2. The effect of the reverse recovery of the body diode on the V_{ds} waveform of S2 is observed. The waveform is shown in Fig. 1.2 as below.

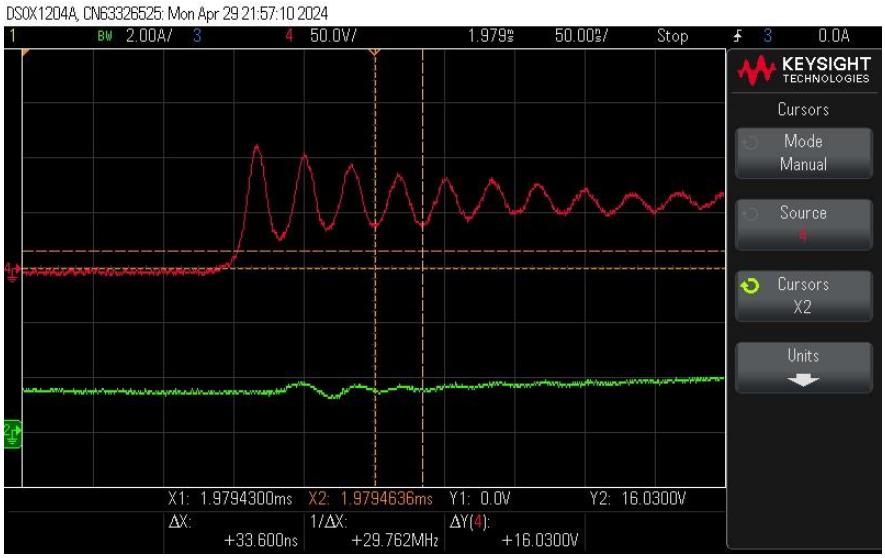

Figure 1. 2: The high-frequency oscillation on MOSFET S2

The high-frequency oscillations observed at the waveform of V_{ds} are known as MOSFETs switching rings. On one hand, the high amplitude of the ring could exceed the breakdown voltage of MOSFETs will shoot through MOSFETs. On the other hand, the ring frequency is usually much higher than the switching frequency, resulting in very high dv/dt in the power circuit. The high dv/dt will then introduce very high conducted and radiated EMI, which might affect the other signal processing circuits nearby and even make the final product not compatible with EMC testing. Therefore, it is very important to suppress or dampen the switching ring as much as possible.

There are several simple and straightforward ways to dampen the switching rings: optimizing PCB layout to reduce parasitic inductances, choosing better reverse recovery performance MOSFETs as well as slow switching speed, etc. In this work, though the above methods can reduce the ring to some extent, we can still observe a very high ring, which could potentially shoot through the MOSFETs and introduce high EMI. An RC snubber circuit is then needed to dampen the switching ring further.

A.1.2 Equivalent Circuit of switching ring

Fig. 1.3 illustrates the half-bridge circuit including main parasitic inductors and capacitors. The parasitic capacitor mainly comes from the equivalent output capacitor (Coss1 & Coss2) of MOSFETs (S1 & S2). The parasitic inductors are from PCB traces (Lp1 & Lp4) as well as MOSFETs long leads (Lp2 &Lp3). The RC snubber circuit is put between the switching node (SW node) and the ground, as shown in Fig. 1.3.

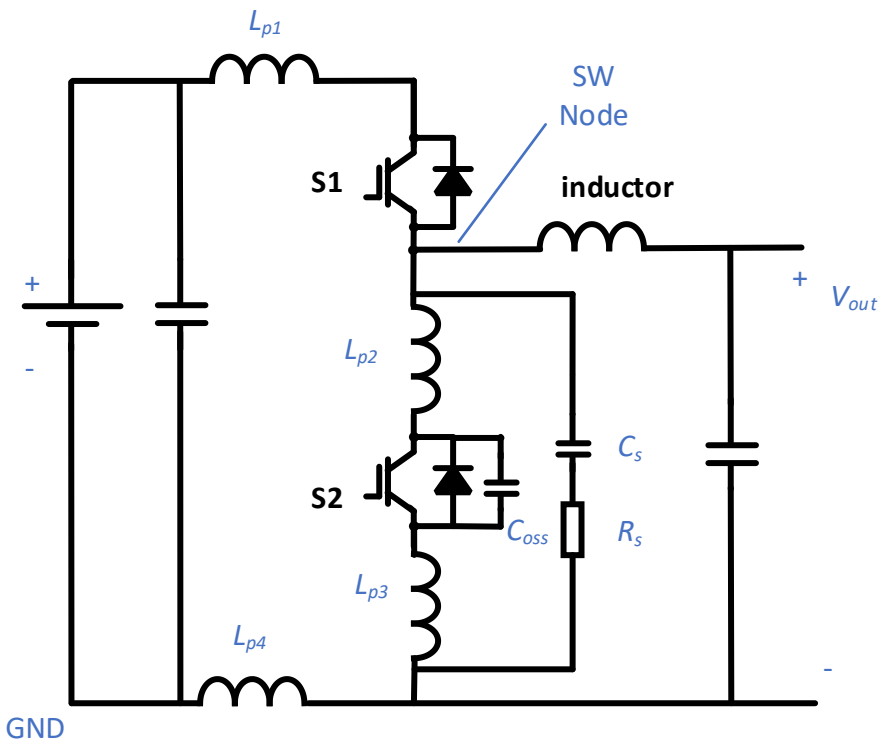

Figure 1. 3: Half bridge circuit including main parasitic parameters.

First, the switching process is usually completed in dozens of nanoseconds. In such a short period of time, the inductor (L) current (output current) almost does not change. So, the output inductor L will not contribute to the switching ring. Second, S1 has been turned on, Coss1 is short-circuited. Overall, we can get a simplified equivalent circuit, as shown in Fig. 1.4. The equivalent circuit is an LC resonant circuit with the added RC snubber. The L_{eq} is the sum of the L_{p1}, L_{p2}, L_{p3}, and L_{p4}, and C_{eq} is the sum of all the parasitic capacitances including Coss2. It is very hard to get the accurate values of those parasitic parameters by direct measurements or from manufacturers. Later on, a detailed method will be introduced to get those values.

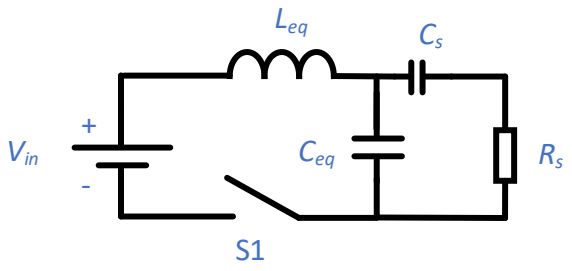

Figure 1. 4 The equivalent circuit during the switching process with the added RC snubber.

A.2 RC Snubber Design process.

A.2.1 Determine L_{eq} and C_{eq}

In the above section, we have identified the equivalent RLC resonant circuit of the switching ring. However, it is very difficult to get accurate parameters from the datasheet or measure directly the

inductances and capacitances. An easier method to get the parasitic parameters is to measure the switching ring frequency. For a simple LC circuit, we know that:

$$f_{r0} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}$$

, where f_{r0} is the frequency of the switching ring without RC snubber in the circuit. If we add an extra known capacitor across S2 (C_{add}), the switching ring frequency will change to another value f_{r1}, as shown in the equation below.

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{eq}(C_{eq} + C_{add})}}$$

Till now, we have two equations and two unknowns. We can calculate the unknown values L_{eq} and C_{eq}.

$$C_{eq} = \frac{C_{add}}{x^2 - 1}$$

$$L_{eq} = \frac{1}{(2\pi f_{r0})^2 C_{eq}}$$

In the above section, an elegant method has been introduced to calculate the parasitic L_{eq} and C_{eq}. Before we start the measurements and determination of parasitic parameters, we have to think about the characteristics of MOSFETs. At different working conditions of MOSFETs, the parasitic capacitance changes. Fig. 2.1 shows the variation of parasitic capacitances at different working conditions for C3M0015065K SiC MOSFET.

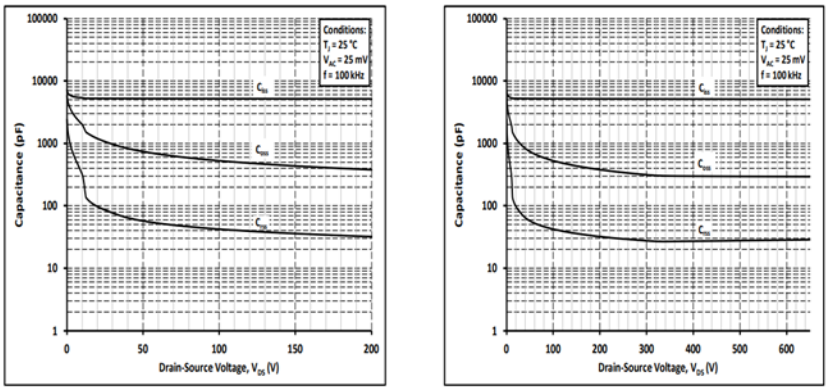

Figure 2. 1: Parasitic capacitances of the SiC MOSFET C3M0015065K

At the different V_{ds} voltage, the output capacitance C_{oss} varies a lot, especially at the low V_{ds} voltage. We can start measurements at the rated voltage, e.g. V_{ds}=400V, however, operating MOSFETs at the high voltage the very first time could shoot through them due to the switching ring. As shown in Fig. 1.2, if the ring amplitude is still two times the operating voltage of 400V, then the ring amplitude goes up to 800V and could be shot through the MOSFETs with 650V breakdown voltage. A good starting point is to measure the switching ring at a reasonable operating voltage. In this case, 100V is chosen to start.

1) 100V10A

The aforementioned half-bridge circuit (buck converter) is operated at the following conditions, as

shown in Table 2.1.

Table 2. 1: Operating conditions of the half-bridge circuit (Buck Converter)

V_{in}/V	100
Duty Cycle	20%
V_{out}/V	20
I_{out}/A	10

Fig 2.2 shows the switching ring waveform and output inductor current across the drain source of S2. The red curve shows the voltage V_{ds} of S2. The inductor L current is shown in the green waveform. From the red curve, we can measure that the switching frequency f_{r0} is around 33.33 MHz.

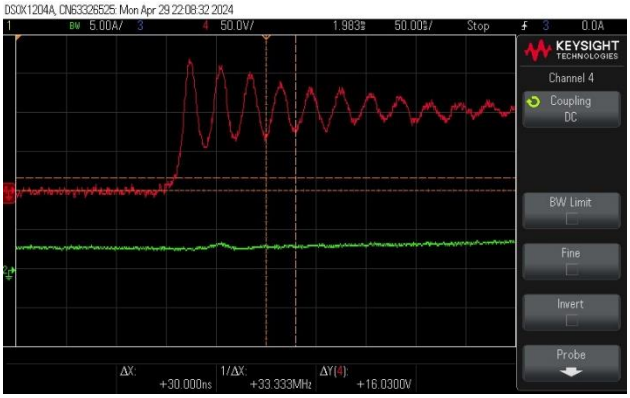

Figure 2. 2: Switching ring of S2 without RC snubber in place

2) With an added capacitor of 3.3 nF

The same working condition, as shown in Table 2.1, is then applied to the half-bridge circuit with an added known capacitor of 3.3 nF. Similarly, we can get the ring frequency f_{r1}. That is about 14.286 MHz.

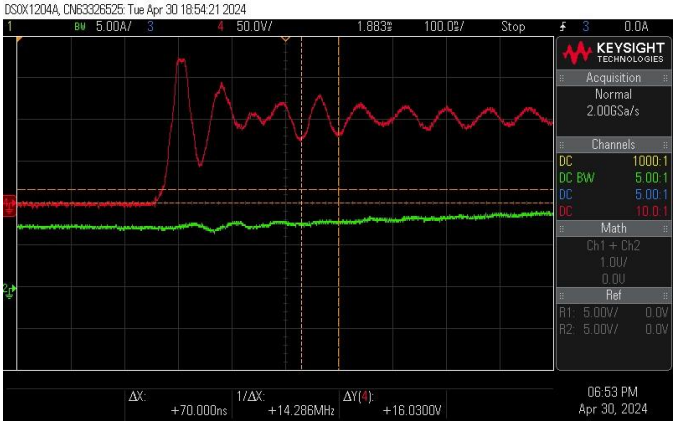

Figure 2. 3: Switching ring of S2 with an added capacitor 3.3 nF

With the two measured ring frequencies f_{r0} and f_{r1}. We can calculate the L_{eq} and C_{eq}, as follows.

$$x = \frac{f_{r0}}{f_{r1}} = 2.33$$

$$C_{eq} = \frac{C_{add}}{x^2 - 1} = 0.744\ nF$$

$$L_{eq} = \frac{1}{(2\pi f_{r0})^2 C_{eq}} = 30.68\, nH$$

A.2.2 RC Snubber Design Process Step-by-step

1) Theory of RLC resonant circuit

Usually, C_s is much larger than C_{eq}. If that is the case, C_s is approximated as a short-circuit. So, the equivalent circuit is then simplified, as shown in Fig. 2.4. The equivalent circuit of the ring is basically an RLC resonant circuit. If R_s and C_s are well designed, the ring or oscillations caused by L_{eq} and C_{eq} will be damped to an acceptable range.

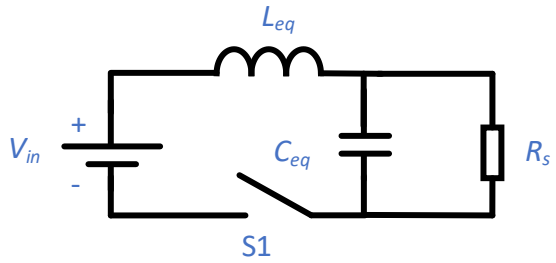

Figure 2. 4: The simplified equivalent circuit when $C_s >> C_{eq}$

$$V_{in} = L_{eq} C_{eq} \frac{d^2 u_{C_{eq}}}{d^2 t} + \frac{L_{eq}}{R_s} \frac{du_{C_{eq}}}{dt} + u_{C_{eq}}$$

Theoretically, if R=0, the circuit oscillates indefinitely. But this is a practical impossibility since there is always some resistance in real circuits. In RLC circuit theory, the circuit oscillates indefinitely if ζ = zero, although this is a practical impossibility as there is always some resistance in a real circuit. As ζ increases towards one, the oscillation becomes more damped that is, tends to decrease over time with an exponential decay envelope. This is an "underdamped" response. The case ζ = one is known as "critically damped" and is the point at which oscillation just ceases. For values of greater than one (overdamped), the response of the circuit becomes more sluggish with the waveform taking longer to reach its final value. There is therefore more than one possible degree of damping that we could build into a snubber, and the choice of damping is part of the snubber design process. For this configuration of the RLC circuit, the relationship between ζ, R_s, L_{eq}, and C_{eq} is:

$$\zeta = \frac{1}{2R_s}\sqrt{\frac{L_{eq}}{C_{eq}}}$$

It is possible to dampen the high-frequency oscillations by a single resistor. However, in this typical half-bridge circuit, we can not mount a resistor directly across S2. If so, the switch S2 is shorted by the resistor. That is basically why we need capacitor C_s connected in series with Rs. The value of C_s should be carefully designed to avoid interfering with the normal operation of the half-bridge circuit. For an RC circuit, its cut-off frequency f_c is:

$$f_c = \frac{1}{2\pi R_s C_s}$$

Again, we must choose which value of f_c to use, and there is no single correct answer to this question.

The cut-off frequency of the snubber must be low enough to effectively short-circuit the undamped oscillation frequency f_{r0}, but not so low as to present a significant conduction path at the operating frequency of the circuit (for example 40 kHz in this case). A good starting point has been found to be $f_c = f_{r0}$.

2) Design the RC snubber in practice

Now, we have enough information to design the RC snubber. The practical steps are illustrated as follows.

- Measurement of the high-frequency rings: In the RC snubber design, accurate measurements of the high-frequency ring are very important. Fig.2.5 shows the voltage probe to measure the high-frequency ring. To reduce the impacts from the long leads of the probe and external EMI, the leads of the probe should be put as close as possible to the MOSFETs. The leads of the probe shown in Fig.2.5 are used to measure the ring in this study.

Figure 2. 5: The voltage probe to measure the ring accurately

- Calculation of the L_{eq} and C_{eq}, as discussed in Section 2.1.
- Set damp ratio ζ of the RC snubber to be equal to one. The R_s can be calculated as follows.

$$R_s = \frac{1}{2}\sqrt{\frac{L_{eq}}{C_{eq}}} = 3.21\ \Omega$$

- With the calculated R_s, 3.3 Ω (R_{s1})can be selected. Set the cut-off frequency $f_c = f_{r0}$. The C_s can be calculated as follows.

$$C_s = \frac{1}{2\pi R_{s1} f_{r0}} = 1.45\ nF$$

- Two 3.3 nF ceramic capacitors are connected in series to provide the required capacitance.

A.3 Results and analysis

With the designed RC snubber circuit parameters, 3.3Ω resistor $R_{s1,}$ and two 3.3 nF ceramic capacitor C_s are mounted across the switch S2. The reason to use ceramic capacitor is that it has relatively lower parasitic inductance, so as to improve the effectiveness of the RC snubber. The results of damping high-frequency oscillations are shown below.

A.3.1 100V10A with designed RC snubber

With the same working conditions as shown in Table 2.1, the S2 V_{ds} waveform is shown in the red curve in Fig. 2.6. The green curve is the output inductor current waveform. Compared to Fig. 2.2, the RC snubber has significantly damped the high-frequency ringing.

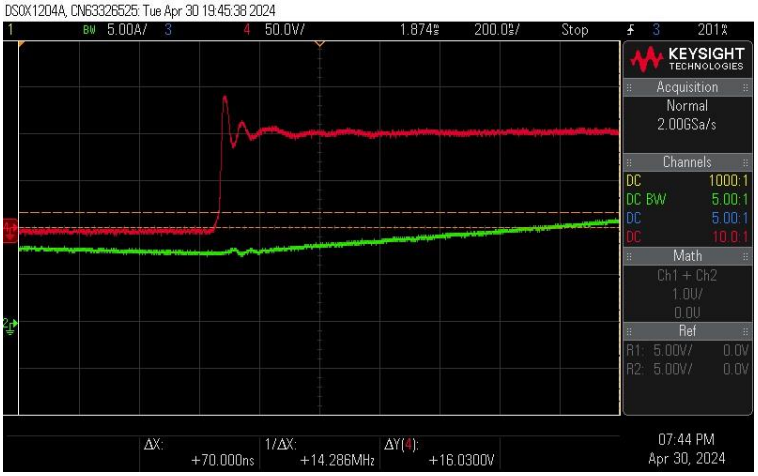

Figure 2. 6 S2 V_{ds} waveform with the designed RC snubber.

A.3.2 200V13A with designed RC snubber

To test the effectiveness of the RC snubber at higher working voltage, the half-bridge circuit was tested at the working condition shown in Table 2.2.

Table 2. 2: Operating conditions of the half-bridge circuit (Buck Converter)

V_{in}/V	200
Duty Cycle	20%
V_{out}/V	20
I_{out}/A	13

As shown in Fig. 2.7, we can find that the designed RC snubber is more effective when working at higher voltage. The peak value of the ring is about 250V (25%) with 200V input voltage. Previously, the peak value of the ring was over 40% of the input voltage.

If we recap the parasitic capacitance C_{oss} variations of S2 (in Fig. 2.1), we can find that C_{oss} decreases when V_{ds} is higher. According to LC resonant theory, lower C_{oss} means resonance frequency is higher. With the same RC cut-off frequency, the ring is more effectively damped. Therefore, designing the RC snubber circuit at a relatively lower input voltage is effective. Especially when the ring is too high to allow the MOSFETs to work at high voltage during the parasitic parameters determination stage, since a high ring could potentially shoot through the MOSFETs.

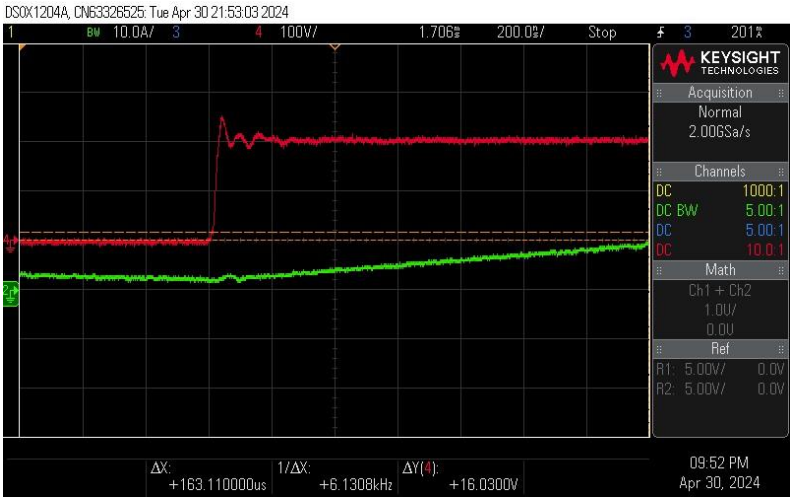

Figure 2. 7: S2 V_{ds} waveform with the designed RC snubber at a higher working voltage

A.4 Summary

In the above sections, we have designed RC snubber circuits for SiC MOSFETs, the results show that the designed RC snubber circuits can significantly damp the high switching ring. The design procedure is suitable for Si MOSFETs too. Still, there is a peak at the rising edge of the V_{ds}. If necessary, it can be further reduced by slowing down the turn-on speed of S1, e.g. increasing turn-on resistance and adding an input gate-source capacitance. Besides, when the output inductor current increases, the ring amplitude increases. This needs to be further investigated.