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DC Testing of Analog Integrated Circuits with Piecewise Linear Approximation and Interval Analysis

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Abstract—**In this paper a test method for analog circuits is presented which is based upon simple DC measurements that can be performed directly on the wafer. Our method handles parameters at various levels, e.g. process, device and circuit parameters. In contrast to other methods that use parameter intervals, our method obtains a mathematical relation between the parameters, which results in a more powerful decision criterion. The method may be used as the basis for automatic testing.**

I. Introduction

Testing analog circuits is an issue of increasing importance in IC production. This is mainly caused by the integration of ever greater analog functionality on a single chip, for instance as interface circuitry in mixed-signal integrated circuits [1, 2]. A major problem with analog circuits testing is the occurrence of hard faults and soft faults [3, 4, 5]. The former cause the failure of a complete function of the device under test (DUT), and are comparable to the digital stuck-at faults. The latter are deviations of parameters outside their permissible interval. A related problem in the analog test domain is that multiple relevant parameters must be deduced in a complete test, such as impedances, transient and frequency domain behavior, distortion, etc.

Hence a reduction in cost, time and complexity of analog circuits testing is beneficial in IC manufacturing. This can be accomplished by using DC measurements. Not all parameters can be deduced with these measurements, since only time-independent behavior is analyzed. However, using DC measurements a high percentage of hard and soft faults can be detected [6]. Thus, in the fabrication process, a large amount of faulty devices can be sieved out and dumped prior to packaging, which may save quite an amount of money.

In this paper a test method for analog circuits is presented which is based upon simple DC measurements that can be performed directly on the wafer. The method uses parameter intervals, which are inherent properties of analog circuits (e.g. gain > 80 dB). Our method handles parameters at various levels, e.g. process, device and circuit parameters. In contrast to other methods that use parameter intervals (e.g. [14]), our method obtains a mathematical relation between the parameters. The method may be used as the basis for automatic testing.

The proposed test procedure consists of three phases. In the pre-test phase, using a special technique, the complete DC performance of the DUT is obtained. Since all parameters are treated as intervals one obtains a space, called the state-space, in which the relation between the parameters and the DC performance is expressed. In the test phase some DC voltages and currents on some nodes are measured. In the post-test phase, the measured data is mapped on the computed state space. If the mapping fails then it is concluded that the DUT is defect.

To illustrate this test method we assume, without loss of generality, that only the threshold voltage v_{th} of MOS devices varies within a wafer and from wafer to wafer, due to manufacturing process variations or spot defects. Thus the behavior of the circuits on the wafer can differ from the simulation results in the synthesis phase. Now the testing problem is to detect whether or not the circuit is functioning -concerning the v_{th} deviation- with the measurement of only a few points of the DC transfer characteristic.

Analog circuits are modeled with the piecewise linear modeling technique, as explained briefly in section II. The test strategy is illustrated in section III. In section IV we will demonstrate the technique on two analog examples, and finally some concluding remarks are given in section V.

II. Piecewise Linear Approximation

In the general case, the relations between a circuit element's inputs and outputs are non-linear. These non-linear relations can be approximated by a collection of linear affine mappings. Each mapping is valid for a specific range of the circuit element's input/output variables.

The mappings may be stored in a closed-form model [7, 8]. This piecewise linear (PL) model can be analyzed using a PL simulator [9, 13]. Rather than keeping a complete list of all the mappings, they are efficiently stored in the model. Only the current mapping is available. If the input or output variables of the model change

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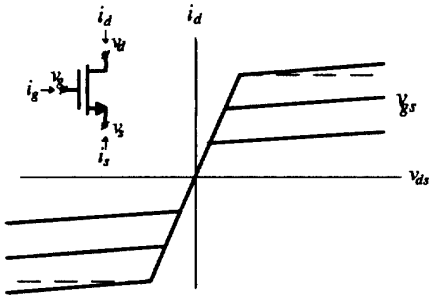


Fig. 1. i_d-v_{ds} Characteristic of NMOS PL model.

to cause the current mapping to be invalid, then a mathematical operator is applied to obtain the new mapping.

In this way the static behavior of a NMOS transistor can be described, as shown in Fig. 1. Here we use a PL mapping from R^4 to R^3 with $\mathbf{x} = (v_d, v_g, v_s, v_{th})^T$ and $\mathbf{y} = (i_d, i_g, i_s)^T$ respectively the input and output variables, and v_{th} the threshold voltage. New in our method is that parameters that must be determined are contained in the input or output vectors of our PL model.

This first-order approximation can be made more accurate at the expense of more linear segments to approximate the i_d-v_{ds} and i_d-v_{gs} characteristics. The PL model of a PMOS can be treated in the same way.

III. Test Strategy

Our test strategy consists of three phases: pre-test, test and post-test. The following definitions are used:

- **p**: The vector of parameters to be determined. It contains for example device parameters like a resistor value. Each entry of **p** is an interval, in this paper an interval for the device parameter v_{th}.
- **t**: The test vector. This vector contains for example the applied input voltages and measured output voltages of the DUT. $\mathbf{t}^{(i)}$ Is the test vector obtained with measurement i.
- **S**: The mathematical relation between **p** and **t**. Thus, **S** represents the DC performance of the DUT, concerning **p** and **t**.

A. Pre-test phase

In the pre-test phase, **p** and **t** are defined by the user. The entries of **p** and **t** are taken from the PL input or output vectors. Therefore, the PL model of the DUT must be constructed so that all entries of **p** and **t** appear in its input or output vectors. For example, in section II it was shown that the threshold voltage is contained in the PL input vector.

Then our simulation program determines the state space **S**. It is obtained as a set of mathematical relations between **p** and **t**. The used method is based on a theory of Tschernikow [10] and is treated in detail in [11, 12]. The necessary operations can quite naturally be combined with the solution methods for PL equations and hence nicely fit in such a type of modeling and simulation.

B. Test Phase

In the test phase, $\mathbf{t}^{(1)}$ ... $\mathbf{t}^{(k)}$ are obtained. Thus the DUT's behavior is measured. Generally, a few measurements suffice to test the DUT.

C. Post-test phase

In the post-test phase the test results may be evaluated as follows. Suppose that we obtained $\mathbf{t}^{(i)}$. Then the parameter vector can be calculated from **S** and $\mathbf{t}^{(i)}$. Define the resulting vector as $\mathbf{q}^{(i)}$. Comparison of $\mathbf{q}^{(i)}$ and **p** shows for this measurement if the parameters are within their allowed intervals. There are three possibilities:

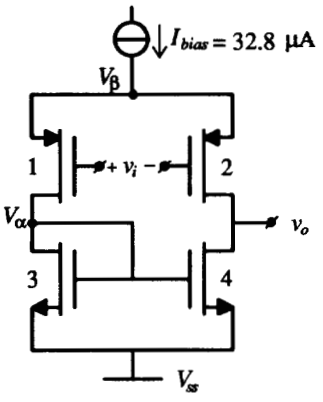
1. One or more parameters are outside their allowed intervals. The DUT does not function according to normal operating conditions.
2. All parameters are single-valued. The DUT operates for exactly one value of the parameters so it functions normally according to measurement i.
3. We obtain a mathematical relation between the parameters from which we cannot infer if any parameters are outside their allowed intervals.

We make the following observations.

- To illustrate our method, only the v_{th} variation is considered. For a more complete DC test, also other parameters must be checked. These parameters are added to vector **p** as explained in section IIIA. More test points can be taken into account at the expense of a larger test vector **t**.
- One measurement only tests the DUT in a certain operating region. More operating regions must be checked to completely test the circuit. Therefore, in the second case the circuit possibly is defective.
- In the third case, more measurements must be made to obtain additional independent relations between the parameters. Thus there are multiple iterations of the test phase and post-test phase, until it is possible to solve for the parameter values.

IV. Example Test Circuit: Operational Transconductance Amplifier

To illustrate our method, consider the test of a simple operational amplifier as depicted in Fig. 2. For simplicity, we will use the same PL models as before to



T_1, T_2: $\frac{W}{L} = \frac{12}{2.4}$, $\lambda = 0.0378$

T_3, T_4: $\frac{W}{L} = \frac{8}{2.4}$, $\lambda = 0.06$

Fig. 2. Operational Transconductance Amplifier.

approximate the non-linear behavior of the MOS transistors.

In the pre-test phase we compute state space S. We define:

$\mathbf{p} = (v_{thp1}, v_{thp2}, v_{thn3}, v_{thn4})^T$,
$\mathbf{t} = (v_i, v_o, v_\alpha, v_\beta)^T$,

with $v_{thp1,2} \in [-0.91, -0.89]$ V
and $v_{thn3,4} \in [0.89, 0.91]$ V.

In this example, v_o, v_α and v_β are measured at bias conditions (v_i = 0V).

In the test phase we measure three devices:

Device 1.

We measure $\mathbf{t}^{(1)} = (0, -3.65, -3.97, 1.11)^T$. Although all individual voltages are within their ranges, it is not possible to calculate a set of threshold voltages that are within the allowed intervals. Thus the DUT is defect.

Device 2.

We measure $\mathbf{t}^{(2)} = (0, -4.0, -3.99, 1.10)^T$. In the post-test phase, from S and $\mathbf{t}^{(2)}$ we calculate parameter vector $\mathbf{q}^{(2)}$ as:

$$\mathbf{q}^{(2)} = \sum_{i=1}^{i=6} r_i \mathbf{a}_i, \sum_{i=1}^{i=6} r_i = 1, r_i \geq 0$$

$\mathbf{a}_1 = (-0.910, -0.910, 0.894, 0.893)^T$,

$\mathbf{a}_2 = (-0.910, -0.898, 0.897, 0.890)^T$,

$\mathbf{a}_3 = (-0.903, -0.890, 0.897, 0.890)^T$,

$\mathbf{a}_4 = (-0.894, -0.890, 0.890, 0.897)^T$,

$\mathbf{a}_5 = (-0.890, -0.907, 0.890, 0.897)^T$,

$\mathbf{a}_6 = (-0.890, -0.898, 0.894, 0.893)^T$.

Each point in this space results in the measured node voltages. To test whether or not the circuit is operating correctly concerning the threshold voltages, additional measurements must be performed. Note that our method also takes into account mismatches in the threshold voltages, since this parameter is considered separately for each transistor.

Device 3.

This example is added to demonstrate how testing time may be saved by using tests of increasing complexity. Suppose we define:

$\mathbf{p} = (v_{thp1}, v_{thp2}, v_{thn3}, v_{thn4})^T$,
$\mathbf{t} = (v_i, v_o)^T$,

with $v_{thp1,2} \in [-0.91, -0.89]$ V
and $v_{thn3,4} \in [0.89, 0.91]$ V,

so we use a more simple test vector.

Note that the test vector contains only one input variable and one output variable. Assume that the threshold voltages are within their intervals. In the pre-test phase we may then use S to obtain the relation between v_i and v_o.

In the test phase we measure $\mathbf{t}^{(3)} = [0, -3.60]$ V. Since v_i is known to be 0V, we can use S to obtain directly $v_o \in [-4.31, -3.65]$V. Obviously, the measured v_o is not in its allowed interval, so we may conclude immediately that the device is faulty.

If v_o would have been in its allowed interval, we would have to use more elaborate tests, actually determining all the threshold voltages, to determine if the DUT is indeed functioning correctly.

Consequently we arrive at the following simple test strategy for the operational amplifier:

1) *Use test vector $t = (v_i, v_o)^T$ to check if v_o is in its allowed interval. If not the DUT is faulty, otherwise proceed with step 2).*

2) *Make additional measurements, using the test vector $t = (v_i, v_o, v_\alpha, v_\beta)^T$.*

Because the first test is much more economical than the second test, and because an error in any v_{th} has its effect on v_o, testing time may be saved by ordering the tests as indicated.

Please note that this last example is included merely to indicate the general useability of our method. It is by no means a complete discussion.

V. Concluding Remarks

In this paper a method is proposed that performs the functional test of an analog circuit by a combination of DC measurements, interval analysis and a PL simulation. The pre-test phase consists of the computation of the state space that contains the relation between the parameters to be considered and the DC data obtained with the test vector. In the post-test phase, the measured data is mapped onto the parameters. Then it is concluded whether or not the circuit is faulty.

The above method is explained in the view of a circuit's test phase. However, it may also be used in the synthesis phase. Then it produces results similar to a Monte Carlo simulation as possible in e.g. SPICE. However our method has two distinct advantages. Firstly, in stead of iterating over several parameter values, the method obtains at once the behavior of the circuit for all values of the parameters. Secondly the behavior is obtained as a mathematical relation between the parameters and the test vector. This is not possible with a simulator like SPICE.

Although in this paper only the threshold voltage deviation is examined, also other physical process parameter or component variations can be considered. The method is demonstrated only for DC voltages, but also other DC data, e.g. DC impedances, can be tested in this way.

Here it must be mentioned that the method of Tschernikow can be time consuming for large systems. However, we have the strong feeling that large systems behave more linearly than non-linear [8,13]. This means that to model such systems, only a few linear mappings are necessary. Therefore fewer segments have to be considered in our method, which will reduce the computing time.

Further research must be done which will lead to a more complete functional test on the wafer, using DC measurements only. Such a test will be less complex and less time consuming than a complete test in all domains. Also the necessary test equipment will be less expensive.

Acknowledgment

The authors wish to thank Prof. dr. ir. W.M.G. van Bokhoven for valuable discussions and suggestions on the subject.

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